Design & Simulation of Low Power Dynamic Logic

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***Abstract*—as far there is vast applications of vlsi circuit designing so regularlythere is introduction of some new techniques goes on to make better of it , as traditionally static cmos found to have some problems regarding power consumption so standard dynamic logic introduced but as far as concern to make better of it ,there is domino logic, another technique that overcomes the problem of dynamic so there are different techniques introduced doing better than the previous one,similarly in this proposed topic there is another technique to make dynamic logic much better to perform regarding with its area ,power speed as well .The technique is "single transistor type dynamic logic" STTDL,using TANNER EDA tools for its designing and simulation.**

***IndexTerms*—STTDL, CMOS, VLSI, TANNER EDA TOOLS.**

I. INTRODUCTION

Although static cmos logic has the lowest static power disscipation,but due to use of a p-type transistor for each n-typedevice in the circuit gives it several disadvantages as a consequence of it speed is degraded as wellbecause the preceding gate has to drive two transistors,the use of larger number of transistors increases capacitance causing degradation of dynamic power dissipation which can be solve by decreasing number of transistorsof one type while leaving the number of other complementary transistor unchanged. A logic which can resolve some of this problem is standard dynamic logic as shown in fig ,driven by clock signal so also known as clocked logic.It consists of pull down NMOS / pull up PMOS logic block and an extra NMOS and a PMOS transistors,Clock is used to ensure that PMOS and NMOS transistors are not turned ON simultaneously ,but this logic has problems when cascadedBecause of floating nodes during evaluation phase so to overcome this problem , domino logic is introduced with the use of an inverter.As foreffective noise tolerant design techniques that incur little overhead in silicon area,speed and power consumption are highly demanded.

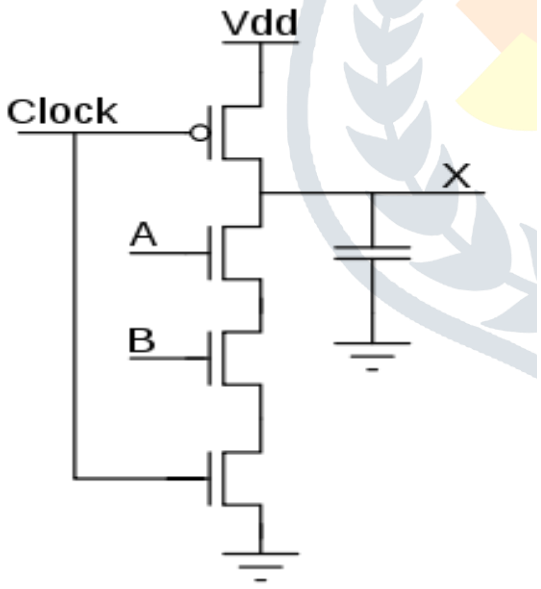


fig 1. STANDARD DYNAMIC LOGIC

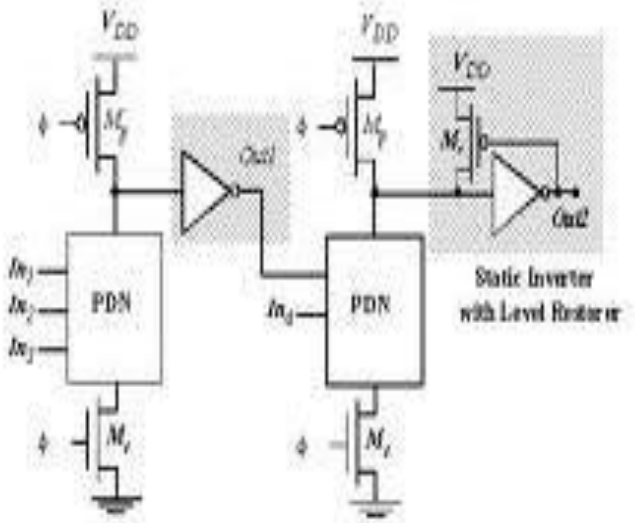


fig 2. Cascaded domino logic

There are several techniques improved and still improving to improve domino logic,In this proposed topic ,another technique has been introduced to improve the performance of domino logic.

The present thesis describes STTDL, a Single Transistor Type Dynamic Logic that can be built entirely with either NMOS or PMOS transistors with the objective of using minimum number of transistors for implementation of a given logic function,proposed technique achieves better performance and simpler design compared to conventional domino logic.

In this proposed topic gated diode is used which is an essential part of it as shown in figure,GATED DIODE is a two terminal device basically used to precharge the boost voltage ,gated diode is also known as variable capacitor as it drain and source is shorted

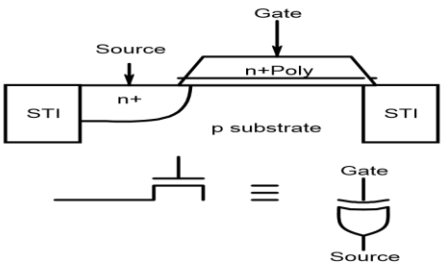


Fig. 3.1: Gated diode structure

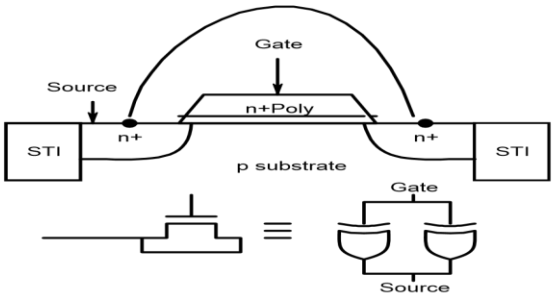
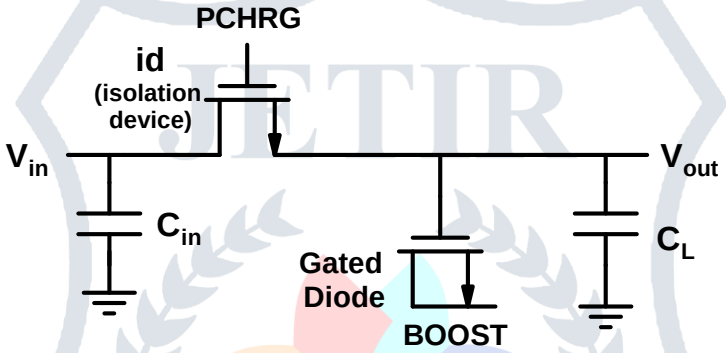


Fig. 3.2: Gated diode structure with source drain shorted

This gated diode will also work in two phase :precharge phase and boost phase or evaluation phase ,as shown below.Inprecharge phase when precharge voltage is high and boost voltage is low ,node connected to gate terminal of gated diode will be precharged by Vin and when in another phase when precharge voltage become low node will disconnectedfrom Vin and boost signal will be precharged depends on precharge voltage,



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$$V_{out}(Boost) \cong V_{out}(Pchrg) + C_{gs}\{V_{out}(P_{chrg})\}C_{gs}\{V_{out}(P_{chrg})\} + C_L \times \Delta V_s$$

Where,

V_{out}(Boost) = Boosted output voltage when Boost signal high

V_{out}(PCHRG) = Output voltage in precharge phase

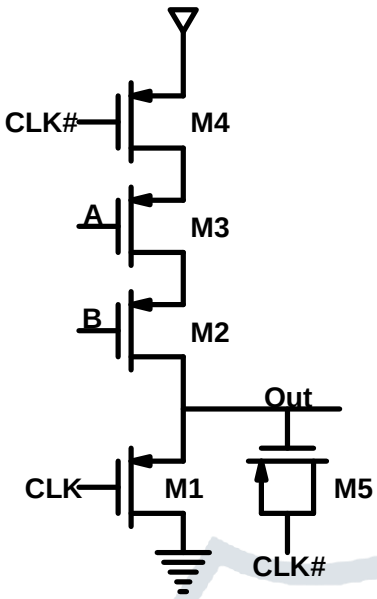
C_{gs}= Gate to source capacitance in precharge phase

C_L = Load capacitance

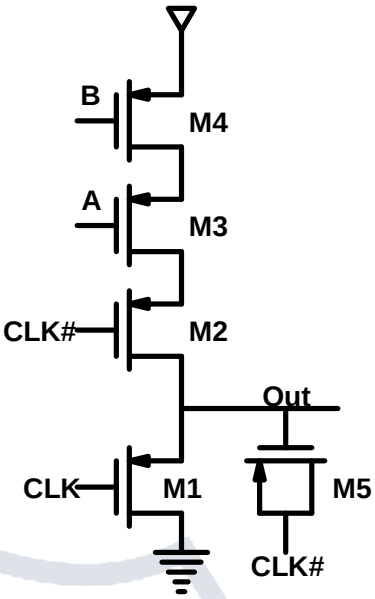
ΔV_S = Change in voltage across gated diode during between precharge and boost phase

With the help of this above explained gated diode proposed single transistor type dynamic logic is design as shown below the**" P type single transistor type dynamic logic"**

Below shows **the 2 input nor gate** design using P type sttdl ,here all the transisitor are Pmos and gated diode M5 ,clock signal are used with inverted clock signal



Clock up configuration

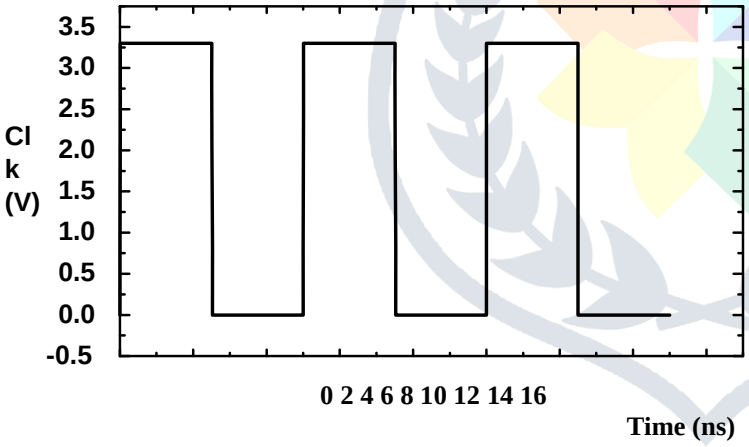


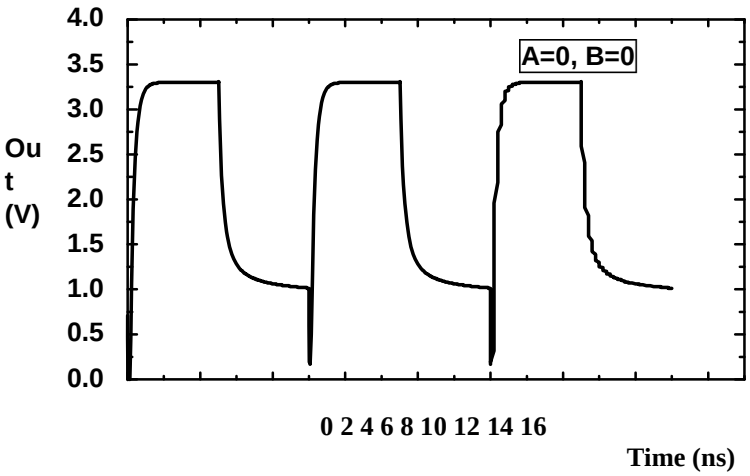
Clock down configuration

P-type STTDL design

It works in two phase namely predischarge and evaluation phase. In the predischarge phase CLK signal is low and CLK# signal is high, resulting in discharge of node 'Out' through transistor M1. However, node 'Out' is not fully discharge due to threshold drop across PMOS transistor M1. This drop can be compensated by PMOS based gated diode M5. During the evaluation phase, CLK signal goes high and CLK# signal goes high. Depending upon the inputs A and B output will either be raised to VDD through pull-up network or discharged through gated diode M5.

Simulation results are shownbelow:





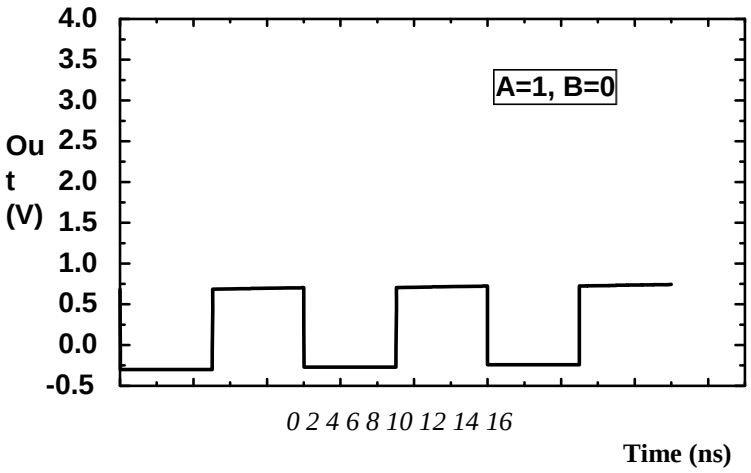


Table:*Because STTDL uses only one transistor type, this design can achieve significant savings in silicon area. Table 1 shows a comparison of area for static cmos, domino logic and proposed P-STTDL NOR gates.*

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No. of inputs (Nor gate)	Area (Static CMOS) (μm^2)	Area(standard domino) (μm^2)	Area (STTDL) (μm^2)
2	32.595	43.99	26.04 (30%, 40%)
3	40.545	43.99	30.225 (25%, 31%)
4	48.495	47.17	34.41 (29%, 27%)

CONCLUSION: In this work, a new dynamic logic family, STTDL, has been proposed, which achieves higher speed, smaller area, and simpler design over the conventional domino logic. A key feature of these dynamic logic styles is the use only Single type of transistors (either PMOS or NMOS) for the complete logic design. Basic building blocks such as NAND, NOR, Half-Adder and a larger carry lookahead adder block were implemented to validate the proposed design

REFERENCES:

[1] D. Harris, "Skew-Tolerant Circuit Design", PhD., Stanford Univ., Stanford, CA, 1999.

[2] Jan M. Raebey, AnanthaChandrakasan and BorivojeNikolic, "Digital Integrated Circuits – A Design Perspective", Second Editions, Pearson Education.

[3] R. H. Krambeck, C. M. Lee, and H. S. Law, "High-speed compact circuits with CMOS," *IEEE J. Solid-State Circuits*, vol. SC- I 7, pp. 614-619, June 1982.

[4] V.G. OWakdzija and R. K. Monoye, "Design-performance trade-offs in CMOS domino logic" *CICC*, pp. 334337, 1985.

[5] N. Goncalevez and H. De Man, "NORA:ARacefree Dynamic CMOS Technique for Pipelined Logic Structures", *IEEE Journal of Solid State Circuits*, Vol. SC -18, no. 3 pp.- 261-266, June, 1983.

[6] R. Rafati, **A.** Z. Charaki, **S.** M. Fakhraie and **K. C.** Smith, "Data-Driven Dynamic Logic versus NP-CMOS Logic, A Comparison", *Microelectronics, 2000. ICM 2000. Proceedings of the 12th Int. Conf.*,Page(s):57 – 60, Oct, 2000.

[7] G.R. Chaji , S.M. Fakhraie and K.C. Smith, "Pseudo dynamic logic (SDL): a highspeed and low-power dynamic logic family, *Circuits and Systems*, Vol. 3, pp. 245,