Asynchronous Viterbi Decoder Using Hybrid Register Exchange Method: A Review

[1]Pooja M. Chandel, [2]Prof.M. N. Thakre , [3]Prof.G. D. Korde

[1]Student Mtech, [2]Assistant Professor,Sel. Grade, [3]Assistant Professor

[1]VLSI, BDCE, Sevagram, Wardha, India

***Abstract*— Viterbi decoders are used to decode convolutional codes.Using Viterbi alogorithm Viterbi decoder decodes a bit stream that has been encoded using convolutional encoder. The choice of asynchronous design was predicted due to its power and speed advantage. HREM is a combination of Trace Back Method(TBM) and Register Exchange Method(REM). HREM reduces the switching activity.There are two types of decision outputs, hard decision and soft decision. As soft decision output is having high error correcting capability than hard decision, accuracy can be increased. In this paper we are proposing a new approach of asynchronous design using HREM.The main aim of proposed method is to reduce power consumption.**

***Index Terms*- Convolutional encoder, Viterbi Algorithm, Viterbi decoder, asynchronous, power consumption, hybrid register exchange method, soft output decision.**

1. INTRODUCTION

With the proliferation of battery powered devices such as cellular phones and laptop computers, power dissipation, along with speed and area, is a major concern in VLSI design. In CMOS technology the major source of power dissipation is attributed to dynamic power dissipation, which is due to the switching of signal values [1]. The Viterbi decoding algorithm was proposed and analyzed by Viterbi in 1967 [2], is widely used as a decoding technique for convolutional codes as well as the bit detection method in storage devices. In more than one billion cell phones Viterbi decoders currently find their use. Viterbi decoders used in digital wireless communications are complex and dissipate large power. The algorithm works by forming trellis structure, which is traced back for decoding the received information. Convolutional encoding with Viterbi decoding is a powerful method for forward error correction. Convolutional codes are considered suitable for protecting the digital data transmission from random errors due to any noise source.

Convolutional codes are very suitable to protecting the digital data transmission from random errors due to any noise source. It achieves error free transmission by adding sufficient redundancy to the source symbols. Convolutional encoder increases the length of the message sequence by adding redundant bits in order to increase the likelihood of detecting the transmitted sequence even if errors have occurred during transmission.[3]

Viterbi decoders [4] are used to decode data which is encoded using convolutional encoders and transmitted over noisy channels. A message encoded using a convolutional encoder follows what is a trellis diagram which shows the different states of the encoder as well as the path taken to encode an arbitrary message. Viterbi's algorithm tries to reconstruct this correct path based on the received stream, despite errors in the received stream. This is done by reconstructing the trellis diagram and allocating a weight to each branch and node (i.e. state) of the reconstructed trellis, at each time slot. By tracing back through the reconstructed trellis, the decoder can detect and correct errors in the received stream.

Two design styles are available for designing the Viterbi decoder i.e synchronous and asynchronous. Synchronous designs are controlled by a global clock, running throughout the entire system. Asynchronous designs, on the other hand, are locally rather than globally synchronized and use handshaking signals between their components in order to perform the necessary synchronization and sequencing of events. There are many advantages to be gained from migrating to asynchronous designs such as negligible power consumption of ideal parts and switching activity is also less. Asynchronous systems produce less electromagnetic emissions. These signals interfere with cellular phones, television and navigation systems. Finally the speed of asynchronous systems is determined by the average delay of all their components. There are two types of decision outputs, hard output and soft output [5]. In soft decision output, error correcting capability is more as compared to hard output decision. So to increase the accuracy as compared with hard decision outputs, soft output Viterbi algorithm can be used.

There are two types of decoding technique, Register Exchange Method (REM) and Trace Back Method (TBM). The REM is simple, but it requires large power consumption and large chip area.TBM is used for large constraint length and for high performance. However, the TBM has drawbacks, which requires last-in-first-out (LIFO) buffer and has to use multiple read operations for high speed operation. This multiple operation results in complex control logic.

This paper provides an overview of the different asynchronous techniques used for reduction of power consumption. In the proposed method the TBM and REM can be combined called as Hybrid Register Exchange Method (HREM) [6] to reduce the switching activity and power. The soft decision output can be used to increase the accuracy.

2. LITERATURE SURVEY

B. Javadi et.al. in paper [7] entitled "An Asynchronous Viterbi Decoder For Low-Power Applications" presents a robust and low-power Viterbi decoder designed based on asynchronous architecture. The design is based upon Quasi Delay Insensitive (QDI) model which leads to a robust functionality for the decoder. To lower the power consumption of the decoder further, an optimization technique to reduce the power dissipation is applied to add-compare select (ACS) unit of the decoder. The simulation results of the optimized asynchronous decoder shows a 20% reduction in power consumption compared to synchronous design in 0.35µm CMOS technology with a power supply of 2.5V.Therefore asynchronous Viterbi decoder could be a good candidate for low-power applications [7].

M. Kawokgy et. al. in paper[8] entitled "Low-Power Asynchronous Viterbi Decoder for Wireless Applications" describes the implementation of an asynchronous 64-state, 1/2-rate Viterbi decoder using an original architecture and design methodology. The asynchronous Viterbi decoder uses a pipelined architecture with asynchronous control units and normally opaque latches. The latch control units were designed as speed independent asynchronous circuits using 4-phase bundled-data protocol. The complete design was carried out using VHDL Hardware Description Language. The decoder, implemented in a 0.18µm CMOS technology, occupies an area of 2 mm and operates upto 213 Mb/s while consuming 85 mW: a 55% power reduction when compared to state of the art synchronous design implemented in a 0.25 µm technology. A simple asynchronous design methodology was developed in this work and allowed the use of commercially available simulation tools as well as standard cell libraries rather than requiring the development of custom libraries geared to asynchronous designs [8].

T.Kalavathi Devi, C. Venkatesh in paper[9] entitled "Design Of Low Power Viterbi Decoder Using Asynchronous Techniques" states that Viterbi decoders employed in digital mobile communications are complex in its implementation and dissipate large power. Fast developments in the communication field have created a rising demand for high speed and low power Viterbi decoders with long battery life, low power dissipation and low weight. Despite the significant progress in the last decade, the problem of power dissipation in the Viterbi decoders still remains challenging and requires further technical solutions. The proposed method is focused on the design of VLSI architecture for a Viterbi Decoder using low power VLSI design techniques at circuit level with asynchronous QDI templates and Differential Cascode Voltage Switch Logic (DCVSL). The simulation results show the asynchronous design has the decrease in power consumption by 56.20% with increase in transistor count by 1.8 times in relative to synchronous Viterbi decoder with code rate of ½ and constraint length of 3 to 7 in 0.25µm CMOS technology with a power supply of 2.5V[9].

M. Kawokgy et. al. in paper[10] entitled "A low-power CSCD asynchronous viterbi decoder for wireless applications" presents a 64-state, 1/2-rate asynchronous Viterbi decoder suitable for wireless and mobile applications. The decoder uses a novel dynamic Current Sensing Completion Detection (CSCD) technique and achieves significant power reduction while maintaining speed. The decoder, implemented in a 90 nm CMOS technology, occupies an area of 0.81 mm^2 and operates at 378 Mb/s while consuming 45 mW: a 43% power delay product improvement when compared to its synchronous counterpart.

3. SUMMARY OF LITERATURE

From the study of all the papers it is observed that the asynchronous techniques used in above papers is implemented in different CMOS technologies has various power consumption. There are different type of asynchronous methods which are used for low power consumption. The various techniques such as QDI technique, handshaking protocols, CSCD techniques are used. The design uses different code rates and achieves maximum speed. Different average power is achieved in every design.

4. PROPOSED METHODOLOGY

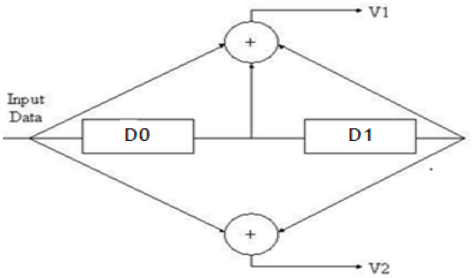

Fig 1. Convolutional Encoder
(r = ½, k=3)

Fig1 shows the convolutional encoder (2,1,3) structure which we have to use in our paper. It consist of 2^m (m=2) shift stages,with a constraint length(k = 3) and modulo-2 adders (n=2) giving the output of the encoder. The rate of the code becomes ½. The output of V1 and V2 of the adders are calculated as follows:

V1= input XOR D0 XOR D1

V2= input XOR D1

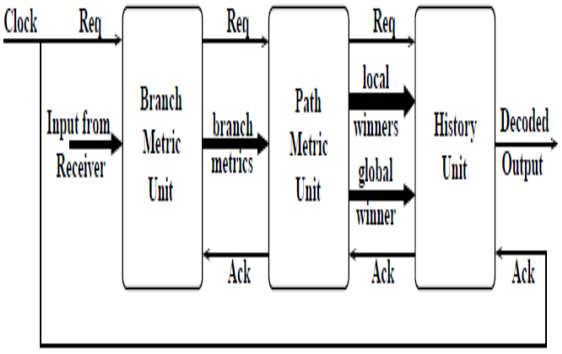

Fig 2.Block Diagram of Asynchronous Viterbi Decoder

Fig2. shows a block diagram of asynchronous Viterbi decoder. It consist of three main blocks which performs the operation.

Branch Metric Unit (BMU): BMU performs the comparison between received code symbol and expected code symbol. It also counts the number of differing bits. Euclidean distance is used for branch metric calculation in case of soft input decoding.

Path Metric Unit (PMU): PMU performs the node plus branch weight calculations and selects the lower weight as the next weight for a node in particular timeslot. The computed node weights are then fed back and become the node weights for next timeslot. On each time slot, this information is passed to the History Unit (HU).

History Unit(HU): The HU uses both the overall winning node information (the global winner) and the local node winners in order to reconstruct the trellis and trace back the path from the current overall winner to find the node indicated by the oldest timeslot stored, the bit for this node is then output.

Asynchronous Techniques

There are different types of asynchronous methods are used, some of them are given below.

Quasi Delay Insensitive (QDI): In digital logic design, Quasi Delay-Insensitive (QDI) circuits are a class of almost delay-insensitive asynchronous circuits which are invariant to the delays of any of the circuit's wires or elements, except to assume that certain fanouts are isochronic. Isochronic forks allow signals to reach two destinations with negligible difference in delay.

4-Phase Handshaking Protocol: In this type of protocol, the request and acknowledge wires also use normal Boolean levels to encode information.

Current Sensing Completion Detection (CSCD) technique: The goal of this method is to detect a predefined current threshold and generate a signal as soon as the transient-current flow is above this threshold level.

Hybrid Register Exchange Method (HREM)

TBM needs to search or trace the survivor path back sequentially which requires much more time compared to REM, and requires extra hardware circuitry. In register exchange method a register is assigned to each state contains information bits for survivor path from initial state to current state. Register keeps the partially decoded output sequence along the path. REM eliminates need to trace back since register of final state contains decoded output. The main drawback of register exchange method is its frequent switching activity and long constraint length. One of the promising solutions to reduce the switching activity can be achieved by combining the REM and TBM techniques. In HREM instead of processing single bit in a cycle, now two bits are decoded, this reduces the switching activity to half as compared to REM.

5. RESULT AND CONCLUSION

Though the power reduction is achieved in above mentioned papers but then also it is having some drawbacks such as the trace back method (TBM) used in the review papers requires last-in-first-out (LIFO) buffer and has to use multiple read operations for high speed operation. This multiple operation results in complex control logic and also the memory requirement is high in TBM. The main drawback of register exchange method is its frequent switching activity and long constraint length. So total power dissipation is high. The hard decision output used in literature review is having less error correcting capability as compared to soft output decision. So the accuracy gets reduced. To overcome these problems, our objective is to design asynchronous Viterbi decoder for low power consumption by using Hybrid Register Exchange Method. HREM reduces high switching activity. To increase the accuracy we are converting encoder output to soft decision. Asynchronous technique is used for low power consumption which is our main objective.

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