32 Nanometer CMOS Analog Switch With Latch Enable Operation

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Abstract: Solid-state analog switches have become an important component in the design of electronic devices and circuits, which require the capability to control and select a specific transmission path for an analog signal. These devices found its applications in multichannel data acquisition systems, process control, instrumentation and measurement, video systems, etc. In this paper, an innovative analog switch using CMOS has been introduced. The layout has been generated in 32 nanometer using Microwind 3.0 and simulation has been performed using Multisim 13.0.

Keywords: 32 nanometer, Analog switch, CMOS, Microwind 3.0, Multisim

1.1 Introduction

The ideal analog switch has zero resistance, infinite impedance and zero propagation delay, and can handle large signal and common-mode voltages. Practical CMOS analog switches do not satisfies these criteria, but if we understand the limitations of analog switches, most of these limitations can be overcome. CMOS switches have an excellent combination of attributes. In its basic form, the MOSFET transistor is a voltage-controlled resistor. In its "on" condition, its resistance is very less, which is less than 1 Ω, while in the "off" state, the resistance increases to several hundreds of mega ohms, with very small value of leakage currents. CMOS technology is compatible with logic circuitry and can be densely packed in an IC.. Its fast switching characteristics are well controlled with minimum effect of circuit parasitic effect. An Analog switch using CMOS is shown below. The simulation has been performed using Multisim software.

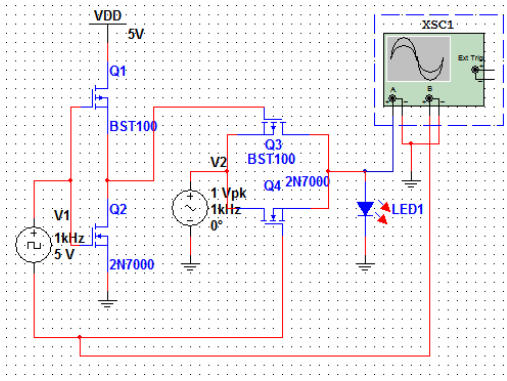

Figure 1.1 Schematic diagram of CMOS Analog switch in Multisim.

Figure 1.2 Input and Output waveform of CMOS Analog switch in Multisim.

The complementary-MOS process (CMOS) yields good P-channel and N-channel MOSFETs. Connecting the PMOS and NMOS devices in parallel forms the basic bilateral CMOS switch of figure 1.1. This combination reduces the on-resistance, and also produces a resistance which varies much less with signal voltage. The load capacitance is 0.01 pF. When the clock pulse applied is "0", PMOS in series connection is ON and the output will be VDD and it will keep the PMOS of parallel connection in OFF state.

At the same time, NMOS in series and parallel connection will be in non-conducting state. Therefore, no input will be transmitted from the parallel connection circuit. When the input applied is "1", PMOS of series connection is OFF and the output is '0', which in turn will turn ON the parallel connection PMOS. At the same time, applied '1' will turn on the NMOS of parallel circuit. Any data applied during this period will be transmitted through this parallel circuit.
When the parallel connected circuitry is not in conducting state then whatever is the output state of inverter circuit, it will appear at the output.
The layout of this analog circuit is shown below using Microwind tool in 32 nanometer process parameter technology.

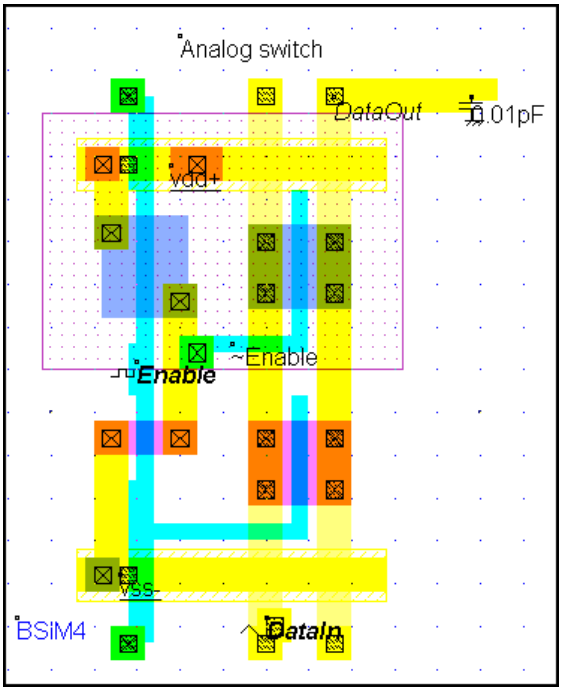

Figure 1.3 Stick diagram layout of CMOS Analog switch in Microwind.

The input and output waveforms for the above layout is shown below. The input is a sinusoidal signal which is depending on clock pulse applied at the inverter circuit. When the clock pulse is high, whatever may be the input it appears at the output circuit through the parallel connected PMOS and NMOS. When clock pulse is low, the inverter output appears across the load capacitance.

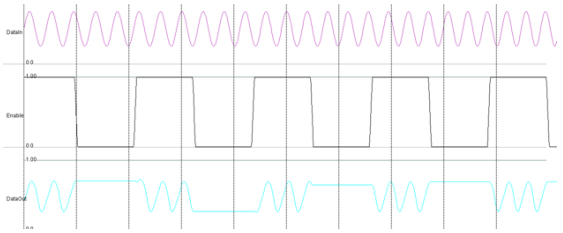

Figure 1.4 Input and Output waveforms of CMOS analog switch in Microwind.

The waveform indicates that when Enable is high the PMOS and NMOS is ON in parallel connection and Data across it appears at the output. But when enable is Low the analog switch acts as a latch in this condition. If the data is low and enable becomes low then the output appears as Low DC. Similarly, if the data is high and enable becomes low then the output appears as High DC. This is nothing but the Latch Operation. Thus, this circuit acts as an analog switch when Enable input is high, but, it acts as switch when enable input across inverter circuit is low. The process parameters for analog switch in 32 nanometre are as follows:

MOS	W (µm)	L (µm)
P1	0.150	0.030
N1	0.060	0.030
P2	0.150	0.030
N2	0.180	0.030

VDD: 1.5 volts

Capacitance (load): 0.01 picofarad

Switching time is an important consideration when being applied in analog switches, but switching time should not be confused with settling time.

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