A Novel Approach of Low Power Low Voltage Dynamic Comparator Design for Biomedical Application

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***Abstract*—A low power dynamic comparator capable of detecting a minimum input voltage difference of 100µV is presented in this article. The comparator is designed and simulated with a supply voltage of both 0.4 V and 1.2 V using UMC 180 nm CMOS technology. All the transistors are compelled to work in the sub-threshold region while working with the supply voltage of 0.4 V. But in case of 1.2 V supply voltage it works in normal region. It consumes 74.09nW power at a frequency of 2 MHz and 136.2 ns delay with a of 0.4 V supply voltage while in case of 1.2 V it consumes 155.70 µW power at a frequency of 500 MHz and 381ps delay.** *(Abstract)*

***Index Terms*— Double-tail comparator, dynamic clocked comparator, ultra-low power, sub-threshold, biosensors, bioelectronics, implantable devices.** *(key words)*

I. INTRODUCTION

Since the invention of first integrated circuit by J. Kilby and R. Noyce in the late 1950s, microelectronics industry has shown an un-dominatable agility to find new dimensions of growth. From the starting of mid 90s it show a new direction of growth opportunity i.e. medical industry. Advancing in microelectronics is also given new possibilities to medical science. Wearable devices have shifted the health care from the hospital to home and allowed to live normal life.

A low power, low-offset, moderate speed comparator is a very important circuit block for biomedical implant devices [1]. There are different types of comparator which can provide the moderate to high speed, like latched comparator, multistage open loop comparator and the dynamic comparator. However the dynamic latch comparator is limited by a huge offset voltage which remarkably affects the resolution whereas bandwidth of amplifier limits the open loop comparator's efficiency. With low offset some architecture on dynamic comparators have already presented in some previous research work but with the cost of high power consumption [2-4]. In [5-7], some conventional dynamic comparators are designed which are capable of working at low voltage without degrading the performance of the circuit. In [7] a comparator is proposed which consumes 18µW while working at a frequency of 600 MHz with a low supply voltage of 0.5V. In [8] a comparator is proposed which works with a supply voltage of 0.6 V and consumes 153µW power while the clock frequency is 1.1GHz. The design architecture of a double-tail dynamic comparator is first proposed in [9] which has separated cross-coupled stage and input stage. As a result, this double-tail comparator can operate fast over a wide range of supply and common mode voltage. In this article, a detailed analysis of a proposed dynamic comparator is presented which is working in sub-threshold region and consumes a considerably low power.

II. DYNAMIC COMPARATOR

Clocked regenerative comparators widely used in high-speed ADCs because of positive feedback in regenerative latch they can operate at faster speed. Many comprehensive analyses of different comparator architecture had already been presented, which investigated different performance of these comparators, like offset [10-12], noise [13], kick-back noise [14] and random decision errors [15]. In this section, an analysis on both the sub-threshold conventional and the sub-threshold dynamic double-tail comparator is done.

CONVENTIONAL DYNAMIC COMPARATOR

In figure 3.1 the circuit diagram of the sub-threshold conventional dynamic comparator [9] is shown. When Clock = Gnd the circuit is said to be in reset phase transistor M_9 is off, transistors M_1-M_4 charge both the output nodes ($Outn$, $Outp$) to V_{DD} (high) which defines the circuit's start condition. When Clock = V_{DD} the circuit is said to be in evaluation phase M_1 and M_4 transistors are off, and M_9 (the tail transistor) is on. Output voltages ($Outp$,$Outn$), which were charged to V_{DD} voltage in reset phase, will discharge but the discharging rates are different. Figure 3.2, shows the total delay of this comparator which has two time delays, t_0 and t_{latch}. The delay t_0 represents the time taken by load capacitance C_L to discharge until the M_2 or M_3 transistor turns on. Let the case be, where the input voltage at node V_{inp} is higher than V_{inn} (i.e., $V_{inp} > V_{inn}$), the drain current (I_8) of M_8 transistor causes fast discharge of $Outp$ node as compared to $Outn$ node, which is driven by M_7 transistor with smaller current.

Now, the discharge delay can be given by equation (1),

$$t_0 = \frac{C_L|V_{thp}|}{I_2} \cong 2\frac{C_L|V_{thp}|}{I_{tail}} \quad \ldots (1)$$

Where I_2 is given by

$$I_2 = \frac{I_{tail}}{2} + \Delta I_{in} = I_{tail/2} + g_{m7,8}\Delta I_{in} \quad \ldots (2)$$

Where I_{tail} is the current of transistor M_9.

The latch delay can be given by equation (3),

$$t_{latch} = \frac{C_L}{g_{meff}} . \ln\left(\frac{\Delta V_{out}}{\Delta V_0}\right) = \frac{C_L}{g_{meff}} . \ln\left(\frac{V_{dd}/2}{\Delta V_0}\right) \quad \ldots (3)$$

Where t_{latch}, is the latching of two cross-coupled inverters.

Where g_{meff} is the effective trans-conductance of the back to back inverters. The ΔV_0 is given by equation (4),

$$\Delta V_o = 2 \mid V_{thp} \mid \sqrt{\frac{\beta_{7,8}}{I_{tail}}} \Delta V_{in} \quad \ldots (4)$$

Where $\beta_{7,8}$ is the current factor of input transistors.

The total delay t_{delay}[16] of the conventional dynamic comparator can be given by equation (5)

$$t_{delay} = t_o + t_{latch} = 2\frac{C_l|V_{thp}|}{I_{tail}} + \frac{C_l}{g_{meff}} . \ln\left(\frac{V_{DD}}{4|V_{thp}|\Delta V_{in}}\sqrt{\frac{I_{tail}}{\beta_{7,8}}}\right) \quad \ldots (5)$$

DOUBLE TAIL DYNAMIC COMPARATOR

Figure 3.3 depicts the circuit diagram of double tail dynamic comparator operating in sub-threshold region. When clock = Gnd (low) the circuit is said to be in reset phase and the tail transistor M_1 and M_{12} are off, M_8 and M_9 transistor charges nodes F_n and F_p to V_{DD}, which causes the transistor M_6 and M_7 to discharges the Output nodes($Outn$, $Outp$) to ground. When clock = V_{DD}, the circuit is said to be in evaluation phase and the tail transistor M_1, M_{12} are turned on and the $Outp$ and $Outn$ will start to charge. Transistor M_8 and M_9 are turned off and the voltage at nodes F_n and F_p will starts to drop. The discharge rate of F_n and F_p are different because it depends on the input voltages. Let the case be where $V_{inn} > V_{inp}$, in this case the discharge rate of node F_n will be more then node F_p and therefore transistor M_6 and M_7 will turn off at different time intervals. Thus $Outn$ node will get charged to V_{DD}-$|V_{thp}|$ before the $Outp$ node, the corresponding transistor M_3 will be turned on and $Outn$ discharges to ground and $Outp$ will charge to V_{DD} as shown in figure 3.4. The circuit works vice versa if $Vinp > Vinn$. The intermediate stage consists of transistors M_6 and M_7 passes the $\Delta V_{Fn(p)}$ (input dependent differential voltage) voltage to cross coupled inverters and provide a batter shielding between input and Output, which results less kickback noise. The delay of conventional double-tail comparator consists of two parts, t_o and t_{latch}. The t_o delay characterizes the load capacitance C_{out} charging (at the output nodes, $Outn$ and $Outp$) until the turns on of the first n-channel transistor (M_4/M_5), after that the latch regeneration begins, thus t_o can be obtained by

$$t_O = 2\frac{C_L V_{thp}}{I_{tail}} \quad \ldots (6)$$

Where I_{B1} = drain current of the $M_4 \approx$ half of tail current I_{tail2} (M_1). The latch delay for the double tail comparator can be calculated from equation 2.

$$t_{latch} = \frac{C_l}{g_{meff}} . \ln\left(\frac{V_{DD}/_2}{\Delta V_o}\right) \quad \ldots (7)$$

Output voltage difference at the time t_0, ΔV_o is given by

$$\Delta V_o = \left(\frac{2V_{thn}}{I_{tail2}}\right)^2 . \frac{C_{L,out}}{C_{Ln(p)}} . g_{mR10} . g_{m10,11}\Delta V_{in} \quad \ldots (8)$$

Substituting the ΔV_o in t_{latch} the delay t_{delay} [16] of the conventional double tail comparator can be given by,

$$t_{delay} = t_o + t_{latch} = \frac{2V_{thn}C_{Lout}}{I_{tail2}} + \frac{C_{Lout}}{g_{meff}} . \ln\left(\frac{V_{DD} . I_{tail}^2 C_{Ln(p)}}{8V_{thn}^2 . C_{Lout} . g_{mR10,11}\Delta V_{in}}\right) \quad \ldots (9)$$

PROPOSED DYNAMIC COMPARATOR

Figure 3.5 depicts the circuit diagram of proposed dynamic comparator which can be made to operate both in sub-threshold and normal saturation region. During reset phase Clock= Gnd (Low) and M_{19} tail transistor is off, transistor M_{15} and M_{16} charges nodes Fn and Fp to V_{DD} voltage, which causes the transistors M_7 and M_8 to discharge the output node to ground. In the decisive phase Clock = V_{DD} (High), M_{19} tail transistor is turned on and M_7-M_8 turned off and the voltage at nodes Fn and Fp starts to drop. The transistor M_1 and M_2 and M_9 to M_{14} will be turned on when the voltage at the nodes Fn and Fp is low enough. Now the $Outp$ and $Outn$ can start to charge. Consider the case where $Vinp > Vinn$, in this case the discharge of node Fp will be more then Fn. Therefore transistor M_2 and M_{12}-M_{14} will be turned on before transistor M_1 and M_9-M_{11}. The output now start to charge and because of different discharging rate of node Fn and Fp, $Outp$ charges at faster rate then $Outn$ and reaches a voltage at which transistor M_6 will be turned on and $Outn$ will discharge to ground and $Outp$ will be charge to V_{DD}. The circuits works Vice versa if $Vinn > Vinp$. In figure 3.6 the waveform of the proposed dynamic comparator is shown.

III. FIGURES

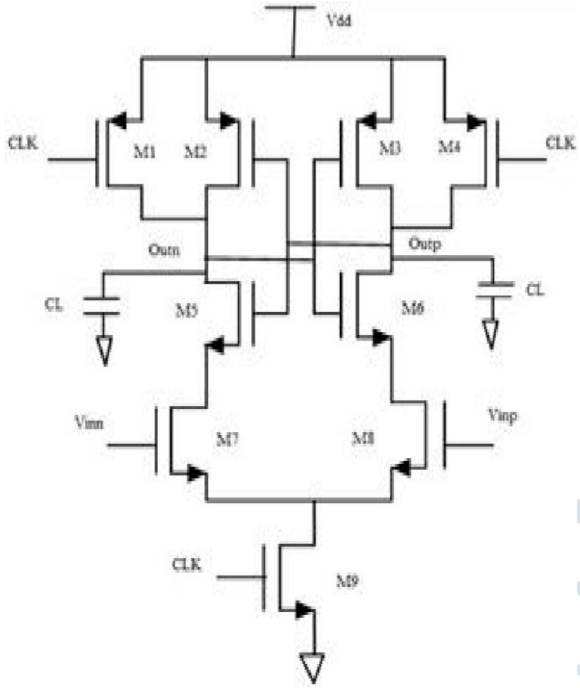

Figure 3.1 Circuit diagram of conventional dynamic comparator

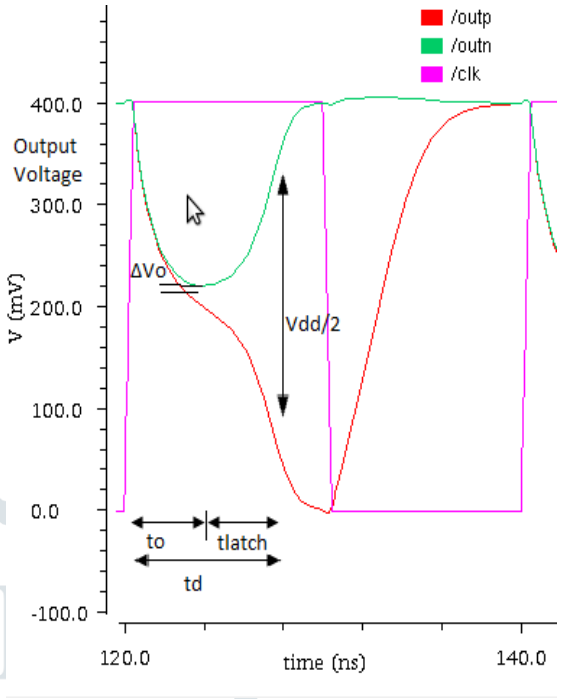

Figure 3.2 Transient simulation of conventional dynamic comparator for V_{CM} = 350mV, ΔV_{in} = 100µV, V_{DD} = 0.4V

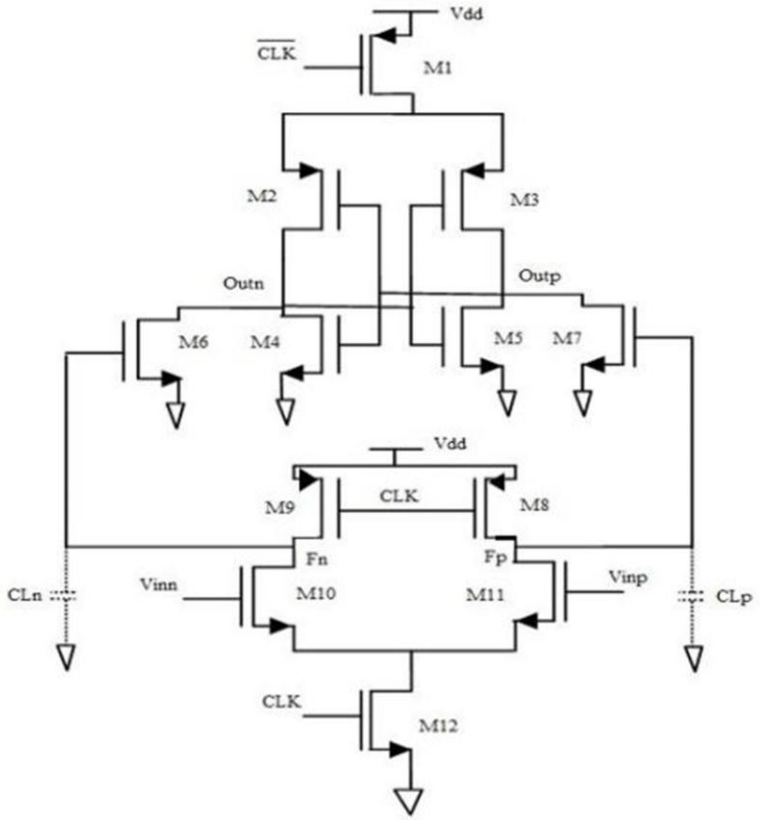

Figure 3.3 Circuit diagram of Double-tail Dynamic comparator

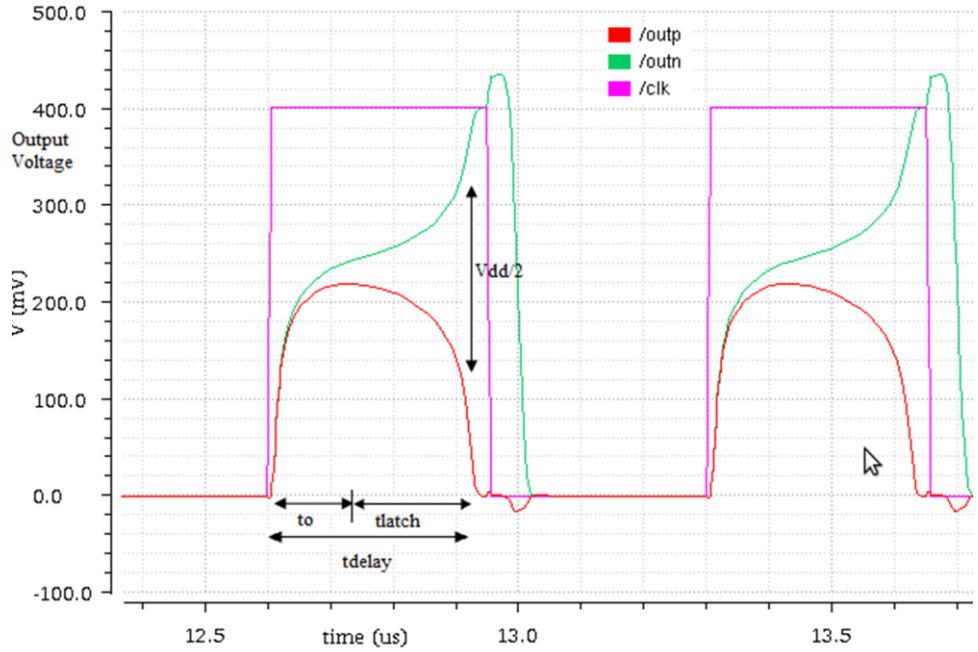

Figure 3.4 Transient Simulation of Double tail Comparator for V_{CM} = 350mV, ΔV_{in} = 100µV, V_{DD} = 0.4V.

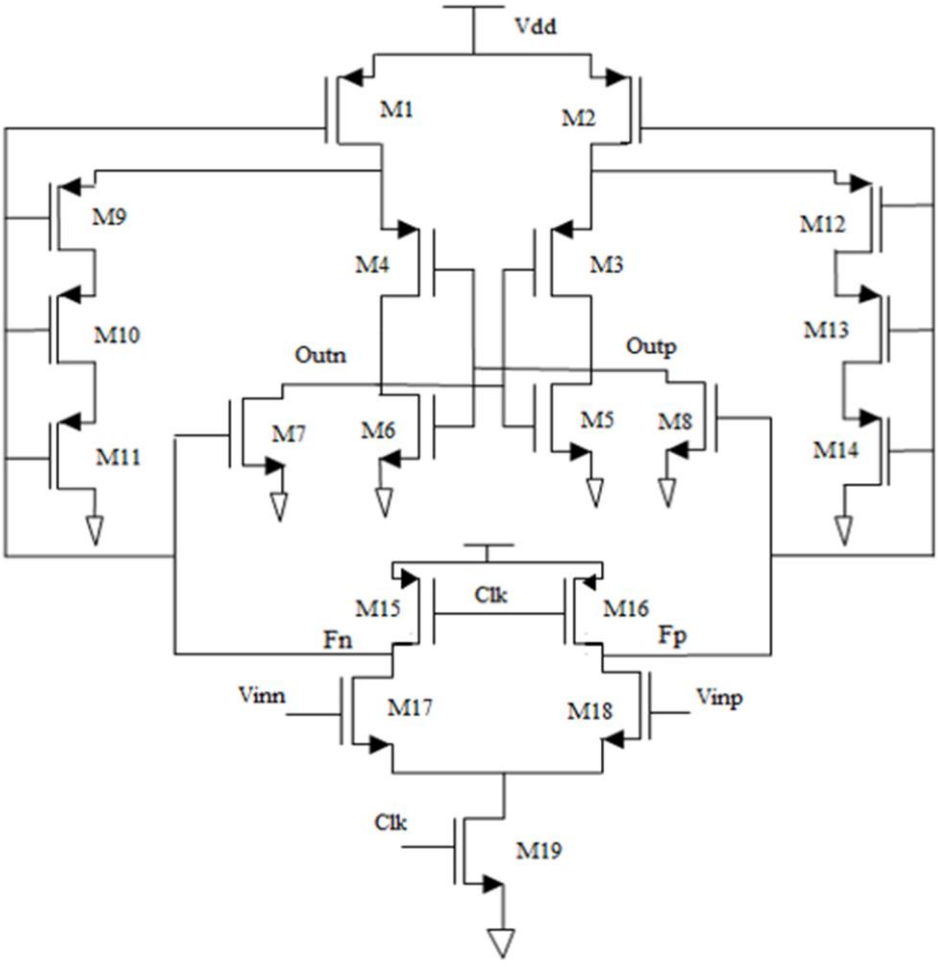

Figure 3.5 Circuit diagram of Proposed Dynamic comparator

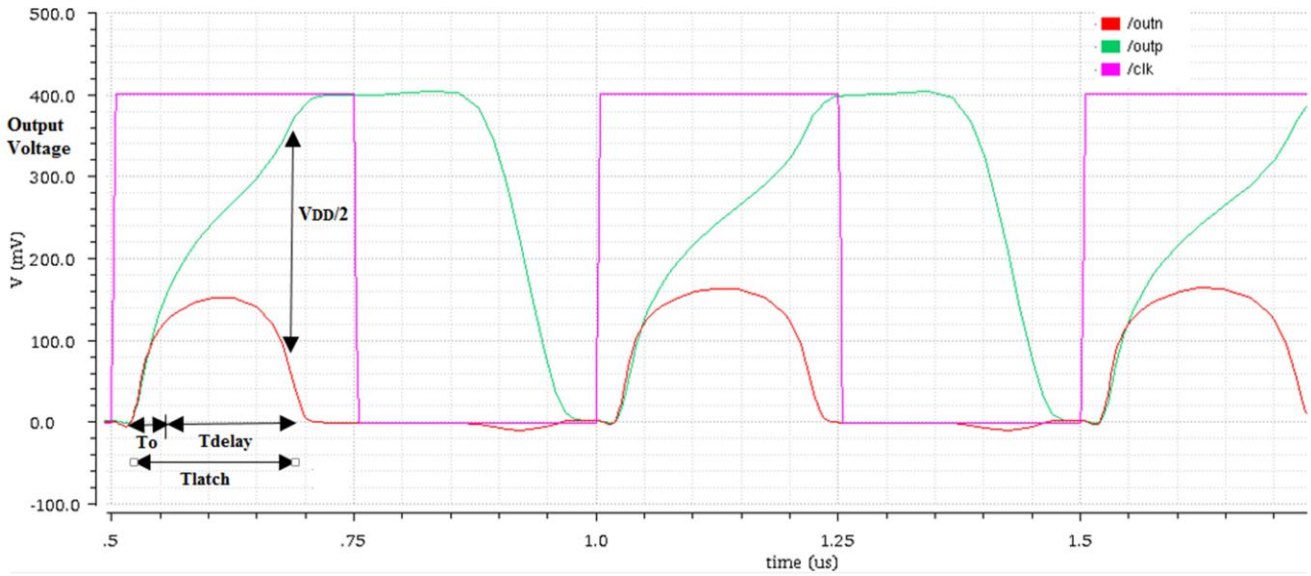

Figure 3.6 Transient Simulation of Proposed dynamic Comparator for V_{CM} = 350mV, ΔV_{in} = 100µV, V_{DD} = 0.4V.

IV. TABLES

Table 1. The performance comparison between conventional dynamic Comparator and double-tail dynamic comparator with differential input voltage of 100µV and common mode voltage of 350mV at 0.4V of power supply.

Comparator Structure	Conventional Dynamic Comparator	Double-tail Dynamic Comparator
CMOS Technology	*180 nm*	*180 nm*
Supply Voltage	*0.4 V*	*0.4 V*
Sampling Frequency	*400 KHz*	*1 MHz*
Delay	*1.109 µs*	*312.18 µs*
Total Power Consumption	*134.3 nW*	*67.07 nW*

Table 2. The performance comparison between double-tail dynamic comparator, proposed dynamic comparator operated in saturation region and proposed dynamic comparator operated in sub-threshold region with differential input voltage of 100µV and common mode voltage of 350mV.

Comparator Structure	Double-tail Dynamic Comparator [16]	Proposed Dynamic Comparator	Proposed Dynamic Comparator (Sub-threshold)
CMOS Technology	*180 nm*	*180 nm*	*180 nm*
Supply Voltage	*1.2 V*	*1.2 V*	*0.4 V*
Sampling Frequency	*500 MHz*	*500 MHz*	*2 MHz*
Delay	*550 ps*	*381.4 ps*	*136.2 ns*
Total Power Consumption	*329 µW*	*155.70 µW*	*74.09 nW*

Remark. A low power low delay time dynamic comparator has been presented which works both on sub-threshold and normal saturation region. The comparator consumes 74.09 nW power at a frequency of 2MHz and 136.2ns delay while working with 0.4 V supply voltage. When the supply voltage is 0.4 V, all the transistors are compelled to work in sub-threshold region. While working with 1.2 V supply voltage, it consumes 155.70 µW power at a frequency of 500 MHz and delay as low as 381 ps. This comparator can detect a minimum input voltage difference of 100 µV which is essential for EEG and ECG application.

As the proposed ultra-low power Dynamic Comparator consumes very low power with small delay time, it is suitable for the implantable biomedical devices such as cardiac and non-cardiac pacemaker.

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