A review paper on design of FPGA based high speed notch filter using parallel processing

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***Abstract*— In this paper, we present a Field-Programmable-Gate-Array (FPGA) based design and implementation of extremely high speed realization of tunable Infinite Impulse Response (IIR) notch filter. The basic 2nd ordered tunable notch filter structure is implementable in FPGA. Here, we propose a FPGA based design of extremely high speed tunable notch filter effectively operating at maximum clock frequency of ~1200MHz with the help of Scattered-Look-Ahead (SLA) parallel processing. FPGA based design for speed up factor, a new efficient simpler approach utilizing Pascal's Triangle is used to calculate the multiplier coefficients of feed-forward and feedback sections of extremely high speed notch filter. The post place & route synthesis results for its FPGA design are obtained by generating VHDL code showing that proposed restructured notch filter can operate effectively greater than 1200MHz clock frequency meeting the present days' certain industry's needs.**

***Index Terms*- Scattered-Look-Ahead (SLA) parallel processing, Pascal Triangle, Tunable Notch Filter**

I. INTRODUCTION

The notch filter is very essential to remove the unwanted interfering signal in present day's communication (GSM, Spread Spectrum Receiver, etc.) [1] as well as non-communication receivers (e.g. Radar, Electronic Support Measure Receiver (ESM), etc.). The requirement of digital notch filter to operate at extremely high clock frequency (in the order of Giga Samples per Seconds, GSPS) comes when military ESM receiver operating in wide-open configuration needs real-time processing of intercepted radar signal (especially in V/UHF band) which is to be extracted by suppressing unwanted communication signals (e.g. FM, Spread Spectrum, Impulse Radar, Impulse Jammer, etc.)[2] in the same band of interest. Notch filter implemented in FPGA need not to be operated at I/O clock (ADC clock of ~1200MHz), even it may be sufficient to achieve effective notch filter throughput rate of 1200MHz, if they operate at In SLA parallel processing with power-of-2-decomposition on basic Nth order notch filter with N poles, results in extra 2logN M multipliers with speed up factor M (i.e. M or multiple of M delays in feedback path of IIR filter) [3][4].

These coefficients can be derived through the use of Pascal's Triangle. System clock (FPGA clock of ~300MHz) with divided by J=4 of I/O clock. The cost paid for this extremely high speed is increase in latency, silicon area and power consumption in FPGA .In general, SLA parallel processing with power-of-2-decomposition on basic Nth order notch filter with N poles, results in extra 2log N M multipliers with speed up factor M (i.e. M or multiple of M Delays in feedback path of IIR filter). The coefficients can be derived through a simpler method of Pascal's Triangle [5].

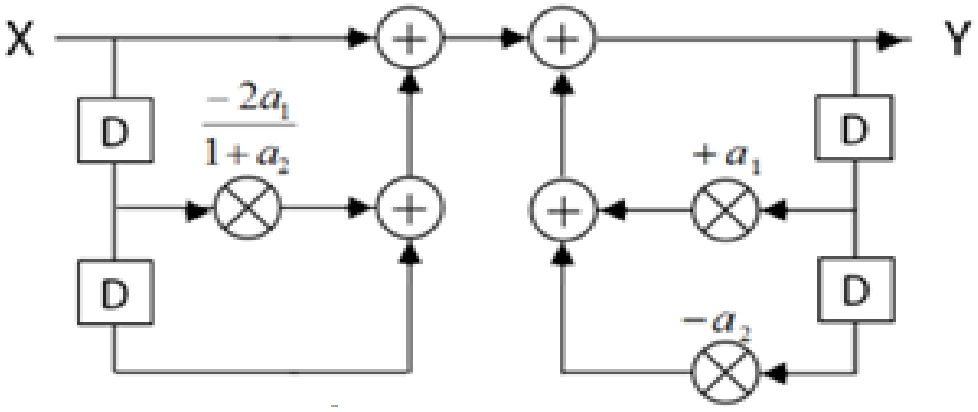

Fig 1: 2nd Order IIR Notch Filter

II. To derive Simple method multiplier coefficient with use of Pascal's Triangle

The coefficient of transfer function can be calculated by using this easy and new method. The values of coefficient can be calculated by subtracting values of square from circle. The first coefficient value is 16-0=16.The second coefficient value is 105-1=104. The third coefficient value is 364-12=352.In this way coefficient of transfer function of filter is obtained.[8][9]

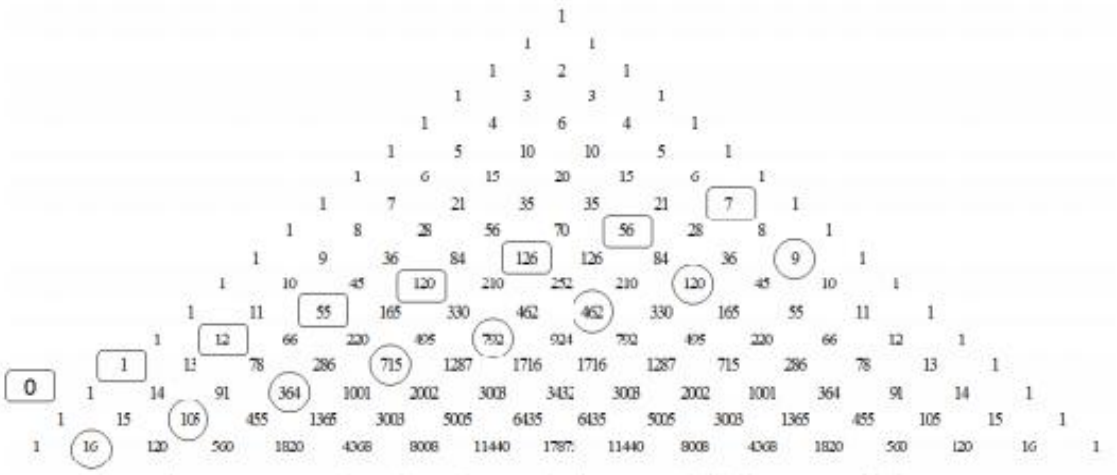

Fig 2: Pascal Triangle to derive Multiplier Coefficients.

III. LITERATURE REVIEW

8. Sounak Samanta and Mrityunjoy Chakraborty "**FPGA Based Implementation of High Speed Tunable Notch Filter Using Pipelining and Unfolding'' IEEE 2014.**
Explanation:- In this FPGA based design of extremely high speed tunable Notch filters develop with the help of Scattered-Look – Ahead pipelining. The concept of pipelining, retiming, unfolding used and high speed ADC with FPGA makes Notch filter to work for high speed. The high speed comes due to enhancement sampling speed of Analog –to-Digital Converter.

9. Bahram Rasidi, Bahman Rasidi, Mojid poyrormazd "**Design and implementation of low power digital FIR filter based on low power multipliers and adder on Xilinx" IEEE2011.**
This method reduces dynamic power consumption of a digital finite impulse response FIR filter .This method include low power serial multiplier and serial adder. Combination of both multiplier, shift/add multiplier, folding transformation in linear phase architecture and applied to FIR filter reduce power consumption due to glitching. The minimum power achieved is 110nw in FIR filter .The proposed FIR filter were synthesized implemented using XILIX ISE, VIRTEX IV FPGA and power is analyzed using Xilinx power analyzer.

IV. PRINCIPLE OF OPERATION

In our project, input signal passes through three stages 1) Input stage2) Filter stage 3) Feedback stage. When input signal passes through input stage .In this stage delay is given to input stage in order to obtained constant speed .In second stage that is filter stage signal is multiplied by multiplier coefficient by Pascal triangle. We will get output whose frequency is less. In third stage that is feedback stage all frequency component is not removed by previous stage. So this signal is feedback till we will notch particular frequency

V. CONCLUSION

FPGA based design and implementation methodology of extremely high speed Notch filter is presented. The concept of parallel processing makes notch filter work effectively. Clock throughout as high as 1200Mhz.A new efficient and easy technique has been used to calculate the multiplier coefficient of extremely high speed IIR notch filter using Pascal triangle. The extremely high speed at the cost of increase in latency, FPGA silicon area and power consumptions

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