ESTIMATION OF THERMAL, NOISE IN SWITCHED-CAPACITOR NETWORK

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Abstract

In this paper presents the sources of noise include the *intrinsic* noise generated in the MOS transistors, as well as the *extrinsic* (interference) noise originating, typically, from the on-chip digital circuitry, and coupled into the sensitive analog stages via the substrate and supply or ground line. There are two important intrinsic noise effects in MOS transistors: thermal and flicker noise. In this paper, the effects of thermal noise on the performance of SC circuits will be discussed, and an efficient algorithm has been described for estimating the magnitude of these effects. The model was verified by comparing the estimation results for a typical SC integrator with those given by a state-of the art CAD program.

Keywords: intrinsic noise, SC circuit, MOS transistors.

INTRODUCTION

One of the main limitations of the performance of switched-capacitor (SC) circuits is noise. The sources of noise include the *intrinsic* noise generated in the MOS transistors, as well as the *extrinsic* (interference) noise originating, typically, from the on-chip digital circuitry, and coupled into the sensitive analog stages via the substrate and supply or ground line.

There are two important intrinsic noise effects in MOS transistors: thermal and flicker noise. Thermal noise is caused by the thermal motion of the charge carriers in the channel of the device. This causes a small amount of random fluctuation in the drain current. If the transistor operates in its triode region, as it does for a conducting switch, the noise can be

represented by a voltage source in series with the device. The power spectral density (PSD) of its voltage is white; its estimated value is given by

$$S_{vt}(f)=4kTR_{on}(V^2/H_z) \quad (1)$$

Here, is the Boltzmann constant, K = 1.38 x 10^{-23} J/K,T is the absolute temperature of the device in degree Kelvin, and is its on-resistance in ohms. The mean value of the thermal noise is zero.

Note that here, and in the rest of this paper, all PSDs are regarded as one-sided distributions, so the noise power between f_1 and f_2 is obtained simply by integrating S (f) between f_1 and f_2.

For a MOSFET operating in strong inversion and in its active region, the thermal noise can be modeled by a current source in parallel with the channel. The PSD of the noise current is to a good approximation given by

$$S_{it}(f)=\frac{8}{3}kTgm(A^2/Hz) \quad (2)$$

Where g_m is the transconductance of the device.

Flicker noise or 1/f noise is caused by charge carriers getting trapped and later released as they move in the channel. It is usually modeled by a series noise voltage source connected to the gate. The PSD of this voltage is approximately given by

$$S_{it}(f)=\frac{K}{WLf}(V^2/Hz) \quad (3)$$

Where and are the width and length of the channel, is the frequency, and is a fabrication parameter. Note that S_{vF} (f) is not white; most of its power is concentrated at low frequencies.

It many cases, the effects 1/f of noise may be reduced using large input devices, and choosing them as pMOS rather than nMOS transistors. Also, correlated double sampling or chopper stabilization [1], [2] may be used to suppress the 1/f noise, or to modulate it to out-of ban frequencies.

In this paper, the effects of thermal noise on the performance of SC circuits will be discussed, and an efficient algorithm has been described for estimating the magnitude of these effects. Section 2 considers the noise effects in the CMOS operational amplifiers (op-amps) commonly used in SC circuits. Section 3 contains a general analysis of filtered and sampled thermal noise. Section 4 described an algorithm for calculating the More discussion of some issues mentioned in this paper can be found in [4] and [5].

THERMAL NOISE EFFECTS IN CMOS OP AMPS

Next, the estimation of thermal noise in op-amps will be discussed. As an illustration, a differential pair (which may be the input stage of a multistage op-amp) is shown in Fig. 1, along with its thermal noise current sources. There represent the effect of the noise currents given in (2). It can readily be seen that the noise current of the tail device Q5 does not contribute to the output current, since it is present in the drain currents of both Q2 and Q4, and hence, cancels in the output current under ideal matching conditions. (This is a good approximation only at frequencies where the gains and delays of the two paths match.[2]) The noise currents of the input devices (assumed to be perfectly matched) can be represented by equivalent noise voltage sources at their gate terminals. From (2), the PSDs of these sources are given by $(8x3)k/T/_{gm1}$.

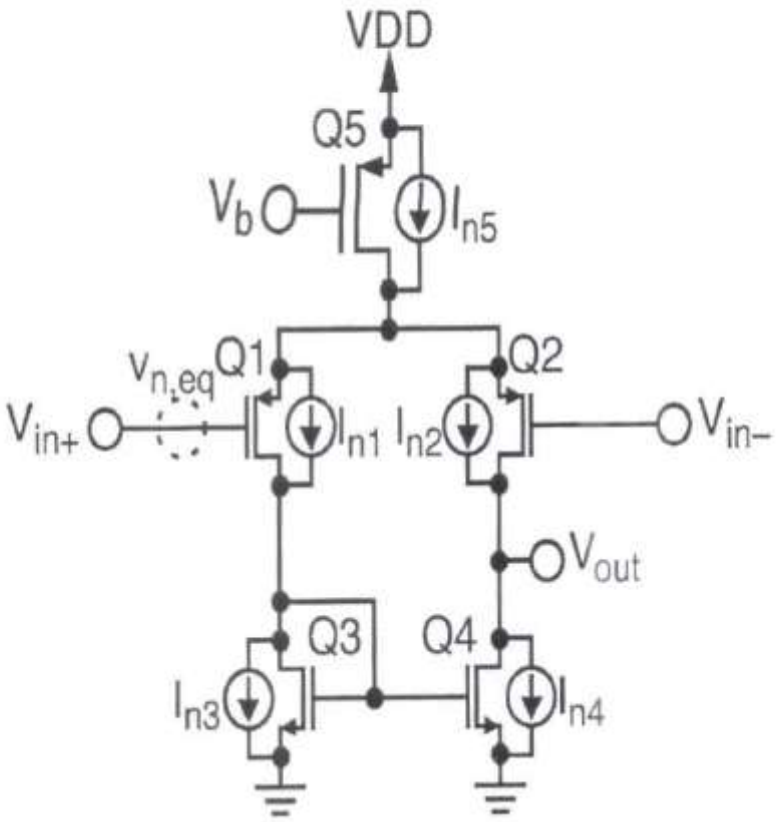

Fig. 1 Noise Sources in a simple CMOS op-amp.

The noise current of Q3 can also be represented by a voltage source at the gate of Q1. The PSD of this sources is $(8x3)k/T/_{gm31/g^2_{ml}}$. Similar considerations hold when 2More importantly, it is a good approximation in fully differential circuits.

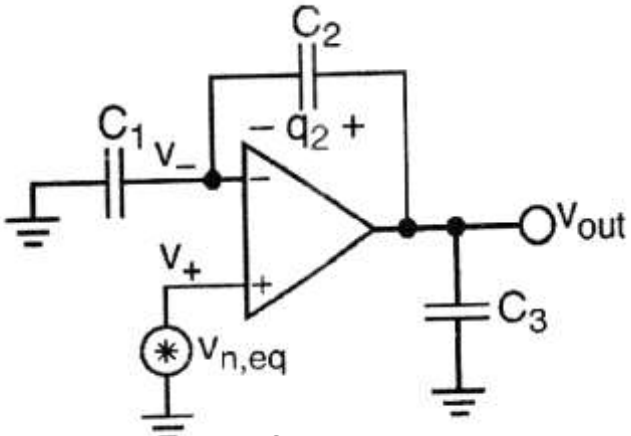

Fig. 2. Op-amp with capacitive feedback and capacitive loading.

the noise of Q4 is represented by an equivalent source at the input of Q2.

Combining these results, the total thermal noise of the stage may be represented by a single equivalent noise voltage sources at the gate of Q1 (or Q2). Its PSD is

$$S_{vt}(f) = (x) = \frac{16kT}{3gm1}\left(1+\frac{gm3}{gm1}\right) \approx \frac{16kT}{3gm1} \qquad (4)$$

The first equality of (4) suggests that for low noise should be used, which justifies the approximation made in the last part.

Consider next the op-amp under negative feedback conditions (Fig. 2). Note that the op-amp noise is represented by the equivalent source and that no signal is present since only the noise amplification is analyzed. It will be realistically assumed that the op-amp is properly compensated, so that in the frequency range of interest (where the loop gain is 1 or larger) the closed-loop transfer function can be approximated by the one-pole expression.

$$H(s) = \frac{V\,out\,(S)}{V+(S)} = + \frac{G0}{1+ST} \qquad (5)$$

Here, G_0 is the dc gain of the stage, and τ is its settling time constant, is determined by the feedback factor $\beta = C = C_2/(C_1+C_2)$ and by the de gain of the op-amp.

Since the settling time is determined by how fast the op-amp output current can charge the load capacitances, will τ will be proportional to $1/_{gm1.}$ Also, since feedback reduces, τ it may be written in the form, $\tau = C_0/(\beta_{gm1})$ where C_0 depends on the structure of the op-amp. For a two-stage op- amp, $C_{c,}$ is the compensation capacitance connected between the stages. For a single-stage (folded- or telescopic-cascode) op-amp, is the load capacitance at the output node of the op-amp: $C_0 = C_{load} = /C3+ C_1C_2/(C_1+C_2)$

The PSD of the white input noise becomes shaped at the output by the first-order low-pass filter function given in (5).

INTEGRATOR NOISE ANALYSIS EXAMPLE

The following example illustrates how to calculate the output noise for the integrator shown in Fig. 3, given some specific values.

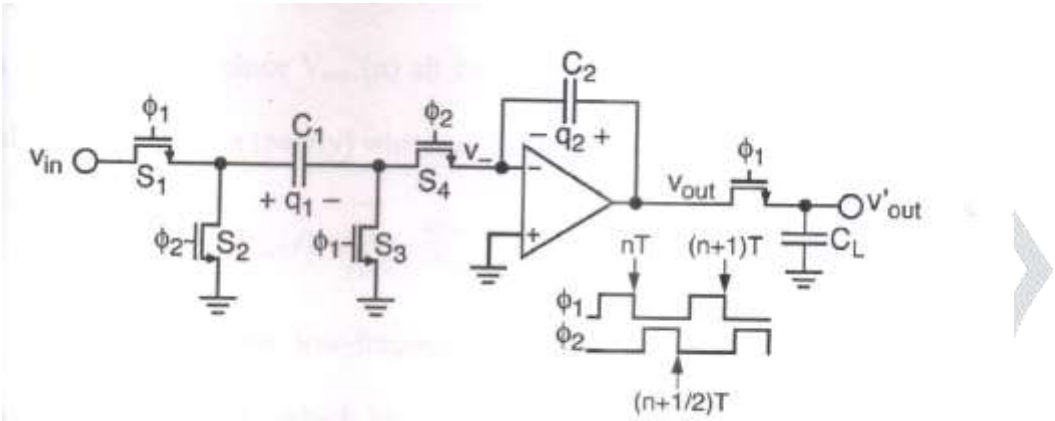

Fig. 3 A stray – insensitive SC integrator.

It is assumed that the flock frequency is f_s = 100 MHz. The signals must settle to an accurancy of N = bits, and an input-referred noise voltage V is desired. The integrator has a gain factor, and must drive the load capacitance pF during phase. To ensure that the op-amp dominates bandwidth noise, was selected

These specifications are used next to calculate the circuit parameters. The settling time constant is determined as ns, and thus 7.6 times smaller than the settling period of $0.5/f_s$= 5ns. The amplifier is an OTA with transconductance g_{m1}=mA/V. For simplicity, to make the de again A = 100, the output impedance is assumed to be R_1 = 680.3 kΩ The input capacitance is then calculated as C_1=0.97pF, and C_2=C_1/k=0.97 pF. The switches must have an on-resistance.

The PSD of the output-referred noise is given by

$$S_w=S_{vis} \mid H \mid^2 + S_{voul} \qquad (7)$$

The parameter is the integrator gain facor, as defined above. A|so,|υ=1A=10^{-3}.

The parameter in the input-referred noise source is x = 2_{gm} R_{on}.

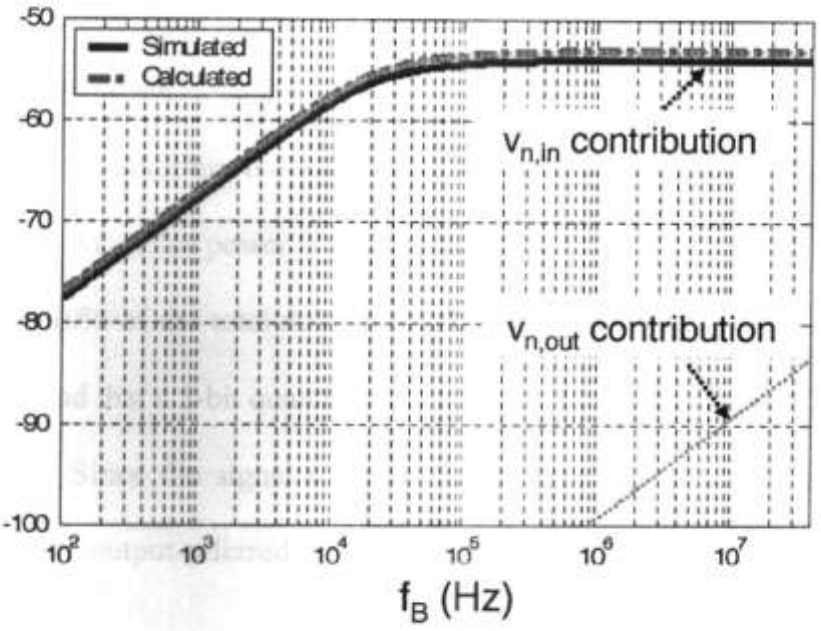

Fig.4 Calculated and Simulated integrated noise powers at the output of integrator.

The output noise power can also be simulated by a dedicated CAD tool, such as RF [8]. This circuit simulator has built-in analysis routines that can handle discrete-time circuits. Fig. 4 shows the calculated and simulated output powers, as functions of f_g. It also shows the noise constribution of $V_{n,\ out,}$ which is negligible here for all values of fg shown, as predicted earlier. The good agreement between the calculated noise and the simulated one confirms the usefulness of the theory discussed earlier.

THERMAL NOISE EFFFECTS IN A DELTA-SIGMA LOOP

As an example of the use of the described noise estimation algorithm, we shall next apply it to the design of a second order low- distortion delta-sigma modulator. We shall assume

an oversampling ratio OSR= 32, a maximum input signal power of 0.25 V2(-6.0 dBV), and a desired 13-bit performance (i.e.c., an SNR of 80.0 dB). The total permissible noise power (including quantization error, extrinsic noise, etc.) is then $10)^{-6.0-80.00)/10}$ V^2= (50.1 μV)^2. Assigning 75% of the noise power to thermal noise [4], the total permissible input-referred thermal noise power turns out to be v= (43.4 μ V)^2.

In addition, the quantizer resolution must be chosen such that the quantization noise power is a negligible portion of the total noise power. Assigning 10% of the total noise power to the shaped in-band quantization noise, we find that a 5-bit quantizer is required for this structure.

Since the signal transfer function for this structure is ideally STF = 1, the output-referred noise power is the same as the input-referred one [10].

DISCUSSION AND CONCLUSION

The effects of thermal noise generated by the switches and op-amps devices in an SC circuit were analyzed. The analysis was simplified by assuming that the circuit contains only first order block (SC branches, feedback op-amps),. all designed to settle with half a clock period. This very practical assumption allowed a simple noise estimation process, resulting in a noise model consisting of input-and output-referred equivalent noise sources. The model was verified by comparing the estimation results for a typical SC integrator with those given by a state-of the art CAD program.

Based on the model, an optimum strategy was also suggested for the design of SC integrators incorporation thermal noise considerations.

Finally, an example illustrated the use of the proposed estimation process in the design of a second-order delta-sigma modulator.

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