HYBRID SYMMETRIC AND ASYMMETRIC CASCADED MULTILEVEL INVERTERS WITH MODIFIED PWM OPERATION

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Abstract— when asymmetrical inverter is operated in PWM mode it gives high value of total harmonic distortion (THD) which is mainly due to unequal pulses in the each stage of multilevel output. To avoid this hybrid asymmetrical inverter is proposed in this paper with asymmetrical and symmetrical parts. The main objective is to get the same THD value in asymmetrical inverter as same level symmetrical inverter when both are operated in PWM mode. Hybrid symmetrical inverter is proposed with modified PWM technique and it can be used in symmetric part of the hybrid asymmetric inverter.
Further in this paper a novel operation called as modified PWM operation is proposed for cascaded multilevel inverters in order to decrease high frequency switches in these inverters. This proposed inverter uses few levels at high frequency and remaining at low frequency. Henceforth this proposed PWM operation which uses more number of low frequency switches gives the same output as that obtained without using this modified PWM operation. This decreases the cost of the inverter and increases the reliability of the inverter.

Index Terms— Cascaded multilevel inverter, Hybrid asymmetrical inverter, Hybrid symmetrical inverter, Pulse width modulation, Total harmonic distortion.

I. INTRODUCTION

The Cascaded H-bridge multilevel inverters can be divided into two groups from the viewpoint of values of the dc voltage sources: the symmetric and the asymmetric topology. In the symmetric topology, the values of all of the dc voltage sources are equal. This characteristic gives the topology good modularity. However, the number of the switching devices rapidly increases by increasing the number of output voltage level. In order to increase the number of output voltage level, the values of the dc voltage sources are selected to be different, these topologies are called asymmetric [1]. The advantage of an asymmetric cascaded inverter is an increased voltage levels number for a given modules count. If the dc voltages of individual cells are arranged according to a geo metric progression with a common ratio of 2 [2], then the output voltage levels count grows with a modules number approximately as a power of 2. For converter cell dc voltages arranged as a geometric progression with a common ratio of 3, the levels count grows as a power of 3 of cells number. In spite of the above-mentioned advantages, this type of inverters has got some disadvantages. One is the unequal power generated by the existing dc sources. As a result, the life time of the sources applied in bridges would be different. Therefore, the number of checkups, substitution and battery changing time increases and as a result the maintenance cost of inverter increases too. In many industry applications it is often necessary to control the output voltage of asymmetrical inverters in order to cope with the variations of the dc input voltage, to regulate the voltage of inverters, and to satisfy the constant volts and frequency control requirement. Most efficient and heuristic method of controlling the output voltage is to incorporate pulse width modulation within the inverter [3] & [4]. By using PWM techniques the fundamental voltage of inverter as well as harmonics can be controlled.

II. PROPOSED CASCADED MULTILEVEL INVERTER

A new multilevel inverter topology is proposed by using series-connected submultilevel inverters. Fig. 1 shows the basic unit for a submultilevel converter [5] & [6].

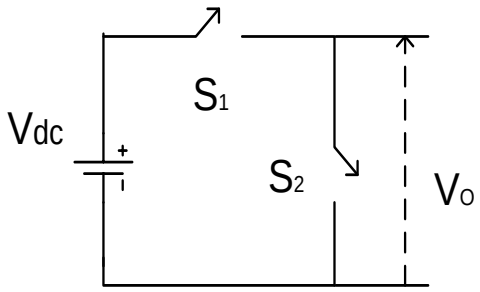


Fig. 1 Basic unit for a sub-multilevel converter

The proposed topology of inverter uses submultilevel inverter part and polarity creator part as shown in Fig. 2. The submultilevel converter gives either zero or positive output as shown in Fig. 3. When the proposed inverter operates as a symmetrical inverter, $V_i=V_{dc}$ where as in asymmetrical inverter V_i is equal to either $V_i = 2^{(i-1)}V_{dc}$ or 3^iV_{dc} where i=1, 2,⋯, n [7].

III. CONTROL STRATEGY

Control techniques used for the proposed symmetrical or asymmetrical inverter are based on fundamental frequency modulation and pulse width modulation techniques. Out of these techniques fundamental frequency operation is easy to control. To apply conventional PWM

techniques for the proposed topology it needs some modifications. Proposed PWM technique is derived from level shifted carrier PWM technique.

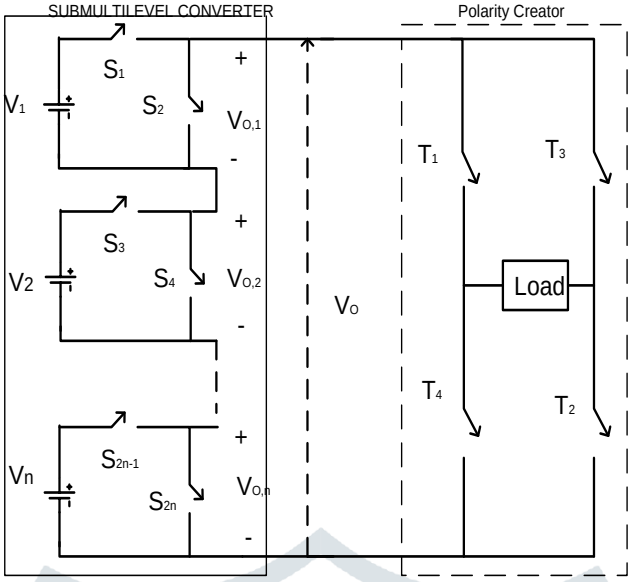


Fig. 2 The proposed topology for symmetric and asymmetric inverter.

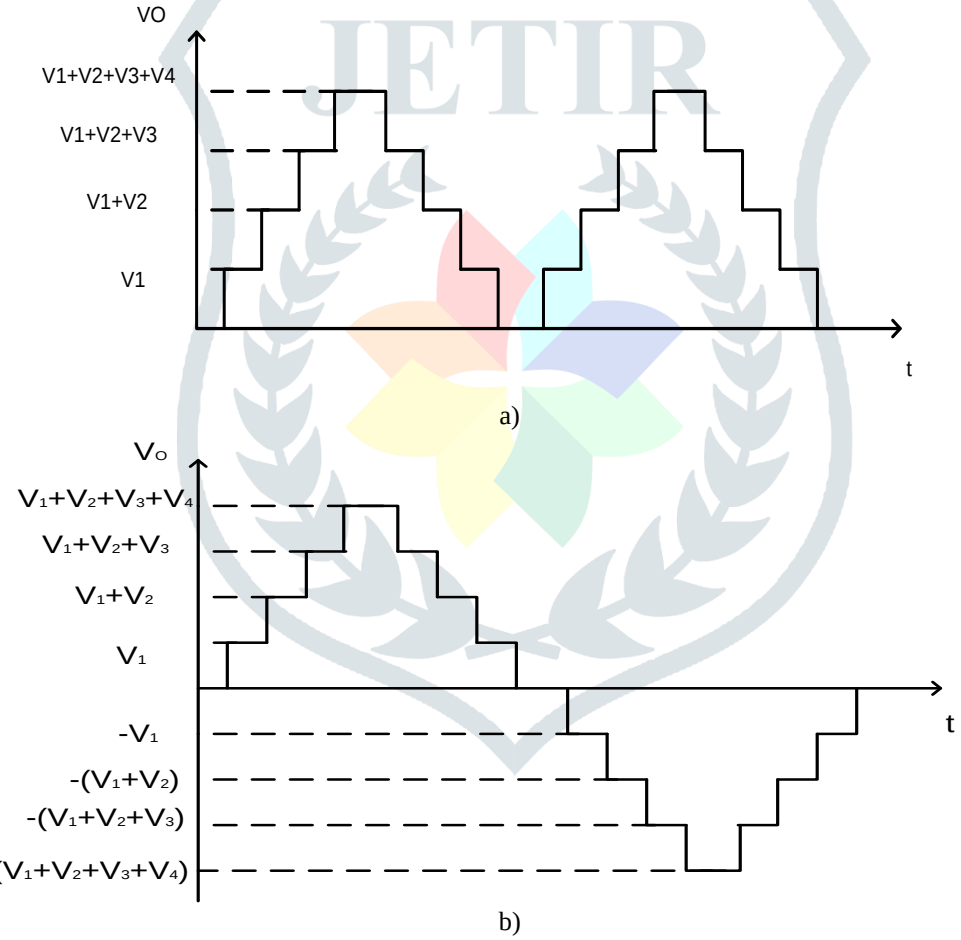


Fig. 3 a) Output of submultilevel converter b) Typical output waveform of nine level multilevel inverter

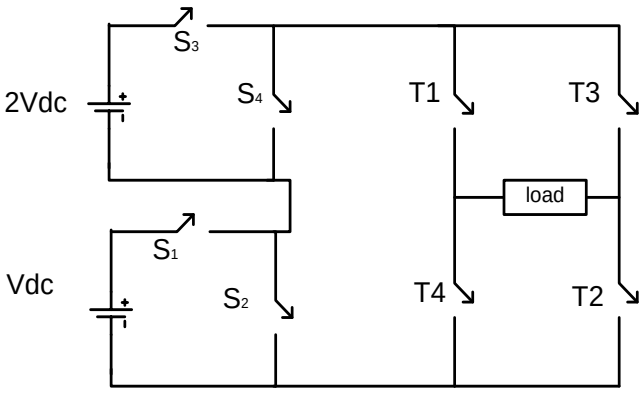


Fig. 4 seven level asymmetric inverter with proposed topology.

A) Fundamental Frequency Modulation

In this technique gate signals of inverter are derived in such a way to get all the levels in the output waveform. Here H-bridge is operated alike in symmetric topology to generate polarities of ac output. For seven level inverter control signals are given in the Fig. 4 and control signals are given in Fig. 5. $Ø_1$, $Ø_2$, and $Ø_3$ are calculated such that major harmonics in the output voltage waveform should be eliminated [8]. These values are called as optimum angles and these can be calculated by using control algorithms. Advantage of this technique is that it uses low switching frequency over the other control techniques. The main disadvantages are the presence of lower order harmonics in the output so the filtering cost increases and the inverter fundamental voltage cannot be controlled with variation in dc input.

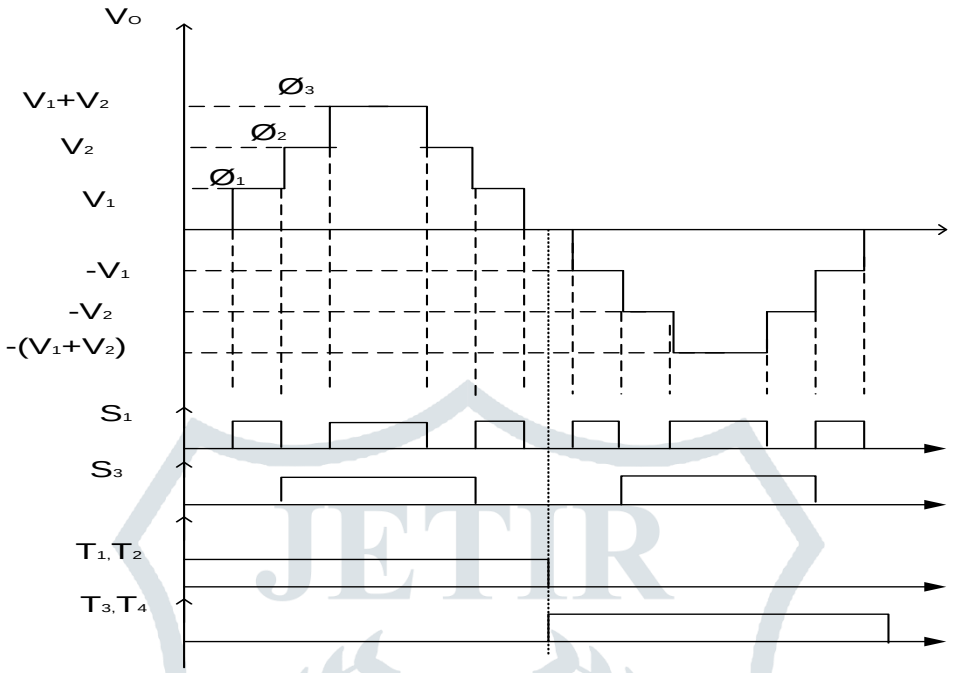


Fig. 5 Output of Seven level inverter with fundamental frequency operation

B) Pulse Width Modulation

For the given proposed asymmetric multilevel inverter special PWM techniques are required in order to get the controlled output. Since the same configuration is used for symmetrical and asymmetrical inverter, same PWM technique can be applied to the both the inverters. But here it is difficult to apply the gate signals directly to the asymmetric inverter which are derived from the comparison of the reference and carrier signals in the PWM operation. This is mainly due to the random distribution of turn on of the switches in the inverter in each half cycle. The proposed PWM technique shown in Fig. 6 gives the contiguous gate signals which are not suitable for the specific arrangement of turn on of the inverters in this asymmetric topology. By using logic circuits any PWM control signal can be modified in such a way that it is suitable for the specific arrangement of gate signals to turn on the switches in the inverter. For example for seven level asymmetric inverter PWM operation control signals are derived from the same level symmetric inverter PWM control signals.

Control signals for seven level asymmetrical inverter are fabricated by using following mathematical equations (1-3).

$$f(t) = \frac{(n-1)}{2} * ma * \sin(wt) \quad (1)$$

$$r(t) = |f(t)| \quad (2)$$

$$C1(t) = f(t);\ f(t) \geq 1 \quad (3)$$

Where,

f(t)	reference signal,
n	number of level, n=7,
m_a	modulation index (0-1.0),
r(t)	PWM reference signal,
$C_1(t)$	Multiplexing signal.

Three carrier signals are required above the zero reference and in general (n-1)/2 carrier signals are required where n is the number of levels. Multiplexing signals for obtaining given gate pattern varies with the number of levels. Here C1 is multiplexing signal and it is used to obtain the PWM gate signal for switch S1 with the help of logic circuit shown in Fig. 7. From the output of seven level inverter it is observed that fundamental component of output is more deviated from the approximate sine wave. This results in high value of THD and poor voltage quality. This is mainly due to the unequal pulses at each step of multilevel output when high voltage source is operated alone to obtain higher levels of the multilevel output. For example seven level hybrid asymmetric inverter output given in Fig. 8 shows that when higher voltage source operated alone in PWM mode it results $2V_1$ magnitude pulses in the second step of output and in the remaining two steps the pulse magnitude is V_1 since the same source gives the pulsed output in these steps. Thus this type of PWM operation results in more THD and poor output quality as compared to fundamental frequency modulation.

Even though if the number of levels are increased but inherently with asymmetric topology but with this type of PWM operation, output losses gets poor quality even the levels are increasing. Seven level asymmetric inverter results in a THD=28.97 % which is far away from the value 17.17% with fundamental frequency modulation and 17.93 % of its counterpart symmetric topology. Apart from this when high voltage source acts alone in the output, it causes high dv/dt across the switch which adversely effects the high frequency switches. The main advantage of asymmetric topology is that as the number of levels are increased per phase with the given number of sources as compared to symmetric topology, which results in better output quality. But during PWM operation of the asymmetric inverter, it losses the above advantage of the better quality output. To maintain its advantages during PWM mode operation a modified PWM technique is proposed.

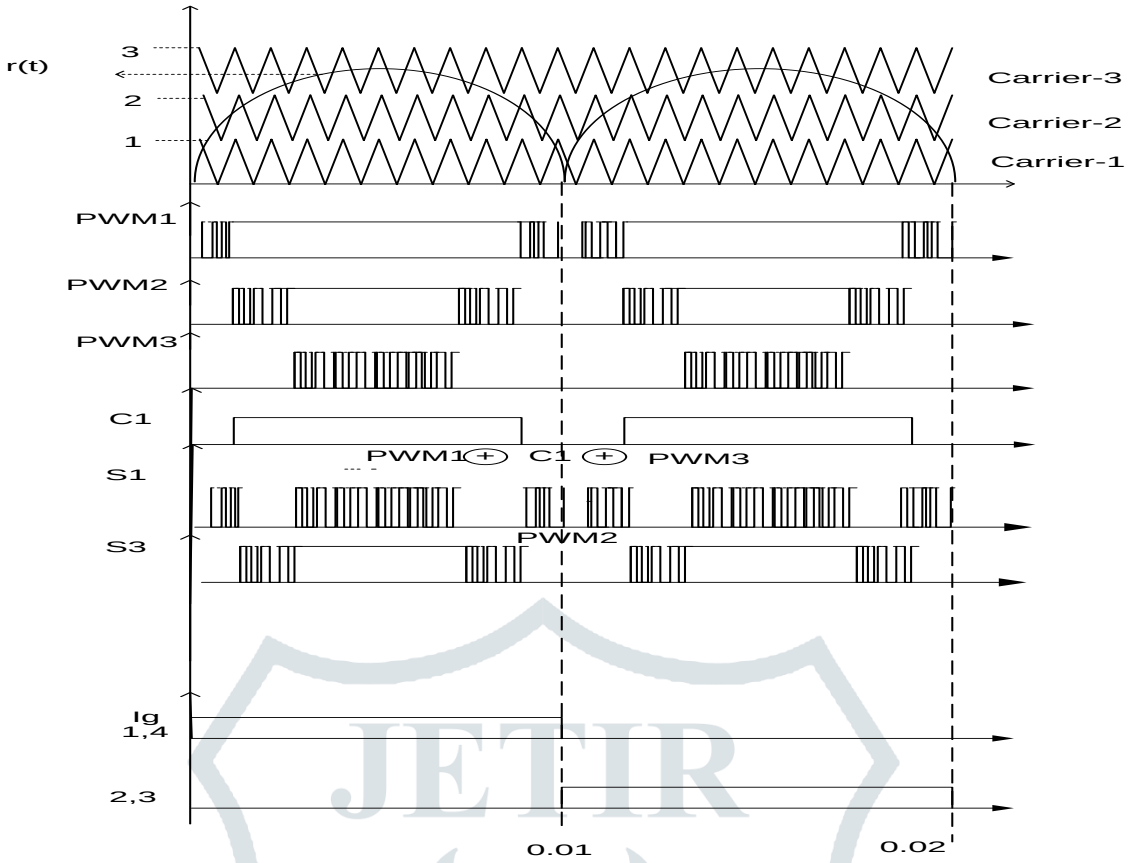


Fig. 6 Control signals for proposed seven level asymmetrical inverter

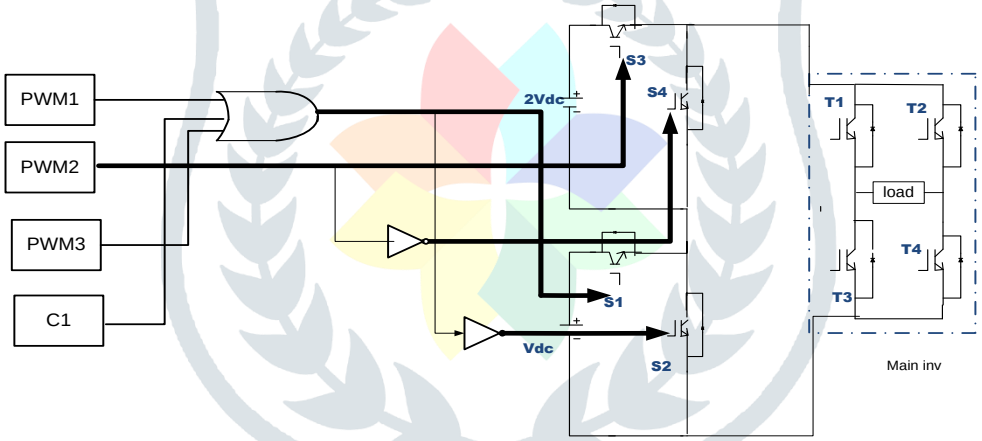


Fig. 7 Logic circuit for obtaining gate signals

Fig. 8 Output of seven level asymmetrical inverter with proposed PWM operation.

IV. PROPOSED HYBRID ASYMMETRICAL INVERTER

In the proposed hybrid inverter, the basic blocks have same rated source as that of the lowest rating source of asymmetric inverter. These are added in the submultilevel inverter of asymmetrical inverter as shown in Fig. 9. The basic blocks are grouped and named as symmetric part and the remaining blocks are called as asymmetric part.

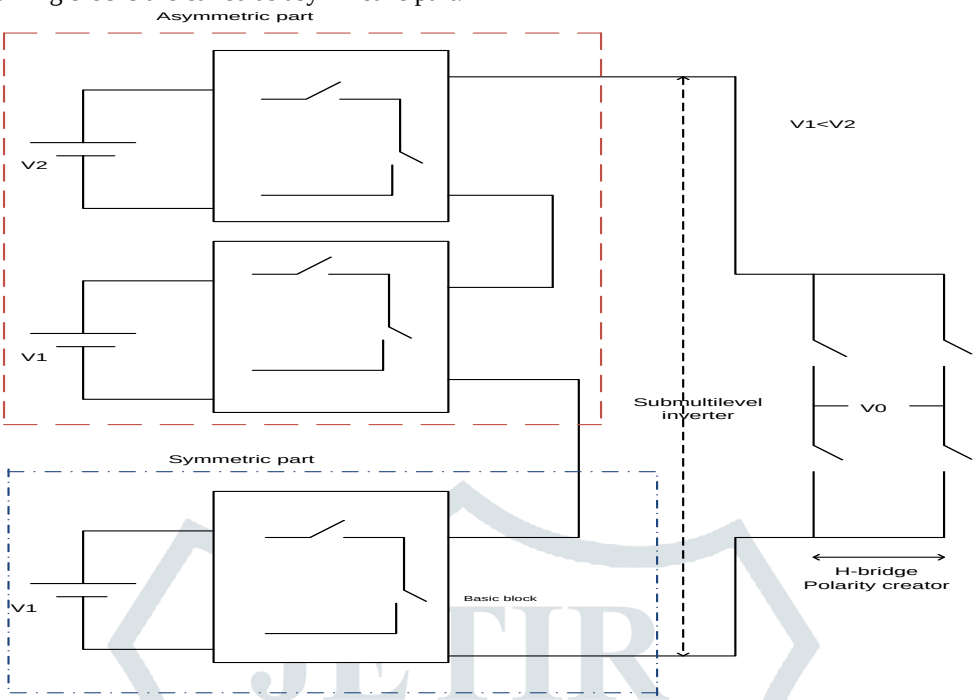


Fig. 9 Proposed hybrid asymmetrical inverter.

To eliminate the unequal pulses in the output of asymmetrical inverter, high voltage sources in the inverter should not give pulsed output when they are operated alone. Instead of operating an asymmetric part in the PWM mode, symmetric part of the hybrid inverter is operated in PWM mode. Since symmetric part of the inverter uses same rating sources, the pulses in the multilevel output are equal. Asymmetric part of the inverter is operated in square wave mode and it gives square wave type output. Finally asymmetric part is used for level creation and symmetric part is used for equal pulses in each step. Thus the multilevel output is better controlled and gives less THD which is equal to the same level of symmetric topology.

By adding the symmetric part to the asymmetric inverter, the number of levels increased in the output of given asymmetric inverter. Number of output voltage levels possible with the proposed hybrid asymmetrical inverter are given by equation (4) and number of IGBTs are given in the equation (5).

$$N_{level} = (2^{(n+1)} - 1) + 2m \quad (4)$$

$$N_{IGBT} = 2(n+m) + 4 \quad (5)$$

Where n is the number of basic blocks of asymmetric part and m is the number of basic blocks of symmetric part.

Possible levels with this type of inverter are 3, 5, 7, 9, 11, 13, 15, 17, 19, and …. for different values of n and m combinations where n, m are positive integers. So with this hybrid configuration all odd levels are possible which was not possible with the proposed asymmetric inverter. Number of basic blocks in the symmetric part depends upon the required level output which is not possible with asymmetric inverter alone. For example nine and eleven level output is not possible with the proposed asymmetric inverter to get these levels with hybrid asymmetric inverter n=2 is used in both the inverters but m=1 and m=2 are the number of basic blocks used in symmetric part of the two inverters respectively.

Since symmetric part is operating at high frequency, the dv/dt during switching is low as compared to that of the asymmetric inverter [9].

Nine level inverter is formed with one basic block in symmetric part and two blocks in asymmetric part as shown in Fig. 10. In asymmetric part the values of voltage sources are V_1=50 V and V_2=100 V. Since V_1 is the lowest rating of voltage source, same value of voltage source should be connected in symmetric part.

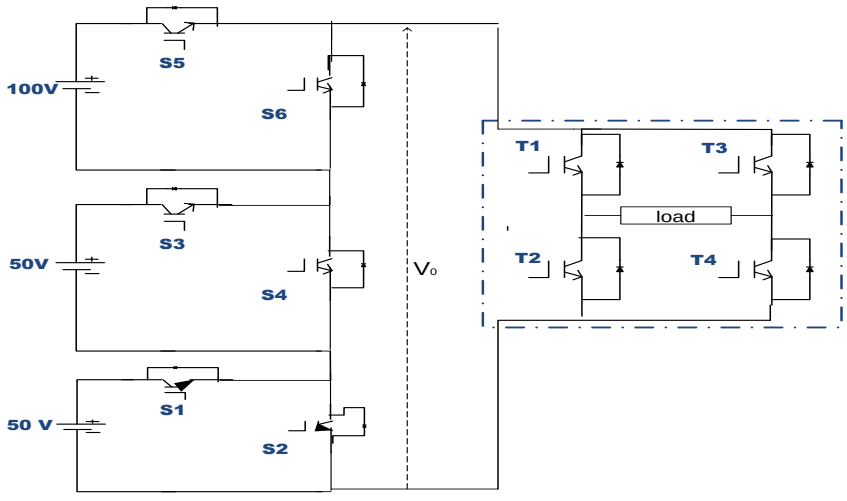


Fig. 10 Nine level hybrid asymmetrical inverter

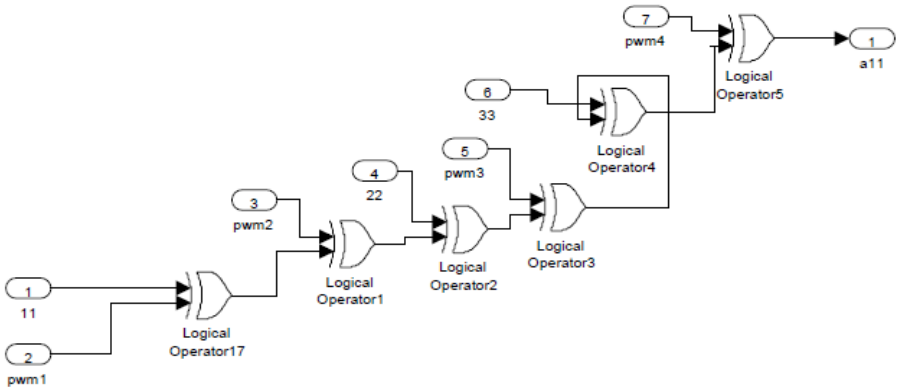


Fig. 11 Logic circuit for symmetric part

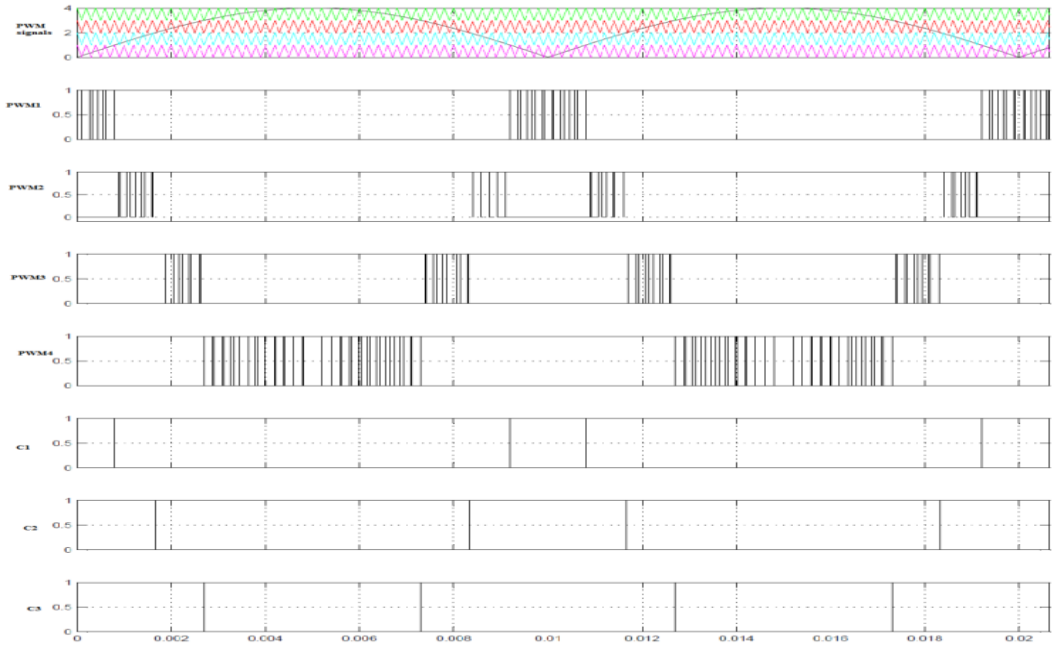
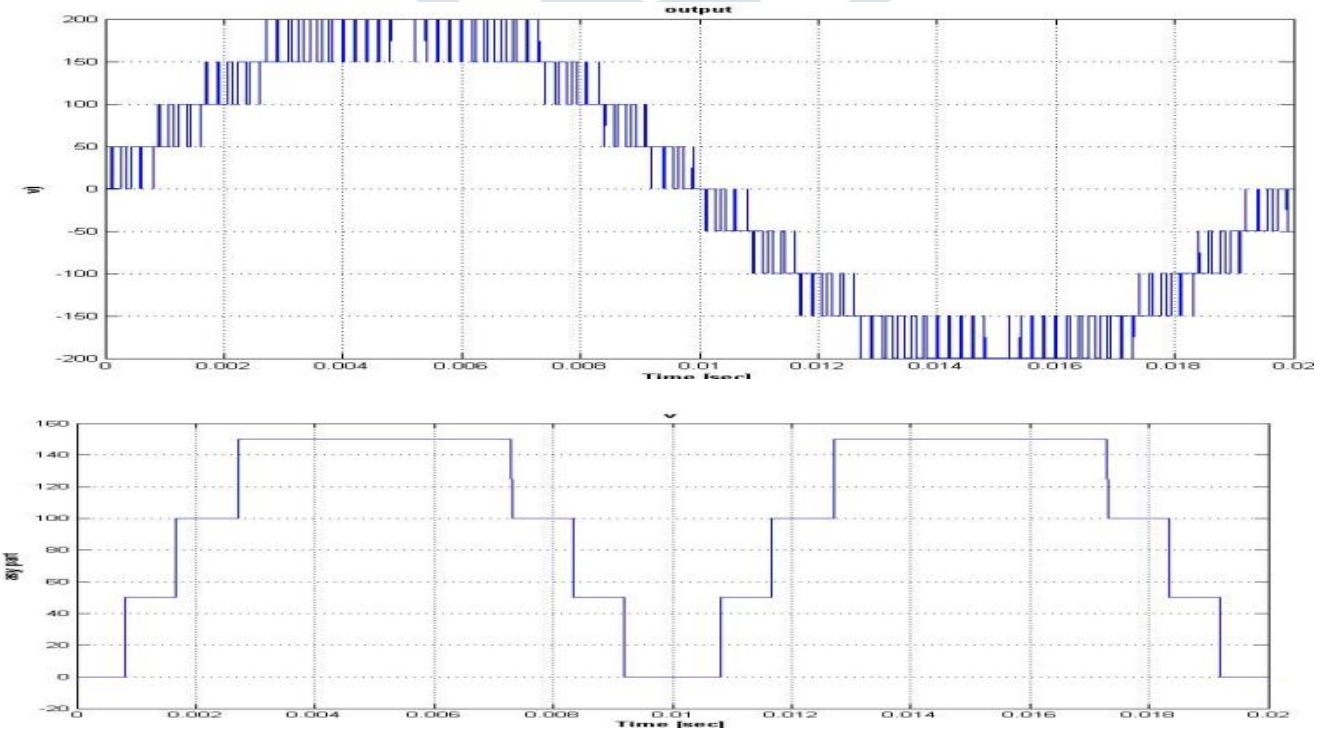


Fig. 12 Control signals of level shifted PWM technique and multiplex signals

Logic circuits are used for the generation of gate pulses for symmetric part and asymmetric part. Symmetric part logic circuit is shown in Fig. 11 and by using multiplex signals shown in Fig. 12. Asymmetrical part gate signals are similar to gate signals of seven level inverter shown in Fig. 5. Simulation output of nine level hybrid symmetrical inverter is shown in Fig. 13.



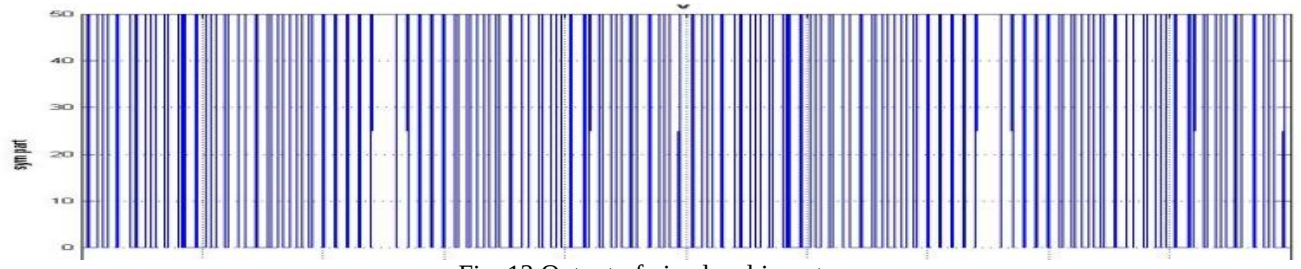


Fig. 13 Output of nine level inverter.

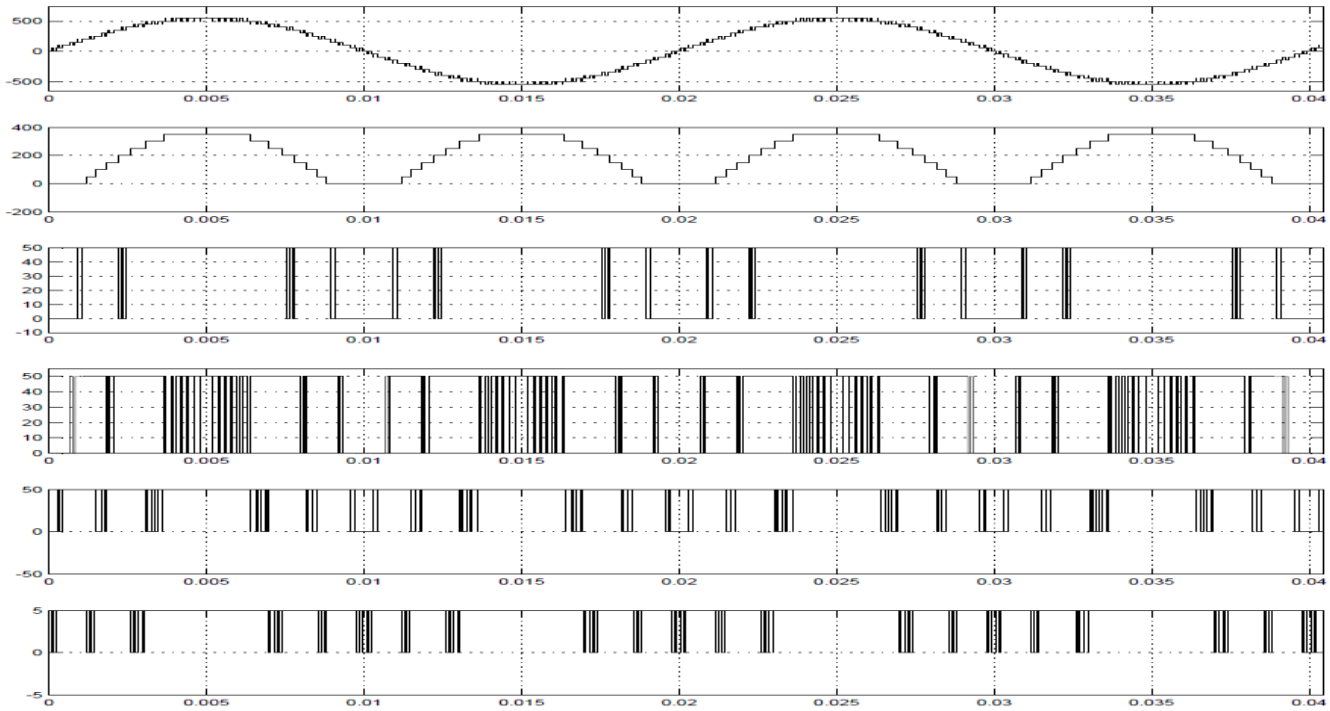


Fig. 14 Simulation output of twenty three level hybrid asymmetrical inverter.

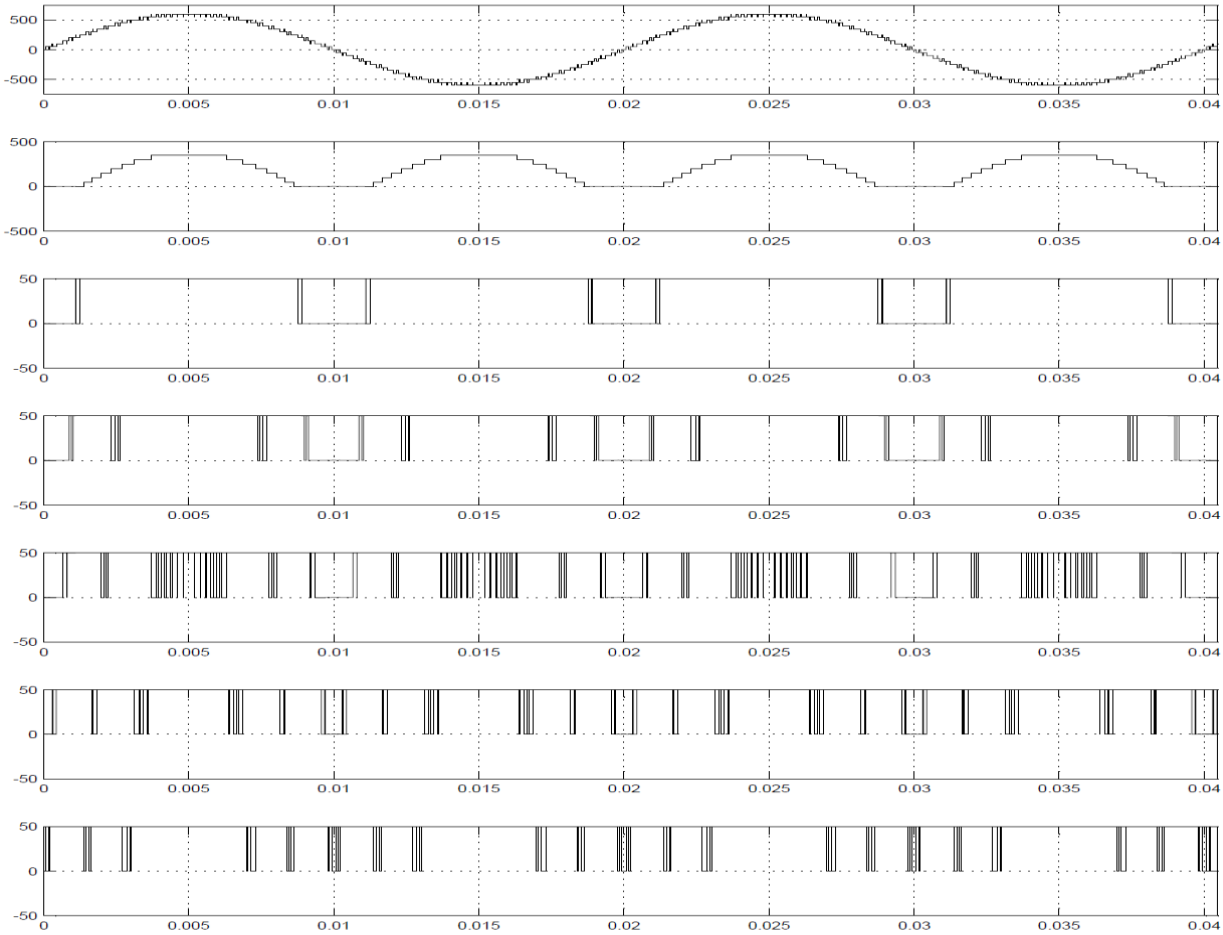


Fig. 15 Simulation output of twenty five level hybrid asymmetrical inverter.

Twenty three level inverter can be formed by using five cells in symmetric part and three cells in asymmetric part i.e n=3, m=4. In simulation model 50 V sources are used in symmetric part and 50 V, 100 V, and 200 V sources in asymmetric part. Simulation output is shown in Fig. 14.

Twenty five level inverter can be formed by using five cells in symmetric part and three cells in asymmetric part i.e n=3, m=5. In simulation model 50 V sources are used in symmetric part and 50 V, 100 V, and 200 V sources in asymmetric part. Simulation output is shown in Fig. 15. The proposed hybrid asymmetrical and symmetrical inverter gives same THD when they are operated in PWM mode for the same level output. For example ninelevel symmetrical and hybrid asymmetrical inverter gives the same THD i.e 13.78%.

V. PROPOSED HYBRID SYMMETRICAL INVERTER

For the given type symmetrical inverter several hybrid connections are possible. One of the proposed hybrid symmetrical inverter is shown in Fig. 16.

In this topology one dc source is directly used without any switches and one H-bridge in submultilevel inverter part of the proposed symmetrical topology. This type of configuration allows only symmetrical connection where as asymmetrical inverter is not possible. But it can be used in symmetrical part of the proposed hybrid asymmetrical inverter.

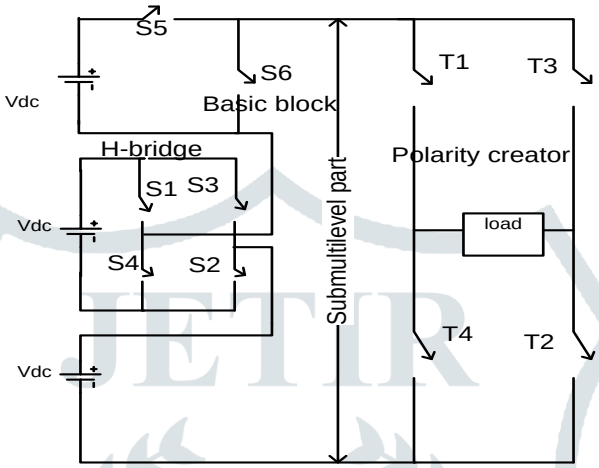


Fig. 16 Proposed hybrid symmetrical inverter

To reduce the switching losses in the inverter, above explained PWM technique is modified. Control signals are derived by using equations (6) and (7) and are shown in Fig. 17.

$$f(t) = m_a \mathrm{Sin}(\omega t) \quad (6)$$

$$r(t) = \begin{cases} \left(\frac{f(t)}{\sin\left(\frac{\pi}{2*(n-2)}\right)} - 1\right) & ; \sin\left(\frac{\pi}{2*(n-2)}\right) \le |f(t)| \le 1 \\ \left(1 - \frac{f(t)}{\sin\left(\frac{\pi}{2*(n-2)}\right)}\right) & ; 0 \le |f(t)| \le \sin\left(\frac{\pi}{2*(n-2)}\right) \end{cases} \quad (7)$$

$$a_2 = \begin{cases} 1; |f(t)| \ge \sin\left(\frac{\pi}{2*(n-2)}\right) \\ 0; |f(t)| < \sin\left(\frac{\pi}{2*(n-2)}\right) \end{cases} \quad (8)$$

Where,

f(t) reference signal,
N number of levels,
m_a modulation index (0-1.0),
r(t) PWM reference signal.

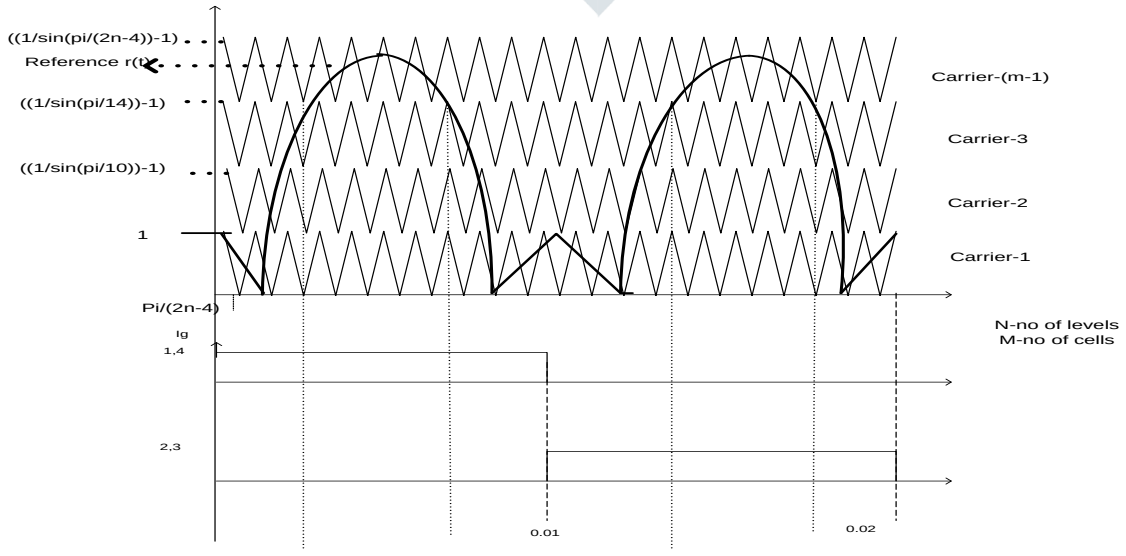


Fig. 17 Control signals of modified PWM technique

The modified PWM technique can be used for the better control of proposed topology and the logic circuit is used for the gate pulses of the positive and negative switches in the H-bridge of submultilevel part which is shown in Fig. 18 where A2 is the multiplex signal as given in equation 8.

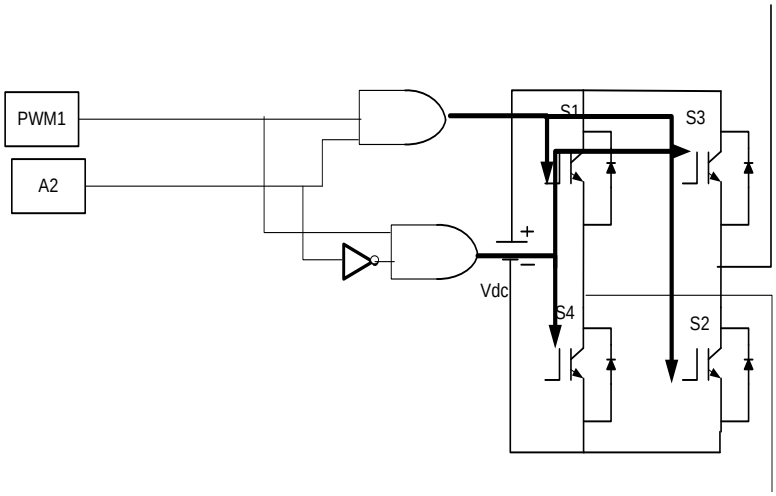


Fig. 18 Logic circuit of H-bridge in submultilevel part

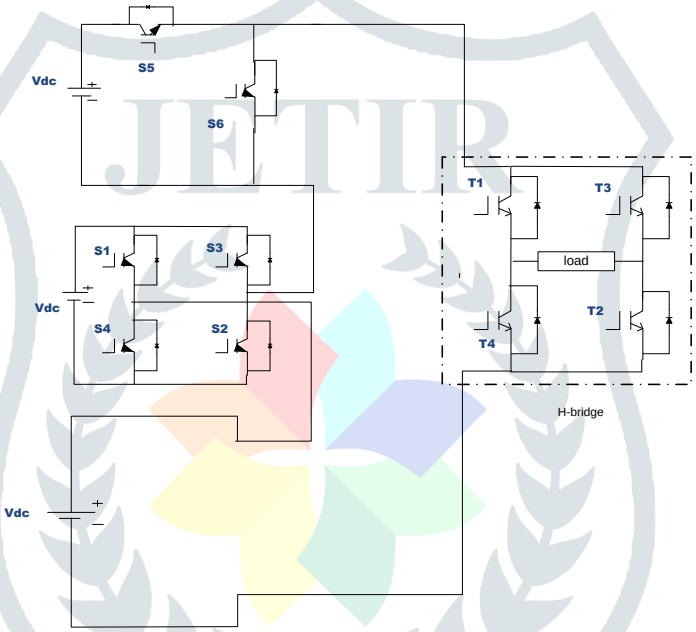


Fig. 19 Seven level hybrid symmetrical inverter.

seven level hybrid symmetrical inverter is shown in Fig. 19 where as simulation output is shown in Fig. 20. When this hybrid inverter is used in symmetric part of the hybrid asymmetric topology the results are shown in Fig. 21 and Fig. 22.

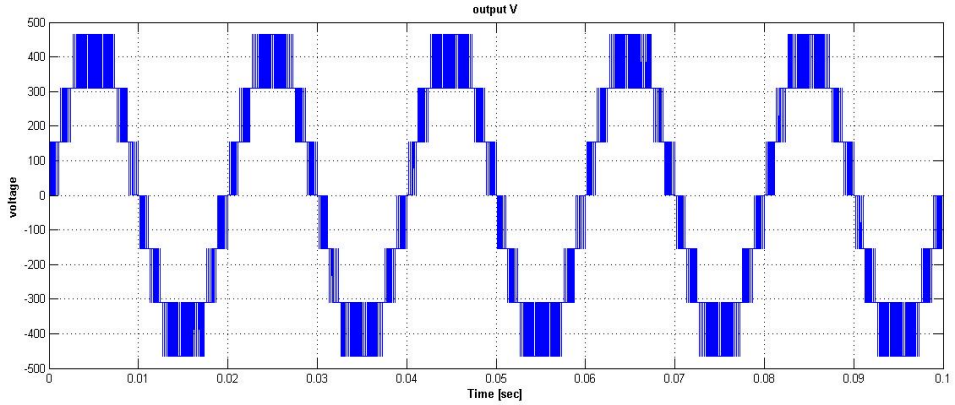


Fig. 20 Simulation output of seven level hybrid symmetric inverter.

VI. MODIFIED PWM OPERATION

From the proposed hybrid asymmetrical inverter it is observed that for getting satisfactory output in PWM mode some of the levels are operated at high frequency and some of the levels are operated at low frequency. Same type of operation can be possible in any type of cascaded multilevel inverters to decrease high frequency switches in these inverters without change in the output quality. This is one alternative to decrease the cost of the inverter and to increase reliability of the inverter since high frequency switches decrease in the current path of the inverter.

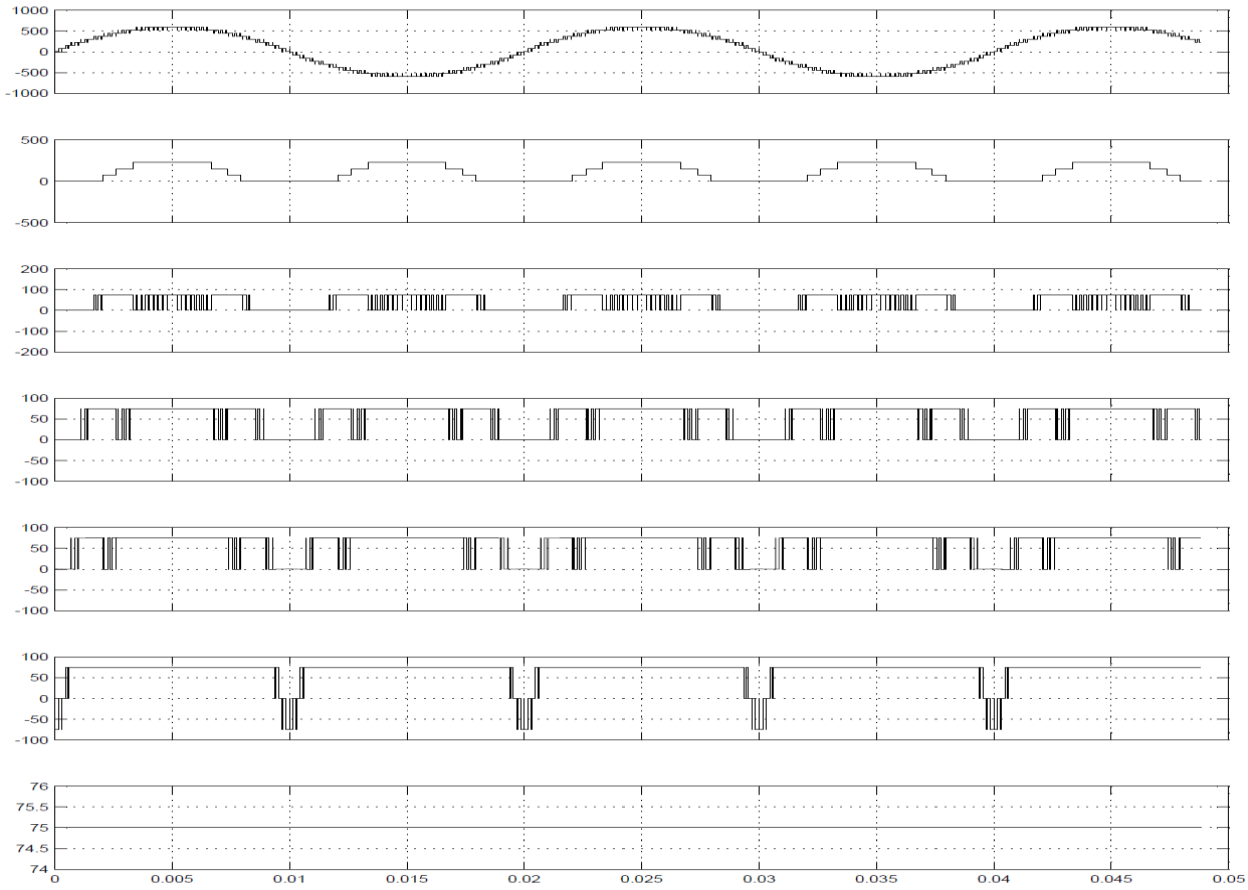


Fig. 21 Output of seventeen level hybrid asymmetrical inverter

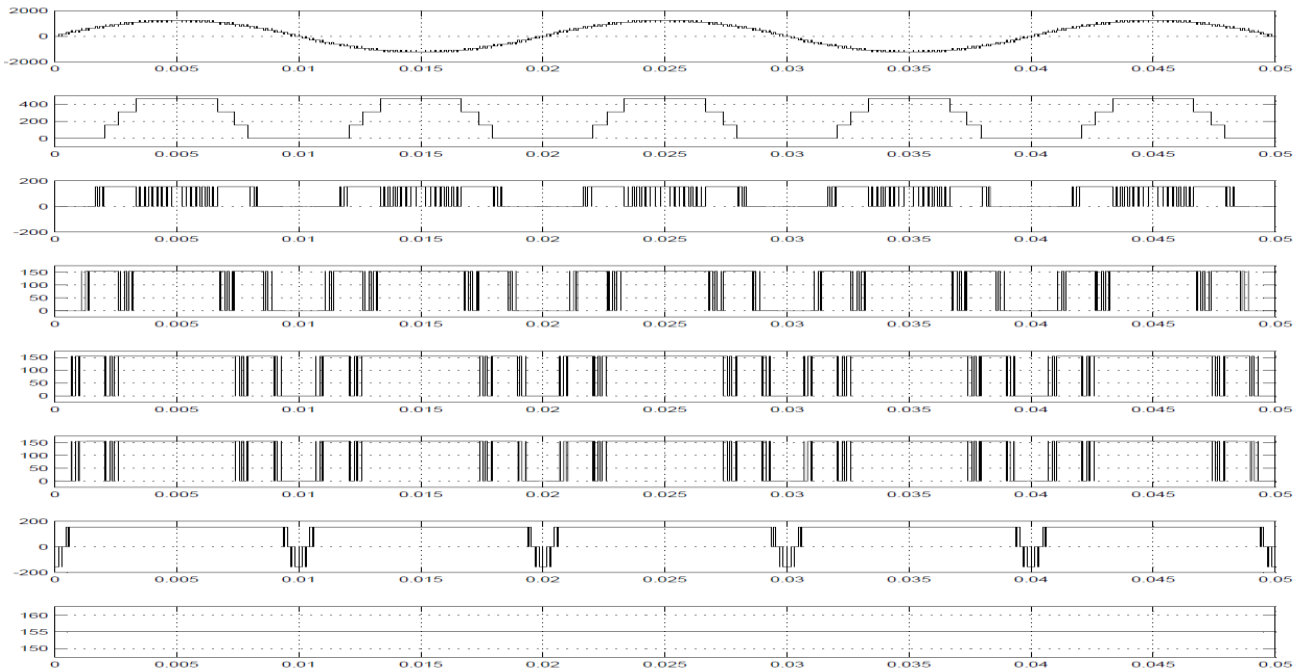


Fig. 22 Output of twenty one level hybrid asymmetrical inverter

VII. CONCLUSION

In this paper a new multilevel inverter topology is proposed by using series-connected submultilevel inverters. The proposed multilevel inverter uses reduced number of switches. Same topology can be used as symmetric and asymmetric inverter. Modified PWM techniques are proposed for the better control of both the topologies and these are derived from level shifted PWM technique. Without increasing basic blocks in the symmetric topology for more levels in the output asymmetric topology is proposed with different dc sources.

Fundamental frequency control is easy to apply in asymmetric topology. But PWM operation gives more THD and poor output quality. When asymmetrical inverter operated in PWM mode to improve output quality hybrid asymmetrical inverter is proposed this gives the same value of THD as symmetrical topology. From the PWM operation of hybrid asymmetrical inverter modified PWM operation is proposed for any type of inverter with some of the levels operating at PWM mode and remaining at square wave mode. Hybrid symmetrical inverter is proposed and this is controlled by modified PWM technique. Matlab/Simulink models are used for the study of all proposed inverters. Since the proposed symmetrical and asymmetrical topology has more advantages over other topologies these can be used in Wind-PV hybrid generating systems.

REFERENCES

[1] Mohammad Farhadi Kangarlu and Ebrahim Babaei, "A generalized cascaded multilevel inverter using series connection of submultilevel inverters", IEEE Trans. on Power Electronics, vol. 28, no. 2, Feb. 2013.

[2] Alex Ruderman and Sam Schlosberg, "A hybrid asymmetric cascaded multilevel inverter comprising high resolution and symmetric low resolution parts", IEEE 25th Convention of Electrical and Electronics Engineers in Israel (IEEEI- 2008), pp. 21-25, 3-5 Dec. 2008.

[3] Ebrahim Babaei and Mohammad Sadegh Moeinian, "Asymmetric cascaded multilevel inverter with charge balance control of a low resolution symmetric subsystem", Elsevier Journal of Energy Conversion and Management, vol. 51, pp. 2272–2278, Nov. 2010.

[4] Khomfoi and L. M. Tolbert, Multilevel power converters Power Electronics Handbook, 2nd Edition Elsevier, 2007.

[5] Ebrahim Babaei and Seyed Hossein Hosseini, "New multilevel converter topology with minimum number of gate driver circuits", International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), pp. 792-797, 2008.

[6] Ebrahim Babaei, Mohammad Farhadi Kangarlu, and Farshid Najaty Mazgar, "Symmetric and asymmetric multilevel inverter topologies with reduced switching devices", Elsevier Journal of Electric Power Systems Research, pp. 122– 130, 2012.

[7] Ebrahim Babaei and Seyed Hossein Hosseini, "New cascaded multilevel inverter topology with minimum number of switches", Elsevier Journal of Energy Conversion and Management, vol.50, pp. 2761–2767, Nov. 2009.

[8] N. Mohan and T. M Undeland, Power electronics-converters, applications and design, 3rd Edition, John Wiley & Sons, New York, 2003. A Rufer, M Veenstra, and A Gopakumar, "Asymmetric multilevel converter for high resolution voltage phasor generation", EPE 99, Lausanne, 1999.