Router1x3 Protocol design with virtual cut through Mechanism for Network on Chip (NoC)

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Abstract : ***System on Chip (SoC) allows million of transistors to be integrated on single chip. Traditional SoC has bus based architecture for communication which limits the processing speed. Now a day's in Silicon industries there is emerging concept of Network on Chip (NoC) to decouple communication from computations. Router is a backbone of NoC, hence efficient design of router is essential to enhance the performance of the system. In present work, we focus on a router input-output protocol design. Proposed system includes virtual cut through mechanism for close loop communication. Router 1x3 has single input port and three output ports. Top-level architecture designed with sub-modules like FIFO, FSM, Synchronizer and Register using Verilog language. Routers RTL design analyzed and verified using Xilinx 14.5 Spartan-3E- xc3s100e FPGA family. Simulation of RTL design carried on ISim simulator. Code coverage observed on Questasim. Power utilization observed on XPower, it is 80mW.***

Index Terms - Network on Chip (NoC), Router, FIFO, FSM, Synchronizer, Register, Verilog.

I. INTRODUCTION

Network on Chip is a concept in SoC which replace bus based architecture with router based architecture in communication of IP cores. Moore's law states that number of transistors on single chip doubles after every 18 months. Hence In silicon industries it is observed that more than million of transistors are integrating over single chip but due to common bus based architecture, processing speed of system degrades and leads to sluggish performance. NoC allows decoupling of communication from computation which leads to improve performance of the system.

NoC contains three building blocks like Link, Router and Network Interfaces out of which Links are actual connections between IP cores, Routers are intelligent elements decides rules and policies for data transmission while Network interfaces are logical connections between IP cores.

The remainder of this paper starts with discussion of Related Work in Section-II. Network topologies described under Section-III. Router-Characteristics in NoC described in Section-IV. Input-output protocol described under section V. Section-VI describes proposed system for router. Section-VII includes Simulation results and protocol waveforms. We concluded this research work with analysis of design under Section-VIII.

II. RELATED WORK

In 2004, NoC is proposed as a future of ASIC [1]. In 2008, Survey paper on Network on Chip proposals has been published, paper focus on NoC evolution methods and actual implementation of router for NoC along with efficient design [2]. Router defines set of policies acts active part of NoC among all some policies listed here like Flow control for data, Switching mechanism for data, Buffering Policy used to store data before transmission to avoid congestion in the network [3].In 2014, Router designed with FSM controller and published as a special issue in international conference [4]. In 2015, different router architectures proposed for router design [5,6]. In 2016, high performance reliable NoC router designed and verified to tolerate any fault in the system [7,8]. There is one article published by Arteris, there is summarized that NoC based architecture for communication has better performance comparatively that of bus based architecture [9]. Research on router design is ongoing at industry as well as academic levels in different countries but every design has some pros and cons hence efficient router design is most important to have better performance of the system.

III. NETWORK TOPOLOGY

Network topology defines how different nodes are connected with each other. The way of connection between different nodes affects latency and bandwidth in communication. There are different topologies for IP core connection like Mesh topology, Tree topology, torus, octagon etc shown in below figures. The most commonly used topology to connect IP core is 2-D Mesh topology. Mesh topology allows parallel communication. In tree topology single source node can communicate with multiple destination nodes. In proposed system router1x3 designed which is in the form of tree topology having single input source node and three output ports.

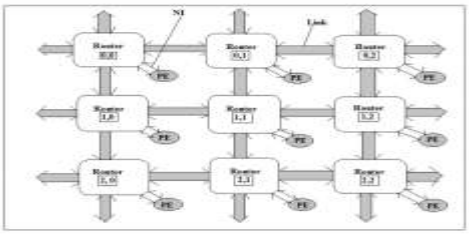

Fig.1 3x3 Mesh topology [4]

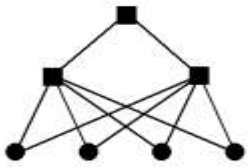

Fig.2 Fat Tree Network [3]

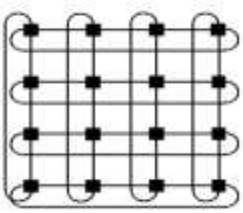

Fig.3 Torus Network [3]

Some researchers have proposed application specific topology that can offer superior performance while minimizing area and energy consumption.[5]. In present work, we considered tree topology for serial communication between single source node with multiple destination nodes.

IV. ROUTER CHARACTERISTIC IN NOC

NoC contains basic building blocks like Links, Router and Network Interfaces. Links provide physical connection between IP cores in NoC while Network Interfaces provides logical connection between connecting nodes. Router in NoC defines overall strategy for data transmission .NoC has some characteristics as Flow control, Routing, Switching, Buffering etc [3]. All characteristics are mentioned as below. These characteristics ensure successful transmission of data from source node to destination node.

1. Flow control- This policy is characterized by movement of packet along with NoC. To avoid congestion and dead locking in the Network, there are two type centralized flow control and distributed flow control. Centralized approach uses Time Division Multiplexing mechanism while distributed control system uses Virtual Channel mechanism.
2. Routing Algorithm- This policy is characterized by path for packet movement. Routing algorithm is a logic that decides destination port by looking at address mentioned in header of the packet. Deterministic routing algorithm follows fixed path to move packet towards destination. Adaptive algorithm has alternative path selection after getting congestion on any one of the path. Dynamic routing algorithm provides run-time path. Minimal routing algorithm provides shortest path towards destination.
3. Switching- It defines how data is to be transmitted from source node to destination node. Mainly there are two types of switching techniques Circuit switching and Packet switching. In Circuit switching, whole path from source to destination is previously established and reserved for transmission. In Packet switching, data transmitted in the form of packets having width 8 bit and length 1 to 63 bytes. First byte is header, according to header data passed to respective destination node. In packet switching there are three strategies Store and forward strategy, Wormhole strategy and Virtual cut through mechanism [3]. In Store and forward strategy, node stores complete packet before transmit it to target. On other hand in Wormhole strategy, node takes routing decision and forward data to target as soon as header arrives. Virtual cut through mechanism is better than of Wormhole since it reduces chances of packet stalling by taking confirmation from target about acceptance of packet.
4. Buffering- This policy is characterized by traffic control in NoC. The buffering strategy has important impact on network traffic. It affects the performance of NoC. There are two approaches for buffering like Centralized buffer and Distributed buffer. In Centralized approach, one single buffer can be shared with all output ports. In distributed approach, each output port has its own buffer element. Generally FIFO is buffering element used for storing data.

V. ROUTER INPUT-OUTPUT PROTOCOL

Router input and output protocol sets rules on movement of packets through NoC..

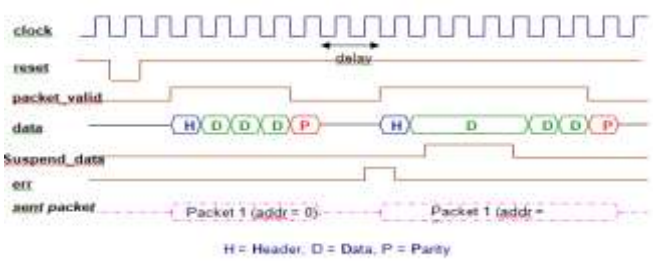

Fig.4 Router Input Protocol [8]

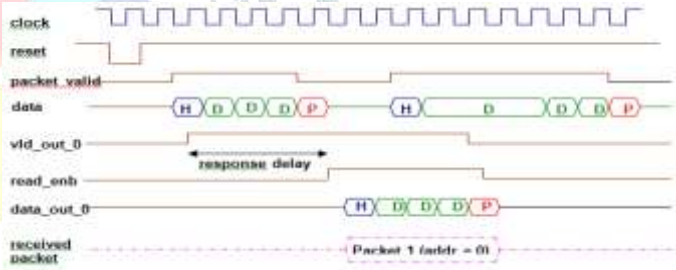

Fig.5 Router Output Protocol [8]

Router is a synchronous type protocol. Fig.4 shows input protocol for router in which active low reset signal is used. When router receive data packet along with packet valid signal from source node, first byte it takes as a header. After that all data packets received as an actual payload on each negative edge of the clock. After receiving last byte of packet it generates error signal. When router observe FIFO full state it sends suspend_data signal back to source node , hence for few clock cycle it will hold that last received data. In Input protocol, router receives data packets successfully [8].

Fig.5 describes Router output protocol, which sets rule for data transmission to respective node. Already received data packets are routed to target node by router output protocol. It will check validity of packets. After getting valid status of data, it will wait for read enable from that target node. Data transmitted to the target node only after getting read enable signal [8].

In proposed protocol design, we used acknowledgement signal which acts as a feedback in communication. Along with this we have implemented internal soft reset facility.

VI. PROPOSED SYSTEM

As mentioned in Section IV, Router in NoC is characterized by different strategies. In present work we focus on design and implementation on router input-output protocol with characteristics 1. Deterministic routing 2.Virtual cut through packet switching 3.Distributed buffering. Purpose of this architecture design is to avoid loss of data in NoC. By including such type of characteristics in router design we tried to achieve control over traffic in NoC.

Fig.6 describes about block diagram of Router top-level architecture. On every positive edge of clock data is received by source node. Reset is an active low signal. Packet valid signal is asserted by source node indicating validity of the packet. There are three read enable input signals from each respective output port. Three valid out signals indicate validity of received data. Busy signal is for acknowledgement to source node. Error signal is for privacy concern indicates corrupted data by using parity check logic

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Top level Architecture for router contains 4 sub modules like FSM, FIFO, Synchronizer and Register.Fig.7 shows RTL view of router 1x3 design. It contains sub modules which are briefly described as below-

Fig.6 shows Block diagram for Router1x3 and Fig.7 Shows top level RTL view generated on Xilinx 14.5 IDE.

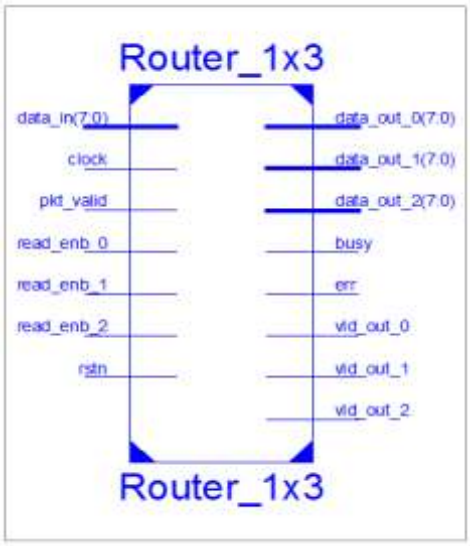


Fig.6 Block diagram for Router1x3

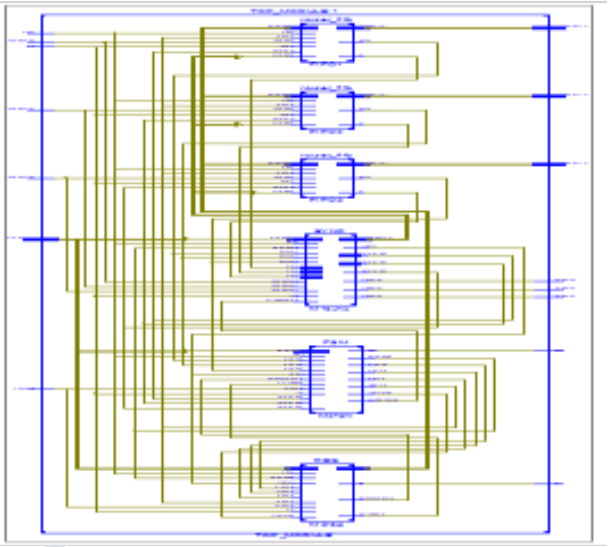


Fig.7 RTL view of Router 1x3 Top level Architecture

1. FSM- It is signal generator type FSM, acts as a monitoring as well controlling element of the router. It can be called as controller of router architecture. Moore's type of FSM is used in the design. There are two logic loops designed for FSM, 1st loop Starts from Idle state, whenever FSM receives packet valid signal, it looks first byte of packet as a header and assert signal Detect_address. Next state is load first data it generates signal lfd_state high indicating that header is accepted by router. After that it goes to accept actual payload by generating signal ld_state high. Next state is parity checking in which FSM receives parity done signal from register module and concludes last byte of data received. 2nd loop starts with Idle state , in which it receives first byte of packet and asserts Detect_address indicating that header is received . In next state it accepts actual payload same as before and if it observe fifo_full status, it directly jumps on fifo_full state in which it asserts signal full_state indicating that any one of the FIFO is full and have to wait till getting empty.

There router will hold last available packet byte till FIFO gets empty and after that starts receiving of new packets asserting signal laf_state means load after full state.

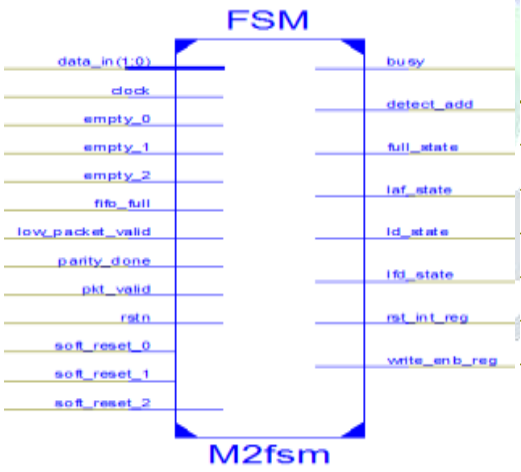


Fig.8 Sub module- FSM

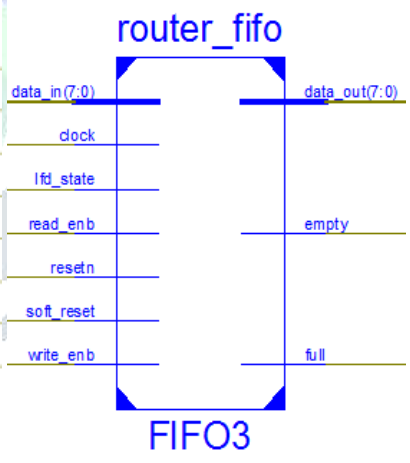


Fig.9 Sub module- FIFO

We have introduced Virtual cut through mechanism by using "busy" control signal of FSM controller. Busy is output signal from router to source node. It gives acknowledgement to the source node about status of the target node. After receiving packet valid signal and valid data from source node, FSM asserts busy signal. Data transmitted to the target node only when busy signal goes to low. Again busy signal goes to high whenever it monitors last parity byte of packet is received by router. This acknowledgement indicates close loop communication.

2. FIFO- It is buffering element that stores packets before actual transmission to the respective target node. In present work we have used distributed type of buffering system means each output port has its own buffer. Since it is Router1x3 architecture, there are 3 buffering FIFO used with depth 16byte and width 8 bit. Logic for FIFO module based on read and write signal. Whenever it receives write enable signal from synchronizer module, data stored in the FIFO by using write pointer. At receiving read enable signal, data is read out from memory location indicated by read pointer.

There are two status signals FIFO Full and Empty.Empty indicates that FIFO is ready to receive data while Full indicates there is no space to write data in FIFO.

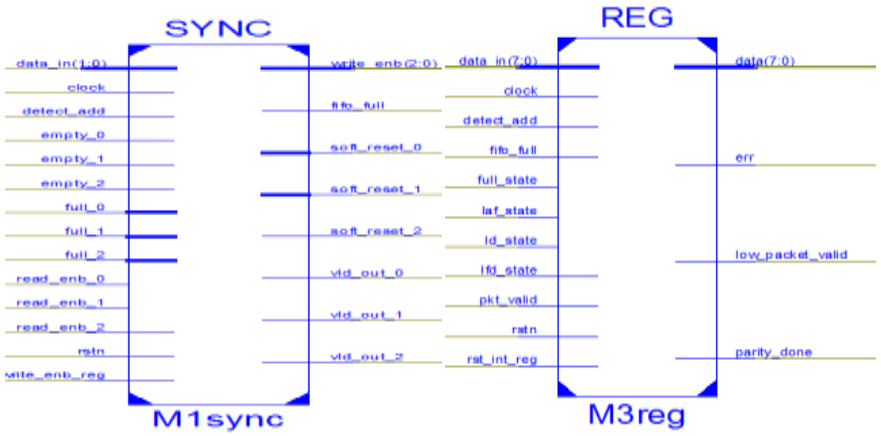


Fig.10 Sub module- Synchronizer Fig.11 Sub module- Register

1. Synchronizer- This sub module has logic for checking validity of data packets and generating soft reset signal. Validity of packet is decided based on FIFO condition. When FIFO empty status observed to be high, it will generate Valid_out signal for data transmission. Synchronizer is designed with Soft Reset Logic
   Logic determined as, after assertion of valid_out signal, module waits for 10 clock cycles for receiving read enable signal from target node. If it does not receive read enable within that period, Soft reset signal asserted to be high. This soft reset signal further used by FIFO modules to internally reset buffer. By integrating full status from all FIFO, module generates one single FIFO-full signal to inform FSM about full status of FIFO hence Synchronization is main purpose of this module. It also provides write enable signal to FIFO.

2. Register- This sub module has internal register that divides data packets as header, payload and parity. It checks signals from FSM controller and accordingly identifies address of the destination. Example, if register receives input data along with detect-add and lfd_state high, it considers that incoming data is header. If it receives input data with ld_state high , it considers that incoming data is actual payload. If it observes full_state and fifo_full high, it stores data in the internal register. Whenever it observes laf_state high, it starts sending newly received data to the output.

These all sub modules are internally connected with each other. Output of one module is input of other and connected with instantiation of sub modules to form architecture of router1x3.

VII. SIMULATION WAVEFORMS

Router 1x3 design verified with ISim simulator. Router input-output protocol is working as per proposed system.

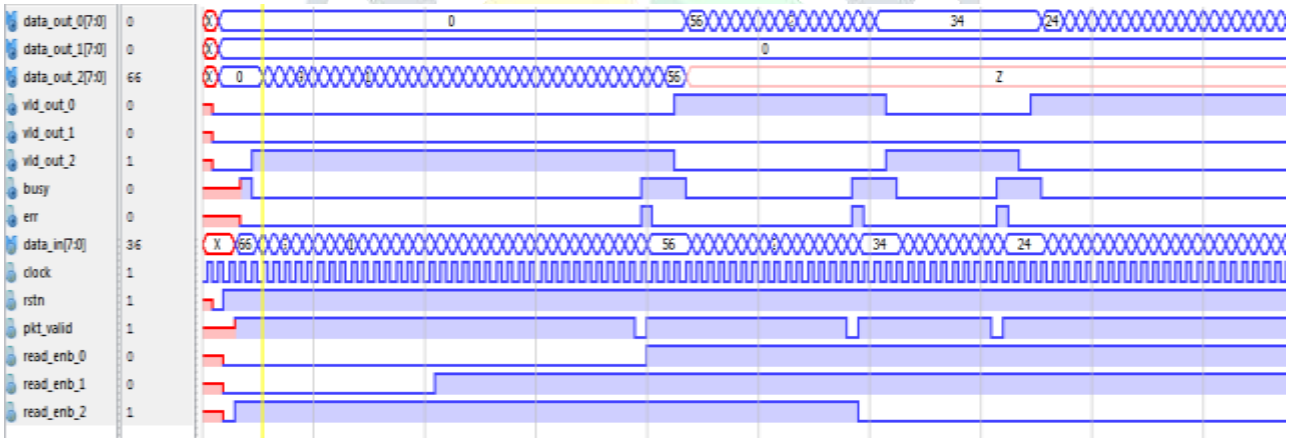


Fig.12 Router 1x3 Input-Output Protocol

Waveforms for each sub module have been observed to check functional correctness and to remove each single bug from design. Fig.13 shows waveform for FSM while Fig.14 shows waveform for FIFO module.

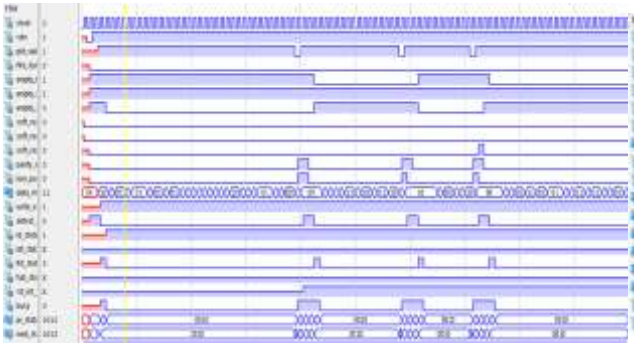


Fig.13 Waveforms - FSM

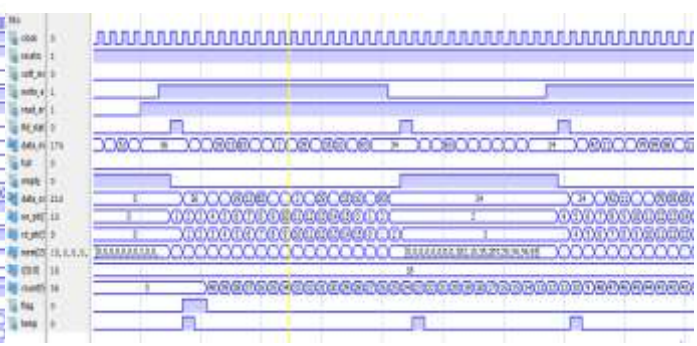
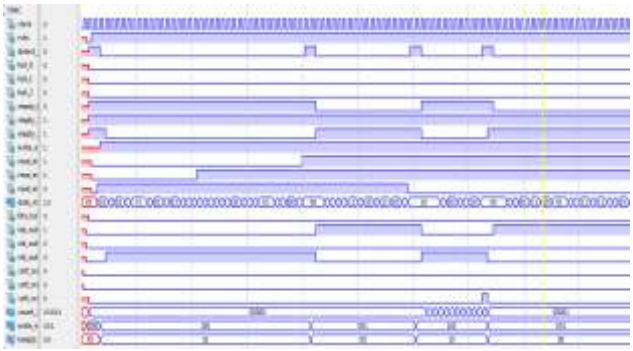


Fig.14 Waveforms- FIFO

Fig.15 shows waveforms for Synchronizer and Fig.16 shows waveforms for Register module.



. Fig.15 Waveforms - Synchronizer

Fig.14 Waveforms- Register

VIII. CONCLUSION

Virtual cut through mechanism proposed in this paper. With present work we conclude that router1x3 protocol designed, analysed and verified successfully. We measured code coverage on Questasim, it observed 81%. Power utilization for Spartan-3E FPGA family it observed 80mW.Memory requirement for design obtained from post synthesis it is observed 305MB. Proposed router design works on 131.097 MHz

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BIOGRAPHY

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