Low Power Logically Reduced TSPC Flipflop Design using Dual Threshold CMOS Technology

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Abstract*— The basic core unit of any sequential digital system is a Flipflop. The most widely used Transmission Gate (TG FF) based flip flop suffer from excessive work load on the clock signal. In this paper low power logically reduced True Single Phase Clock (TSPC) Flipflop using Dual Threshold (DT) technology is proposed. TSPC Flipflops reduces overhead on the clock signal. Logically Reduced Flip Flop (LRFF) is the optimized TSPC FF obtained by structure reduction method. Sub-threshold leakage is the dominating leakage currents over other leakage currents. Sub threshold leakage power can be reduced by using a high threshold voltage on discharging path. The proposed low power logically reduced TSPC using dual threshold technology reduces the overall power by 40.3% and power-delay product (PDP) by 34.8% compared to LRFF. The designs are implemented using cadence virtuoso 90nm technology.

***Index Terms*—TSPC, Dual threshold CMOS, TG FF, LRFF, Leakage power, 90nm technology**

I. INTRODUCTION

As the VLSI technology grows, the complexity of sequential storage operations are becoming complex and hence the design.The basic operation found in most sequential designs is the data storage and synchronization of operation at a given clock frequency. Data storage is the most basic sequential operation; and Flipflop is the most fundamental storage element of the sequential digital design. Flipflops occupy more area and consumes large power so it is very much necessary to optimize the basic storage elements.

The Flipflops power consumption in any typical digital system design, along with the clocking networks, constitutes around 20%–45% of the total power of the system. Particular application demand for high speed and low power, which is the motivation to go for new FF designs.

The most widely used existing Flipflop design is transmission-gate-based Flipflop(TGFF). The drawback of this design is the excessive overhead on the clock signal ie, number of transistors through which the clock signal passes is more and here both clock and its complementary signals are required. Same clock overhead problem also occurs in case of conventional SRFF designs, hence true single phase clocking (TSPC) Flipflop designs are developed. The main objective of TSPC design is to lower the work load on clock signal.

The enhanced version of the conventional TSPC design is logical structure reduction Flipflop. This design is has shorter setup time, consumes less static power by avoiding floating nodes and circuit simplification.

Sub-threshold leakage power is the dominating over all other leakage powers. Sub threshold leakage power can be reduced by using a high Vth(threshold voltage) transistors in leakage path. Though the high threshold voltage can be achieved by applying body bias but this leads to change all the secondary effects. Preferred method is by changing the channel doping concentration to achieve higher threshold voltage. This technique is known as Dual threshold CMOS [DTCMOS] technique. The symbols of Low threshold and High threshold transistors are as shown in Fig.1.In the present work, a low power logically reduced TSPC flipflop using dual threshold CMOS technology is proposed.

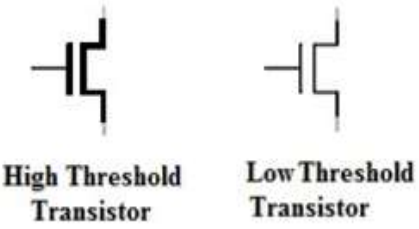

Fig.1. Symbol of Low Vth and High Vth transistors

II. OVERVIEW OF EXISTING FLIPFLOP DESIGNS

Existing Flipflop designs are reviewed for comparison purpose.

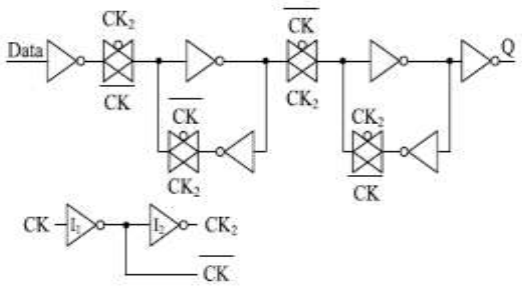

Fig.2. Transmission Gate based Flipflop Design

A conventional master slave Transmission Gate FF design is shown in Fig.2 it comprises of two TG based latches. The Inverters *I*1 and *I*2 shown in fig.2 are used to generate clock and complementary clock signal. This design introduces a higher overhead on clock signal. In this design, 12 transistors are driven by the clock out of 24 transistors, this indicates a continuous power consumption though the input remains static [5]. The same clock loading problem also occurs in conventional master slave Set-Reset FF designs.

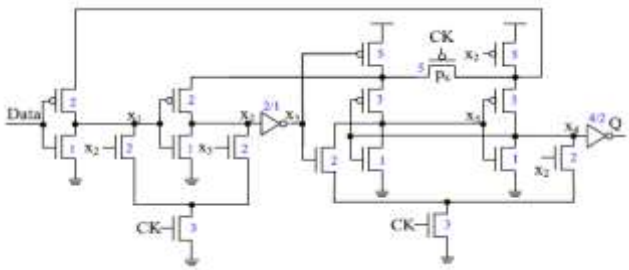

Fig.3. Circuit optimized using topologically compressed circuit scheme

To overcome the problem of clock signal power consumption Topologically Compressed FFs were designed. The Fig.3 shows SR latch based TSPC FF design called topologically compressed Flipflop (TCFF), obtained through a topological compression method. The master latch in the schematic circuit has multiplexer with feedback and Multiplexers can be implemented with AOI logic and an inverter.

Though the design shows improvement in the power consumption, but the timing parameters of the TCFF designs are not satisfactory. Especially the design suffers from a longer setup time. The number of pmos transistors connected to Vdd are only two hence this weakens the pull up network(PUN) hence the TCFF design suffer from longer setup time.

The enhancement of topological compressed FF is logic structure reduction FF shown in Fig.5. TCFF design can be optimized by reducing logic structure for shorter setup time, by circuit simplification for lower power consumption and by eliminating floating nodes to reduce static leakage problem.

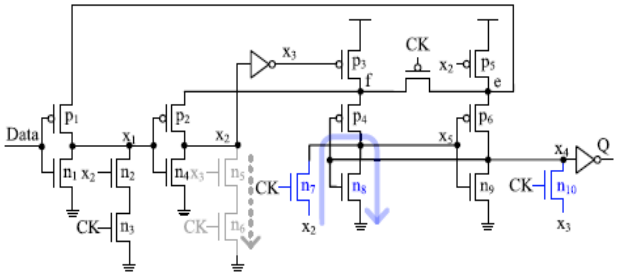

Fig.4. Circuit optimized using logical structure scheme showing discharge paths

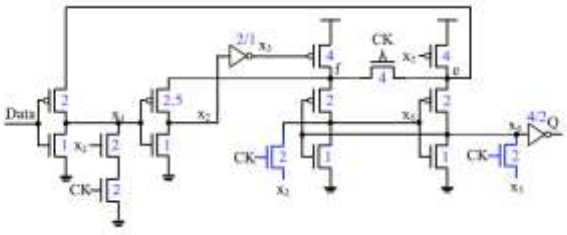

Fig.5. Circuit optimized using logical structure scheme

III PROPOSED DUAL THRESHOLD BASED FF DESIGN

The proposed DTCMOS based LRFF is shown in Fig.6. Here both low Vth and High Vth transistors are used in the circuit hence the name Dual threshold technology.

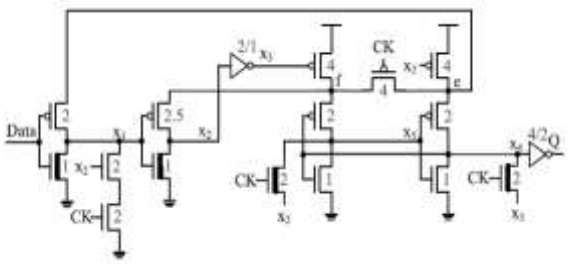

Fig.6.The proposed Dual threshold based LRFF design

The design is the same as a single-threshold logically reduced flip-flop but a high threshold voltage transistors are placed in some part of the design as shown in fig.6. The high Vth transistors reduces the leakage power by holding the state for longer time.

The timing parameters are maintained due to the low threshold transistors in the circuit. Sub-threshold leakage power is reduced by using a high Vth transistors in more frequent switching nodes of the circuit.

III IMPLEMENTATION

This segment includes execution parameters of the proposed Flipflop design. All the simulations are done utilizing Cadence Virtuoso tool using 90 nm technology with supply voltage VDD as 0.9 V. The library files utilized are analogLib and gpdk090. The conventional TG based FF is implemented for the comparison purpose which is shown in the schematic circuit Fig.7, TG based FF is built using 4 Transmission gates and 8 Inverters. The inverters I1 and I2 are used to generate clock and its complementary signals.

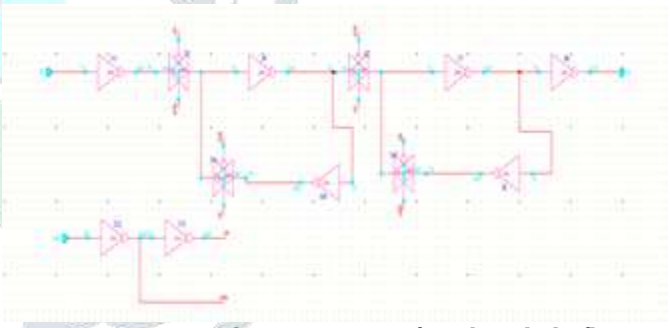

Fig.7. Schematic circuit of TG based Flipflop

Topologically Compressed FF obtained using Flipflop optimization scheme is applied to Mux based TSPC FF and is implemented using 21 transistors as shown in Fig.8. The enhanced version of the TCFF is logically reduced FF which is built using 21 transistors as shown in schematic circuit Fig.9.

Fig.8. Schematic circuit of topologically compressed Flipflop

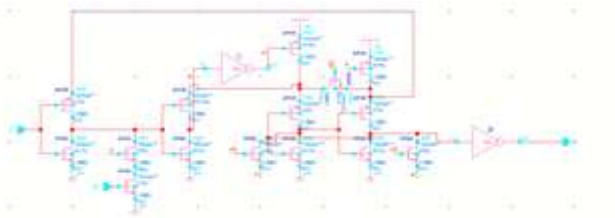

Fig.9. Schematic circuit of LRFlipflop

The conventional LRFF schematic circuit built using 19 transistors is as shown in Fig.9. The proposed low power logically reduced design is built using dual threshold technology using 19 transistors same number as that of conventional LRFF design as shown in Fig.10.

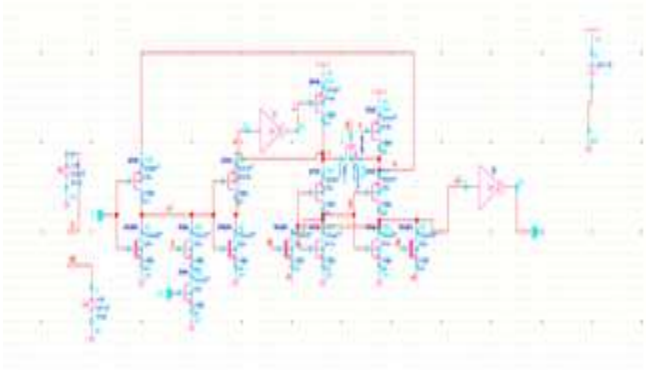

Fig.10. Schematic circuit of proposed low power LR Flipflop

III. RESULTS

The low power LRFF is designed, implemented and simulated using 90nm technology using cadence virtuoso tool at 0.9V supply. TGFF, TCFF, LRFF and proposed low power LRFF were implemented based on single threshold and Dual threshold techniques. The Fig.11 Fig.12 and Fig.13 shows the output waveforms of the TGFF, LRFF and proposed low power LRFF respectively. Here output follows the data input at rising edge of the clock as shown in output waveforms. The fig shows that all the nodes of the proposed design switch between Vdd and Gnd. The Output waveforms of proposed low power LR Flipflop at different nodes are shown in Fig.14.

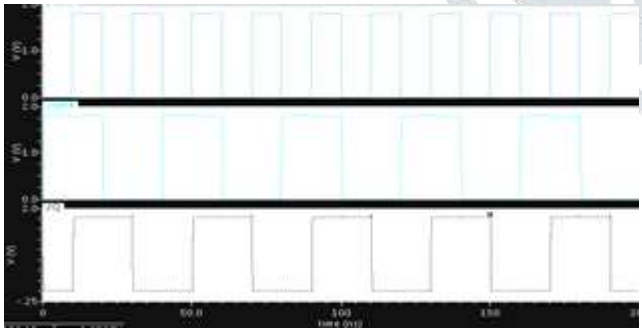

Fig.11. Output waveform of TG based Flipflop

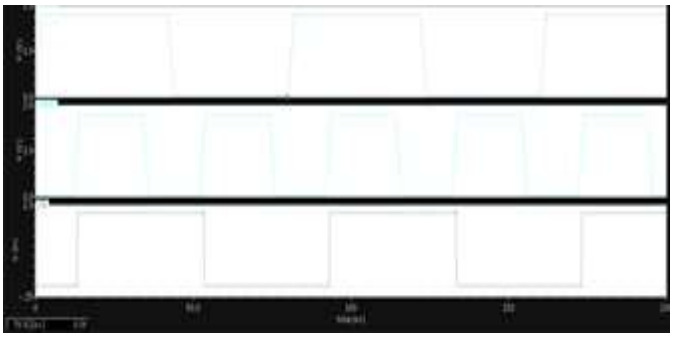

Fig.12. Output waveform of LR Flipflop

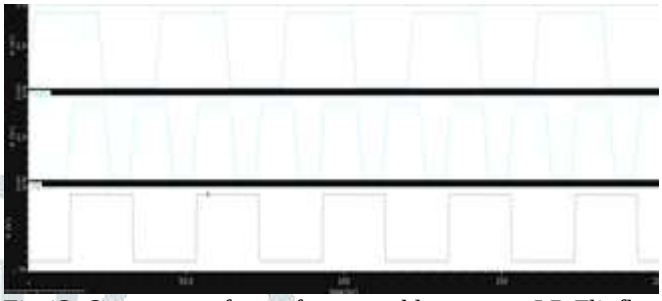

Fig.13. Output waveform of proposed low power LR Flipflop

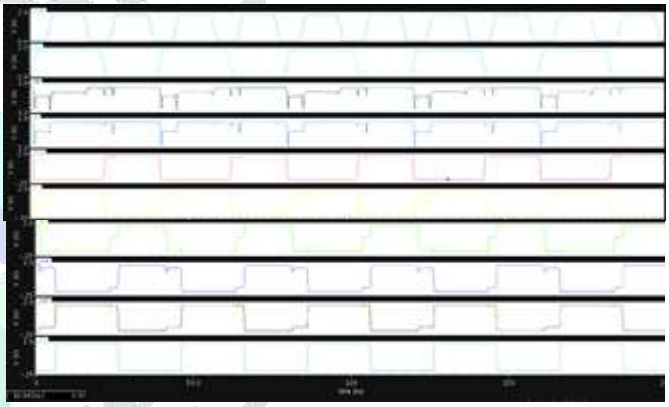

Fig.14. Output waveform of proposed low power LR Flipflop at different nodes of the circuit

The number of transistors, power consumption and delay are calculated and are compared with the conventional design. The comparison based on the different parameters for all 4 designs are shown in Table I.

TABLE I: Comparison made on different parameters of the FFs

FF Design	TG FF	TC FF	LR FF	Proposed Low power LR FF
No. of Transistors	24	21	19	19
Setup time(pS)	84.65	185.75	124.07	120.1
Hold time(pS)	-56.52	-42.5	8.9	20.3
Clock to Q delay(pS)	172.34	133.1	127.69	139.7
Power(uW)	8.9	4.59	3.38	2.02
PDP(fJ)	1.53	0.611	0.431	0.281

IV. CONCLUSION

The high threshold voltage transistor has a characteristic of less leakage current hence the dual-threshold LR flip-flop is used. The simulation results show 40.3% reduction in the static power dissipation of the proposed low power LRFF.The hold time for the proposed design is positive which ensures that completion data transition in slave stage. Power delay product is reduced by 34.8% compared to conventional TGFF.

Future scope:

- The same work can be implemented using 45nm, 7nm and still its parameters can be optimized.
- Furthermore, it can be used in several applications like Data converters, microprocessors, counters, clocking systems,etc

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