Design & Implementation High frequency Candy Vending Machine on Spartan 3 Using Customized DCM.

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Abstract:. This paper presents a modified design of Area-Efficient Low power 16x16 Candy Vending machine Circuit. In most of the digital circuit, clock is used as a input variable and clock is assigned during stimulation. Xilinx software is used to carry out all the design and implementation process.In this design a *a single* Digital clock manager(DCM) is used to generated a clock. In candy vending Machine Seven state are used and overall operation is carried out using adders, multiplexer, inverter. Single DCM for high frequency operation.

Indexterms:Single DCM, Xilinx, Adders, Multiplexers.cadence, utilization Factor.

I. INTRODUCTION

Digital circuit design has evolved rapidly over the last 25 years. The earliest digital circuits were designed with vacuum tubes and transistors. Digital system design is carried on platforms such as Xilinx, Quatrus Altera, Questa etc. Since all the inputs available is nature is analog, it is mandatory to convert then in digital format. This conversion is done using 16 bit ADC converter using Opamp. For a long time, Programming language such as FORTRAN, Pascal, and C was being used to describe computer programs that are sequential in nature, Hardware description is language is the standard language to describe the functionality of the circuit.Digital circuit could be described at a register transfer level(RTL) logic synthesis pushed the HDLs into the forefront of digital design. Designers no longer had to manually place gates to build digital circuits.Spartan 3E board is used to for implementation. Speed offered by Spartan 3E is "-5" whereas speed offered by Spartan 3 is -3.

In booth's multiplier design 31 adders 31 subtractors and 256 multiplexers are used. Adders are used to perform addition whereas subtractors are implemented using Two's complement method.

In this paper a XILINX 14.2 software is used to perform design, simulation and implementation of 16x16 bit multiplier based using behavioral style of Verilog coding.A Typical design flow for designing VLSI IC circuit is shown in Figure 1.1. In any design, specifications are written first, the main aim of the designer is to design the low power, low tolerance IC design , the specification describes the functionality, interface and overall architecture of the digital circuit to be designed. The behavior description is manually converted into an RTL description in an HDL.Logic synthesis tools convert the RTL description to a gate-Level Netlist. The gate-Level netlist is input to an Automatic Place and Route Tool.Most digital design activity is concentrated on manually optimizing the RTL description of the circuit.In design of any VLSI based (IC) either analog or digital the steps of physical layout, layout verification & Implementation are same.

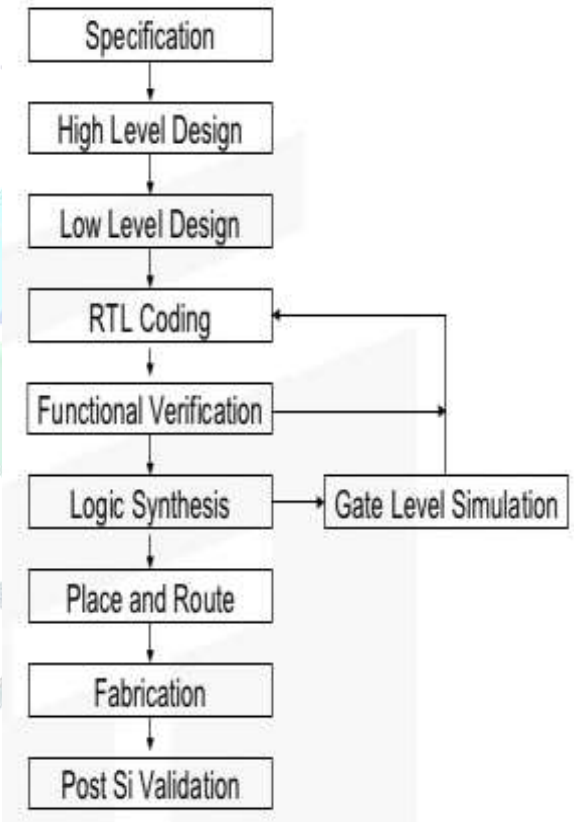


Fig 1.DESIGN FLOW

Digital system design is divided into two major categories 1. Combinational circuits shown in Fig 2. And 2.Sequential circuits showed in Fig 3.

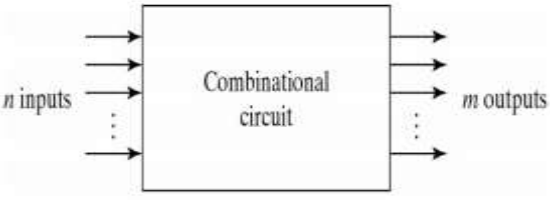


Figure.2 COMBINATIONAL SYSTEM

A combination circuit dependent on input whereas the sequential circuit totally depends on the clock signal. A

combination circuit does not have memory it depend only on current values of the input, it consists of only multiple inputs and outputs. The simplest combinational logic circuit has one input and one output is the inverter, whose output is the inverse of its input and ALU's consisting of multiple instances can also be designed using combinational circuit topology.
The general model of a sequential circuit is shown in Fig 3.

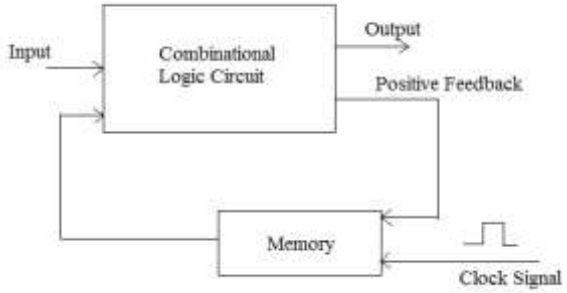


Figure.3 SEQUENCTIAL SYSTEM

A sequential system design is further again classified in to 2 major categories depending on the clock signal.1. Synchronous system design and 2.Asynchronous System design.
In synchronous sequential circuits the contents of memory elements can be changed only at an instant of rising or falling edge of clock signal. In asynchronous sequential circuit the contents of memory elements can be changed at any instant of time.Hence the outputs and the next state of the sequential circuit are decided by the external inputs and the present state.

RESEARCH WORK

In order to design high frequency digital circuits, it is mandatory to generate the high frequency, In this design the high frequency generation is done by the single DCM (digital clock).For the design of Opamp is references are considered..1In design of any sequential digital circuit till today it is observed that a single clock of particular frequency is used which is driven by the user.Initially a clock signal operating at a frequency of 250 MHz is generated using single DCM .Input frequency of the DCM is 45 MHz. By using the multiplication factor with is possible to interface high. Digital clock manager (DCM) is used to generate multiple clocks of the desired frequency. Various clocks of different frequency and phase shifts can be generated using it. Speed devices and by using the Division Factor (D) low frequency device with other devices respectively. DCM is a pin IC consisting of 2 inputs and 6 outputs. The outputs pins are CLKO_OUT,CLKFX_OUT,CLKDV_OUT,CLK2X_OUT,CLKIN_IBUF_OUT,LOCKED_OUT.
By proper selection the phase shifted output signal can also be generated.DCM IC provides a flexibility of generated 90,180 & 270 degrees phase shifted outputs. The DCM also provides the multiple feedback selectivity option. This feedback is nothing but the clock distribution delay feedback. It can be observed in the internal structure of DCM.The block diagram of the DCM IC is showed in Fig 4.

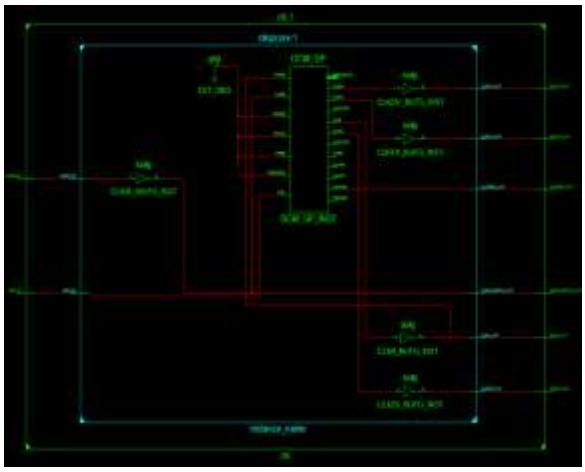
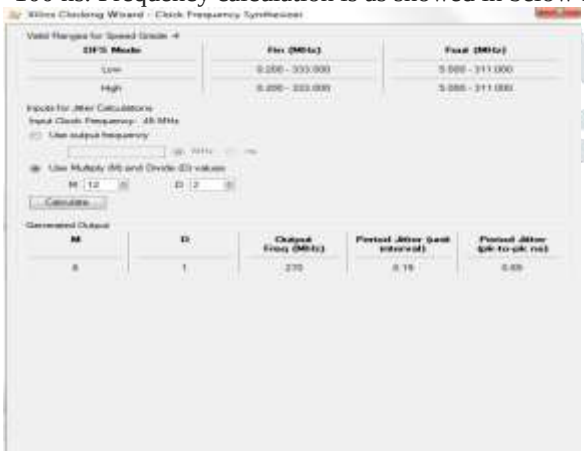


Figure.4 Digital Clock Manager

Intially a DCM is programed to generated multiple frequnecy. Input applied to the DCM are CLKIN_IN,RSTIN_IN. clock signal of specfic frequency is applied. The DCM consists of In this design the input frequency of 45MHz is used. The Division Multiplication factor used in the design are 12 & 2.Since the Multiplication factor is 12 ouput clock frequency generated at the output signal CLK2X_OUT is 270MHz this frequnecy is used in the design of Booth's Multiplier.
The reset pin is Acive Low.The duty cycle of the input signal is 50%.Internally the DCM consists of 6 major unit.
1.INPUT STAGE
2.PHASE SHIFTER
3.DELAY TAPS
4.DIGITAL FREQUNECY SYNTESIZER
5.DELAY TAPS
6.CLOCK DISTRIBUTION DELAY
INPUT Stage consists of clock inputs and the reset input pins. Phase shifter is used to control the phase shift as per the requirement.The following signals control the phase shift offered by the DCM.
A clock signal is provided to PSCLK to clock the phase shift controller. This clock should be something that is used to create the other signals. Use of a 50 MHz, or 100 MHz clock is common, but it can be anything convenient, and it also should be the clock that synchronizes the other control signals. PSEN is the enable. High to enable it, low to stop using the phase shift feature. The phase shift that you are at remains when PSEN is low.PSINCDEC is high to increment (increase the shift) and low to decrease the shift. On the next rising edge of PSCLK, the shifter will start to execute the shift.The Digital Frequency Synthesizer (DFS) provides a wide and flexible range of output frequencies based on the ratio of two user-defined integers, a Multiplier CLKFX_MULTIPLY (M) & the Divisor (CLKFX_DIVIDE) which . The output frequency is derived from the input clock (CLKIN) by simultaneous frequency division and multiplication. This feature can be used with or without the DLL feature of the DCM. If the DLL is not used, then there is no phase relationship between CLKIN and the DFS outputs.
The Status Logic indicates the current state of the DCM via the LOCKED and STATUS output signals. The LOCKED output signal indicates whether the DCM outputs are in phase with the CLKIN input. The STATUS output signals indicate the state of the DLL and PS operations. The RST input signal resets the DCM logic and returns it to its post-configuration state. Likewise, a reset forces the DCM to reacquire and lock to the CLKIN input.The Delay-Locked Loop (DLL) unit

provides an on-chip digital deskew circuit that generates zero-propagation-delay clock output signals. The deskew circuit compensates for the delay on the routing network by monitoring an output clock, either the CLK0 or the CLK2X. The DLL unit effectively eliminates the delay from the external clock input port to the individual clock loads within the device. The well-buffered global network minimizes the clock skew on the network caused by loading differences. The input signals to the DLL unit are CLKIN and CLKFB. The output signals from the DLL are CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.

In the design of sequential booth multiplier.2 modules are defined. First modules define the input configuration of DCM. Based on the configuration the output frequency is generated. Single feedback is used in configuration of DCM.Even tough is the accepted clock signaling with required frequency is generated at the output still jitter is observed in the output.Clock jitter is the deviation of a clock edge from its ideal position in time. Simply speaking, it is the inability of a clock source to produce a clock with clean edges. As the clock edge can arrive within a range, the difference between two successive clock edges will determine the instantaneous period for that cycle. So, clock jitter is of importance while talking about timing analysis. There are many causes of jitter including PLL loop noise, power supply ripples, thermal noise, crosstalk between signals etc. Let us elaborate the concept of clock jitter with the help of an example:A clock source (say PLL) is supposed to provide a clock of frequency 10 MHz, amounting to a clock period of 100 ns. If it was an ideal clock source, the successive rising edges would come at 0 ns, 100 ns, 200 ns, 300 ns and so on. However, since, the PLL is a non-ideal clock source, it will have some uncertainty in producing edges. It may produce edges at 0 ns, 99.9 ns, 201 ns etc. Or we can say that the clock edge may come at any time between (<ideal time>+- jitter); i.e. 0, between 99-101 ns, between 199-201 ns etc. (1 ns is jitter). However, counting over a number of cycles, average period will come out to be ~100 ns. Frequency calculation is as showed in below fig.



Another instance defines candy vending machine algorithim. It has 4 inputs insertion coin, clock, reset, and 1output register . During bitwise operations the variables are stored in the temporary registers. Input clock signal and active low is enable signal is directly connected to the DCM inputs. This connection is done but instantiating the module instance. The main module is candy vending machine and instance of DCM module created in the main module and connections are made in the module with the help of wire, In the design of the module, 31 adders/subtractors, 256 multiplexers and 256 1bit 4:1 multiplexers are used. The utilization factor decreases as combinational design is converted into sequential. The utilization factor of candy vending machine implemented using the combinational design approach is 67%(showed in fig 7) whereas when the design is implanted using sequential methodology the utilization factor reduces to 50%(showed in fig 8).The Multiplexer & adders are showed in Fig 5,6.

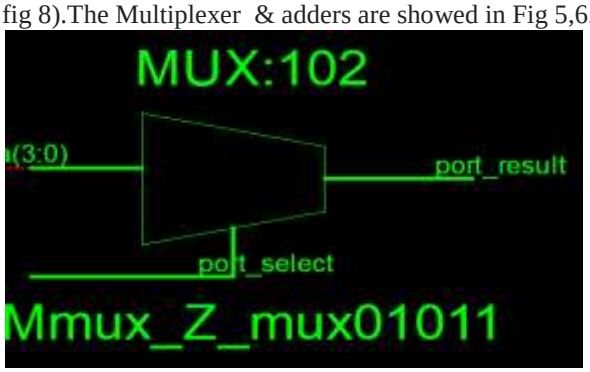


Figure.7 1 Bit 4:1 Multiplexer

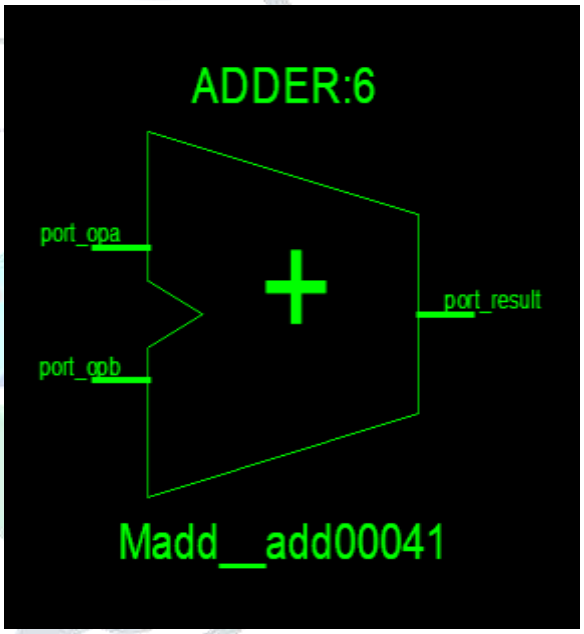


Figure.8 Adder

The main module consisting clk module as a instance is shown in fig 8.It is clearly observed that the 2 inputs x,y of main module is connected to the DCM module pins repectively. Input clock signal is applied to “X” pin whereas acitive low RSTIN_IN input is applied through “Y” pin as shown in Fig 9.

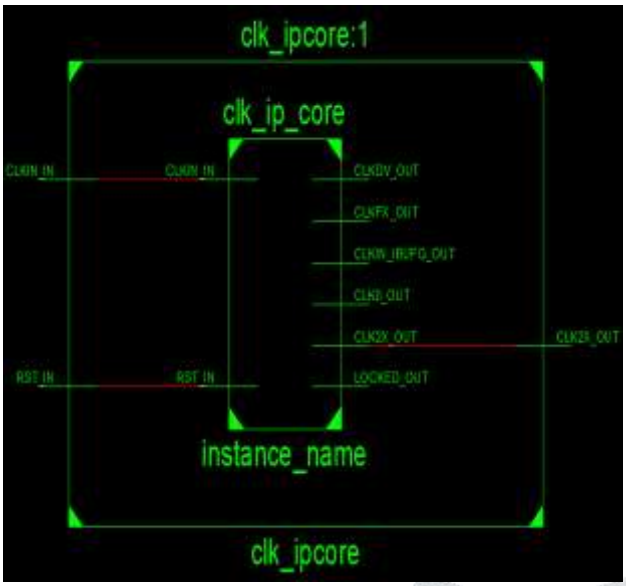
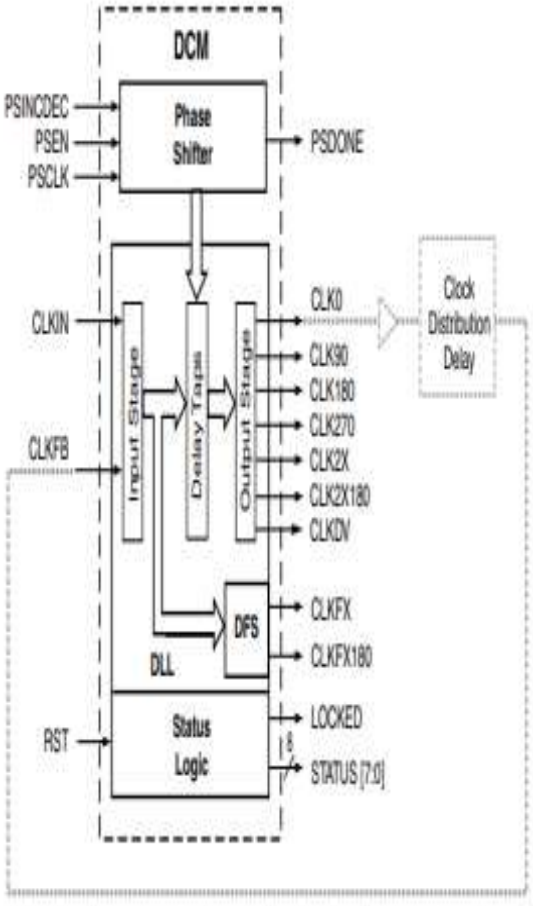


Figure.9 Main Module Structure

In the Fig it can be observed that the in 1st clock cyle time span between clock cycle of CLK2X_OUT is more as compared to CLKDIV_OUT. This is due to the jitter it may lead to un necessary time utilization.

This issue of clock jitter can be avoided by specifying accurate delay. In this design a delay of 1275ns is specified because after this much time the simulation is periodic as per the frequency is concerned. If proper delay is not specified then inputs are passed before the start sequential.The Output for design is as shown in the Experimental results.

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=========================================================================
HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                    : 31
 16-bit adder                          : 31
# Multiplexers                          : 256
 1-bit 4-to-1 multiplexer              : 256

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Figure.10 Simulation Summary

Experimental Results

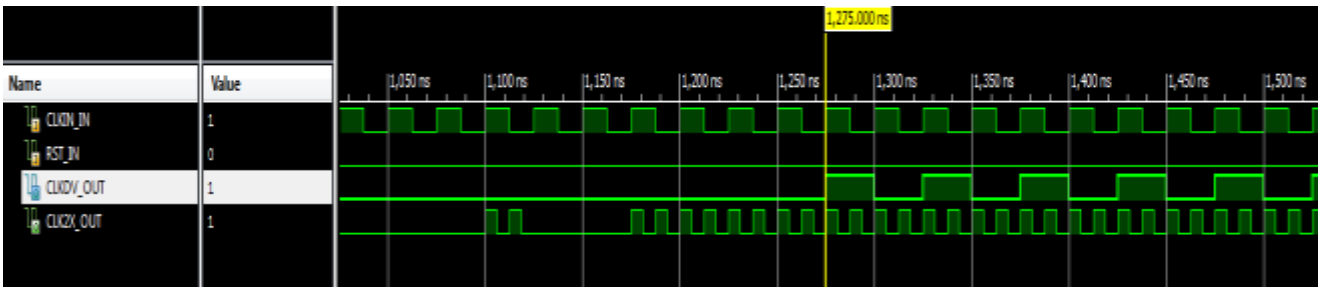
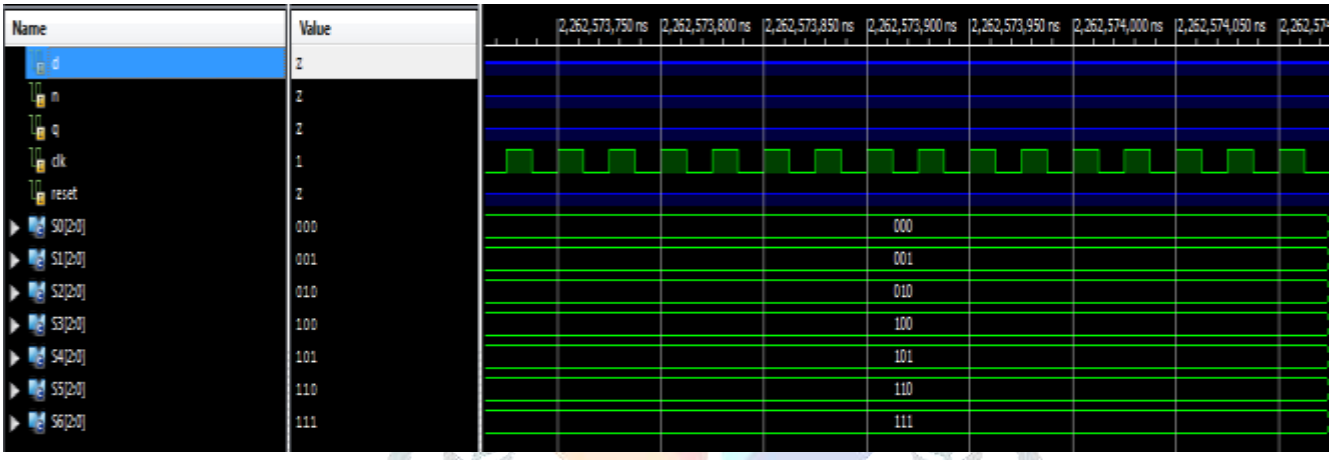


Figure.11 DCM simulation results



Candy Vending Stimulation

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	521	768	67%
Number of 4 input LUTs	978	1536	63%
Number of bonded IOBs	64	97	65%

Summary Report of Combinational Candy Vending Stimulation

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	521	960	54%
Number of 4 input LUTs	978	1920	50%
Number of bonded IOBs	66	66	100%
Number of GCLKs	4	24	16%
Number of DCMs	1	2	50%

CONCLUSION

From the experimental results and analysis of combinational and sequential circuit designs certain conclusion are made.1. If a system is transformed form combinational to sequential domain. Utilization is reduce resulting in the reduction of

number of slices. Reduction in utilization leads to availability of
More slices of other circuits implementations. 2.Even the input signal is of low frequency still with the use of DCM's high frequency clock signal can be generated. Use of Single DCM provides the flexibility to interface 4 devices operating a various frequency having certain phase shifts.3. By assigning proper delay in the test bench the jitter produced can also be avoided.

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