Design And Simulation Of Transistor Clamped H Bridge With Multi Carrier Pulse Width Modulation

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Abstract : Reduced voltage stress and low-total harmonic distortion are the main causes for such widespread application of multilevel inverters (MLIs) in various industrial sectors. However, reliability is one of the major concerns of MLIs as it uses a large number of switches as compared with two-level inverters. Therefore, a newly developed transistor clamped H-bridge inverter is proposed in the literature which uses a relatively less number of switches and DC sources as compared with cascaded H-bridge but lacks in reliability due to the absence of redundant states. Hence, in this study, the reliability improvement strategy for newly developed five-level transistor clamped H-bridge-based cascaded inverter is proposed which can be generalized for any number of levels. In the proposed fault tolerant strategy, the fault can be broadly classified based on the two main legs of the proposed inverter. Moreover, the proposed fault tolerant strategy does not require any kind of external circuit for maintaining its capacitor voltage in the balanced state. Finally, to validate the concept, a laboratory prototype of the five-level inverter is developed and results are obtained successfully.

IndexTerms **- NPC Inverter, MCPWM, Motor**

I. INTRODUCTION

Somecomponents,suchasmultileveledequations,graphics,andtablesarenotprescribed,althoughthevarioustabletextstylesareprovided.Theformatterwillneedtocreatethesecomponents,incorporatingtheapplicablecriteriathatfollow. Reduced voltage stress and low-total harmonic distortion are the main causes for such widespread application of multilevel inverters (MLIs) in various industrial sectors. However, reliability is one of the major concerns of MLIs as it uses a large number of switches as compared with two-level inverters. Therefore, a newly developed transistor clamped H-bridge inverter is proposed in the literature which uses a relatively less number of switches and DC sources as compared with cascaded H-bridge but lacks in [1]reliability due to the absence of redundant states. Hence, in this study, the reliability improvement strategy for newly developed five-level transistor clamped H-bridge-based cascaded inverter is proposed which can be generalized for any number of levels. In the proposed fault tolerant strategy, the fault can be broadly classified based on the two main legs of the proposed inverter. Moreover, the proposed fault tolerant strategy does not require any kind of external circuit for maintaining its capacitor voltage in the balanced state.

The pulse width modulation (PWM) multilevel inverter as an effective alternative to current inverter topologies and provided an introduction of the modeling techniques and the most common modulation strategies. *Lai and Peng have* described three recently developed multilevel voltage source converters and the techniques to balance the voltage between different levels in multilevel converters. *Rodriguez* have described the most relevant control and modulation methods developed for this family of converters: multilevel sinusoidal pulse width modulation (SPWM), multilevel selective harmonic elimination,[2][3]and space-vector modulation. Tolbert have experimentally demonstrated that traditional two-level high-frequency PWM inverters for motor drives have several problems associated with their high-frequency switching and two different multilevel topologies are identified for use as a converter for electric drives. *Rodriguez* have introduced the PWM regenerative rectifiers with reduced input harmonics and improved power factor. In early stages, multilevel active rectifiers were employed mainly in high-voltage, high power industrial and traction applications because they distribute the applied voltage among a number of cascaded power devices, thus overcoming their voltage limits and allowing the elimination of output transformers in medium- to high-voltage systems. Since their output voltage is a modulated staircase, the fact that they outperform two-level PWM inverters in terms of total harmonic distortion (THD), [5] [6]without the use of bulky expensive and dissipative passive filters, has been demonstrated in Cecati Multilevel inverters in the field of renewable energies, including PV generators, have been described in Kjaer and Calais and Agelidis. *Calaisand Gonzalez* have developed unipolar SPWM full-bridge with transformer-less grid-connected inverter, a lot of depth researches, where new freewheeling paths are constructed to separate the photovoltaic array (PVA) from the grid in the freewheeling period.

Multi cell DC–AC converter for applications in renewable energy systems. Alonso have introduced a new control method and proportional PWM of the cascaded H-bridge multilevel converter for grid-connected PV systems, and this control makes each H-bridge module[10] supply different power levels, allowing, therefore, for each module an independent maximum power point tracking of the corresponding PVA. Walker and Sernia14 have proposed an alternative topology of non-isolated per panel DC–DC converters connected in series to create a high-voltage string connected to a simplified DC–AC inverter, and buck, boost, buck–boost, and Conk converters are considered as possible DC–DC converters that can be cascaded[6]. *Rahiman* have developed a 15-level cascaded H-bridge configuration; equal DC voltages are selected for each unit, with step modulation and fundamental

frequency switching which reduced conduction loss and switching loss. Kang et al.16 have developed multilevel PWM inverters suitable for the use of stand-alone PV power grid-connected inverters for PV modules.*Alepuz* have described a three-level inverter that can be used to interface distributed DC energy sources with a main AC grid or as an interface to a motor drive. Ozdemir have proposed a five-level DMLI fundamental frequency switching strategy for three phase stand-alone PV systems by selecting the switching angles such that the lower order harmonics are eliminated. Besides being able to maximize the power obtained from the PVAs, the multilevel converter usually presents the advantages of reducing the device voltage stress, being more efficient, and generating a lower output, that is, a voltage harmonic distortion. Among the following three main families of multilevel converters, diode-clamped, capacitor clamped, and cascaded H-bridge, the latter is usually considered in the literature for PV applications.

*Shanthi and Natarajan*have proposed multilevel inverter control strategies implemented in real time using field-programmable gate array (FPGA) for linear and non-linear loads.*Yang* have introduced H∞ controller with explicit robustness in terms of grid-impedance variations to incorporate the desired tracking performance and stability margin. Josh have proposed multilevel inverter in the field of renewable energies, which reduces output filter dimensions and influences the perturbations caused by cloud darkening or seasonal variations. Mei have proposed an improved phase disposition pulse width modulation (PDPWM)[8][9] for a modular multilevel inverter which is used for PV grid connection to achieve dynamic capacitor voltage balance without the help of an extra compensation signal. It is clear from the above literature works that many researchers are addressing their efforts in proposing new inverter topologies or in modifying the existing ones, aiming at improving the quality of the energy available at the inverter terminals. Among the available multilevel inverter topologies, cascaded H-bridge multilevel inverter is proven to be the best for its high power-handling capacity and reliability due to its modular topology and constitutes a promising alternative that can be extended to allow a transformer-less connection to the grid. The cascaded H-bridge multilevel inverter requires separate DC source, and it is a drawback when a single DC source is available, but it becomes a very attractive feature in the case of PV systems because solar cells can be assembled in a number of separate generators. The[6]CHB-MLI supports different PWM techniques like SPWM, selective harmonic elimination pulse width modulation (SHEPWM), and optimized harmonic stepped waveform (OHSW)

II. Type Style and Fonts

Modulation strategy: The gate pulses for the switches in the proposed topology is provided by using suitable multi-carrier pulse width modulation (MCPWM) strategy with a carrier frequency of 5 kHz,

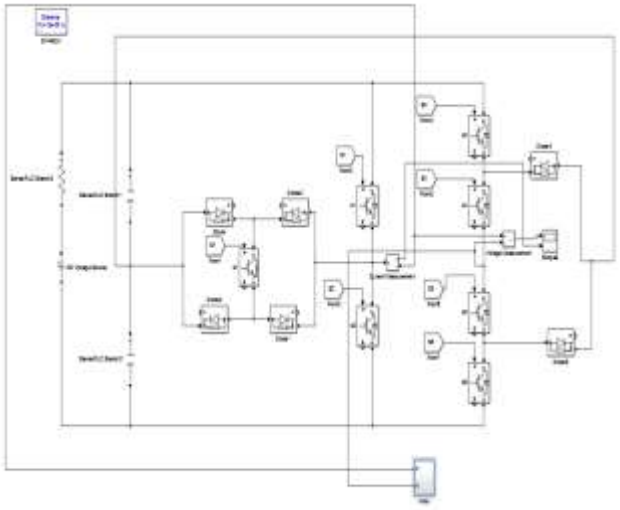

Fig 2.1 H Bridge inverter

Whereas reference signal frequency is kept at

50 Hz. In MCPWM scheme, the carrier signals are compared with the reference signal and the pulses so obtained are used for switching of the devices corresponding to their respective voltage levels. Under normal operating conditions, the modulation index is close to unity, whereas under the faulty condition the modulation index is reduced to half. Fig. 4.1 shows the control strategy adopted for obtaining the pulses for individual switches. For simplicity, the carrier frequency is assumed to be about 100 Hz, which can be increased to any specified frequency with same control strategy, as shown in Fig. 4.2. Here in one cycle, the reference signal is divided into nine different modes:

Mode 1:

a0 = 0 < t < t 1 and t 4 < t < t 5 and t 8 < t <0.02 Mode2:

a1 = t 1 < t < t 2 and t 3 < t < t 4

Mode 3:

a2 = t 2 < t < t 3

Mode 4:

a−1 = t 5 < t < t 6 and t 7 < t < t 8

Mode 5:
a−2 = t 6 < t < t 7 (10)
By using logical operators switching pulses for the switches can be obtained as:
S1 = a2
S2 = a−2
S3 = a−1 + a−2
S4 = a0 + a−1 + a−2
S5 = a0 + a1 + a2 S6 = a1 + a2
S7 = a0 + a1 + a−1

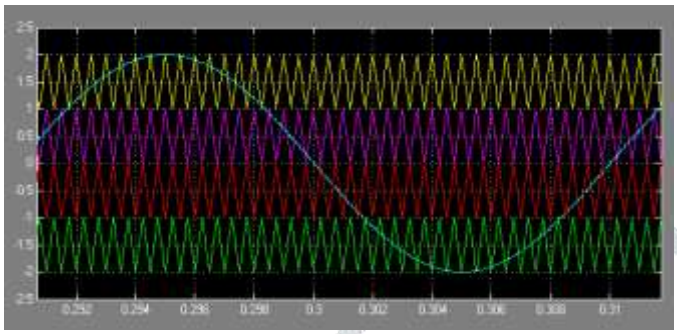

Fig 2.2 simulation results of Multi carrier pulse width modulation

After using above combinational logic, the switching pulse for normal operating conditions have been obtained and is depicted in Fig. 4.3. Under a fault condition on the switches of leg-I, only the modulation index is modified and keeping the switching scheme same as in normal state.

III. COMPARISON AND DISCUSSION

Thetemplateisusedtoformatyourpaperandstylethetext.Allmargins,columnwidths,linespaces,andtextfontsareprescribed;pleasedonotalterthem.Youmaynotepeculiarities.Forexample,theheadmargininthistemplatemeasuresproportionatelymorethaniscustomary.This measurementandothersaredeliberate,usingspecificationsthatanticipateyourpaperasonepartoftheentireproceedings,andnotasanindependentdocument.Pleasedonotreviseanyofthecurrentdesignations. In this section a suitable comparison is drawn between proposed and conventional topologies for a five-level inverter.

Table-3.1 comparison of various topologies based on blockingvoltage

PARAMETERS	5-LEVEL TCHB TOPOLOGY	5-LEVEL TCHB PROPOSED	CHB	NPC	FC	11	12	13
VDC/2	1	5	8	8	8	20	2	4
VDC	4	2	0	0	0	2	0	4
Total blocking voltage	9/2*VDC	9/2*VDC	4*VDC	4*VDC	4*VDC	12*VDC	10*VDC	6*VDC
Dc source	1	1	2	1	1	1	4	1
capacitor	2	2	0	4	10	7	0	2
clamped diode	2	0	0	12	0	0	0	2
Reliability	NO	YES	YES	NO	NO	YES	YES	YES

Table 3.1 gives the detailed comparison of various topologies based on blockingvoltage, DC source and capacitor requirement, clamping diodesand fault tolerance abilities. In proposed modified TCHB topologyfor five-level inverter, one leg is formed by NPC leg instead ofCHB leg. Even though the number of switches looks more inproposed modified topology, but the total blocking voltage remains the same as compared with TCHB inverter as given in Table 1.Proposed topology and CHB is tolerable to fault as compared with the rest of the topologies as given in Table 4, respectively.

Table 1 also provides the comparison of proposed topologywhich recently proposed fault tolerant topologies. The reliability of the proposed topology is more since it requires less number ofswitches as compared with topologies of [11]. Moreover, thetotal amount of voltage blocked by proposed by the switches ofproposed topology is least as compared with topologies of ,respectively. Moreover, the topology of [11] cannot tolerate faultson any of the switches (i.e. total eight switches) which are closer to its DC link. Proposed topology requires less number of DC sources as compared with the topology of [12]. Topology [13] cannot be operated under short circuit fault conditions, whereas the proposed topology can be operated under both open and short circuit fault.

IV. RESULTS

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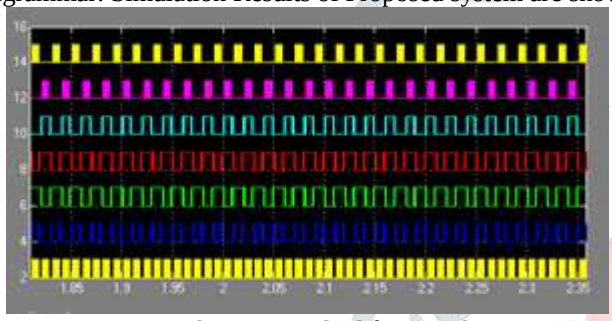

Fig 4.1 Mpwm techniques applied for switches

Fig 4.1 shows the switching operation of the system under no fault condition

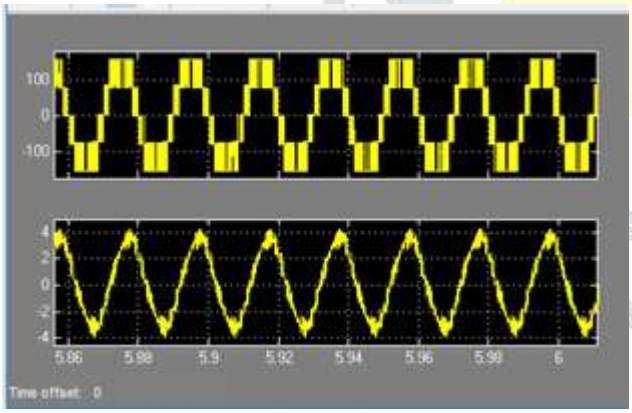

Fig4.2 Normal condition

Fig 4.2 shows the five level output of voltage and current of the Hbridge under the no fault condition

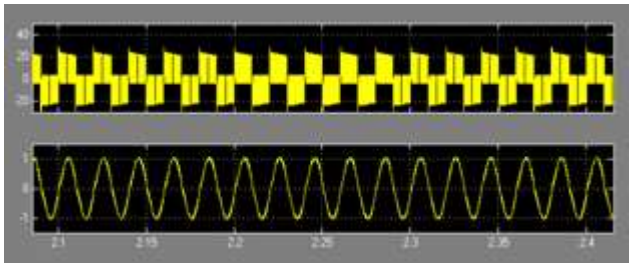

Fig 4.3 Leg one fault

Fig 4.3 shows the output of voltage and current of H Bridge under leg one fault

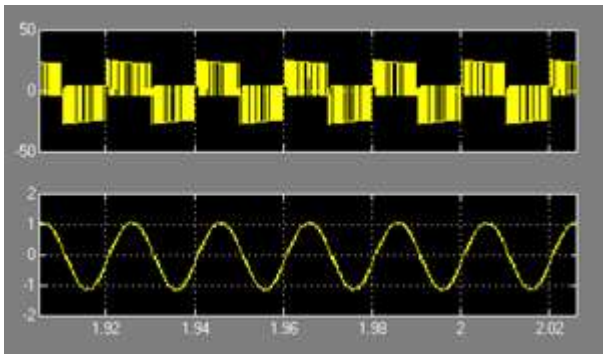

Fig 4.4 Leg two faults

The above Fig shows the output of voltage and current of H Bridge under leg two faults

Results with motor load

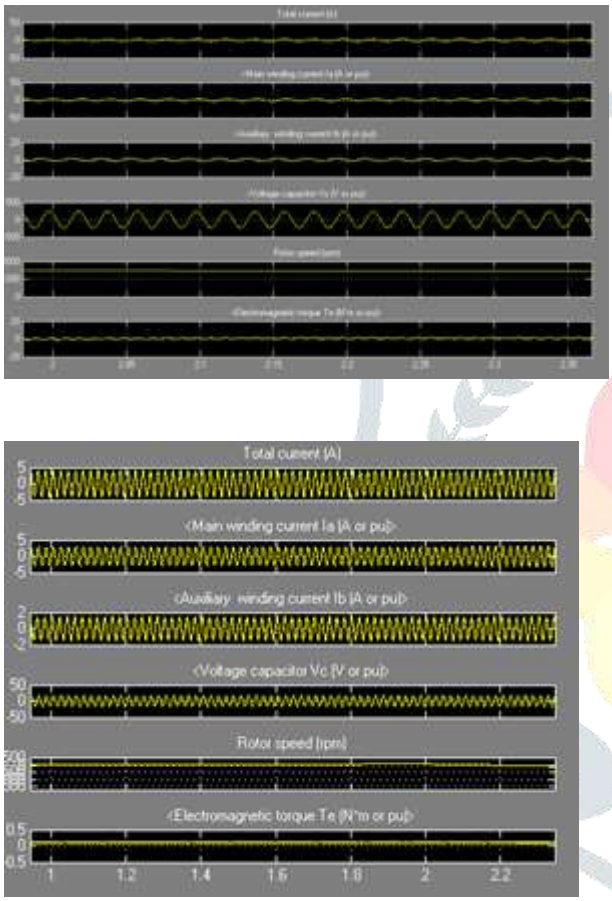

Fig4.5 Motor load output

Fig 4.5 shows the output of total current, winding current, voltage of capacitor and rotor speed of H Bridge under motor load

IV.CONCLUSION

This NPC leg helps in creating inner voltage redundancies due to which inverter can still be operated under faulty conditions as three-level inverter by reconfiguring the control technique. Moreover, fault on the capacitor can be tolerated, but with increased voltage ripples in the capacitor voltage under faulty conditions. Proposed topology poses add on advantage of self-voltage balancing of its capacitor voltage both under normal and post-fault state.

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