MAJORITY LOGIC IMPLEMENTATION OF MAC UNIT

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Abstract: In digital signal processing applications it involves many critical operations such as multiplication and accumulation, so multiply accumulate unit is always a key element to perform high speed operations. In this project, majority logic gates are used to implement the MAC unit. Majority logic gates are the key elements in the QCA technology. The project is simulated and synthesized using Xilinx ISE tool and Verilog HDL is used to describe the behavior or functionality of the MAC. The delay comparisons for various QCA based parallel prefix adders and the MAC unit for different multipliers and adders are given.

IndexTerms–CMOS, MAC, Majority Logic gate, QCA

I. INTRODUCTION

Adder is the key element in most digital circuit designs including digital signal processors (DSP) and microprocessors data paths units. Therefore the performance of the digital system depends on the performance of the adders. In this project parallel prefix adders are implemented by using quantum cellular automata (QCA) logic for high speed of operations. The advantage of using the QCA technology, it is having the high density due to small size of dots and the other feature it is having high switching speed. Due to these advantages the high performance parallel prefix adders are implemented in the multiply accumulate unit to further increase the performance of the MAC unit.

The paper is organized as follows: section II describes about the QCA technology and majority logic gates and section III describes the parallel prefix adders using QCA and section IV describe about the MAC unit using QCA and then follows the simulation results and the comparison table for the delay and area utilization.

II. QUANTUM CELLULAR AUTOMATA (QCA)

QCA have attracted a lot of attention as a result of its extremely small feature size (at the molecular or even atomic scale) and its ultra-low power consumption making it one candidate for replacing CMOS technology [1].

The logic unit in QCA is the QCA cell which is composed of 4 or 5 quantum dots. A quantum dot is a nanometer size structure that is capable of trapping electrons in three dimensions. The basic building blocks of QCA are majority logic gate and inverter gate.

2.1 Majority logic gate

The majority logic gate that implements the majority function and it is a device that outputs high when the majority of its inputs are high, otherwise it outputs low.

It can also be defined as returns true if and only if more than 50% of its inputs are true. Majority logic gate used in many applications of Boolean circuits and circuit complexity.

Majority logic gates can be of different types like three input majority gate and multi input majority gate. In this project three input majority logic gate is used and the logic diagram is shown in figure 1.

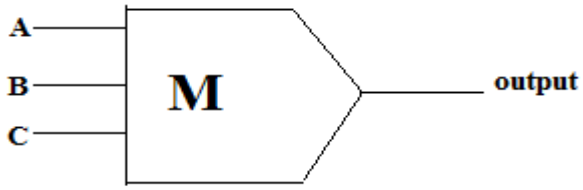

Fig: 1 Three Input Majority Logic Gate

The equation for the mg is given as follows:

$$Mg(A, B, C) = AB+BC+CA \qquad (1)$$

The truth table for the majority logic gate is shown in table1:

Table 1: Truth Table of Three Input Majority Logic Gate

A	B	C	M
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

III PARALLEL PREFIX ADDERS USING QCA

In order to avoid the disadvantages of the existing adders like ripple carry adder RCA and Carry Look Ahead adder (CLA)[2]. Parallel prefix adders are implemented. In ripple carry adder delays is more and whereas in CLA the bit complexity has been increased with increase in bit size for carry computation.

The general terminology for parallel prefix adder is

Prefix: the outcome of the operation depends on the initial inputs

Parallel: involves the execution of an operation in parallel. This is done by segmentation into smaller pieces that are computed in parallel. This is fast because the processing is accomplished in a parallel fashion.

3.1 Structure of Parallel Prefix Adders

The general architecture of parallel prefix adders has three stages [3].

1. Pre computation stage
2. Prefix stage
3. Final stage

The block diagram of parallel prefix adders is shown in figure 3

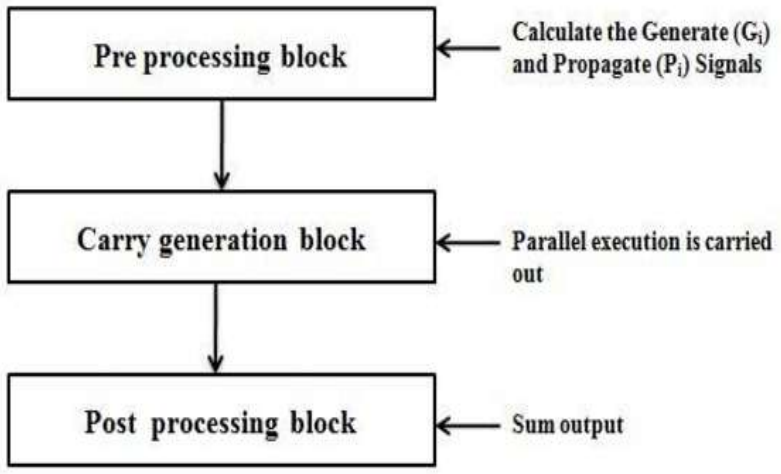

Fig 2: Block Diagram of Parallel Prefix Adders

3.2 Types of Parallel Prefix Adder

There are different types of parallel prefix adders like Kogge stone adder, Sparse Kogge-Stone adder, Spanning tree adder, Brent Kung adder, Ladner Fischer adder, Han Carlson adder. In this project Kogge Stone adder, Brent Kung and Ladner Fischer adders are used to design the multiply and accumulate unit.

3.3 Carry Generation Using Majority Logic Gates

The proposed design requires only two majority gates in all stages of prefix addition and completely eliminates the calculation of P_i and G_i. The equations for the propagation P_i and generation G_i is given as follows

$$P_i = A \wedge B; \quad (2)$$

$$G_i = A \,\&\, B \quad (3)$$

The carry C4 is computed using the prefix associative operator and the block diagram for the prefix operator used in the project and the majority logic implementation is shown in figure 3.

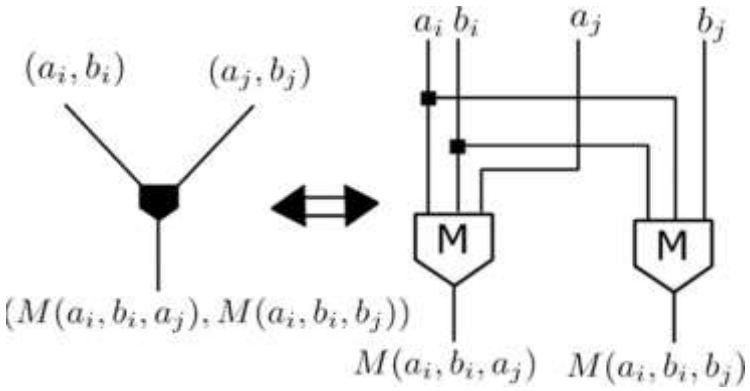

Fig 3: Prefix Operator Symbol and Majority Logic Diagram of Prefix Operator

3.3.1 Carry Generation for Kogge Stone Adder

M.Kogge and Harold S.Stone developed the Kogge stone adder. This is the parallel prefix adder which performs the fast logical addition. The block diagram for the carry generation using majority logic gate is shown in figure fig 4. It requires 3 stages and 4 majority gates for the calculation of carries.

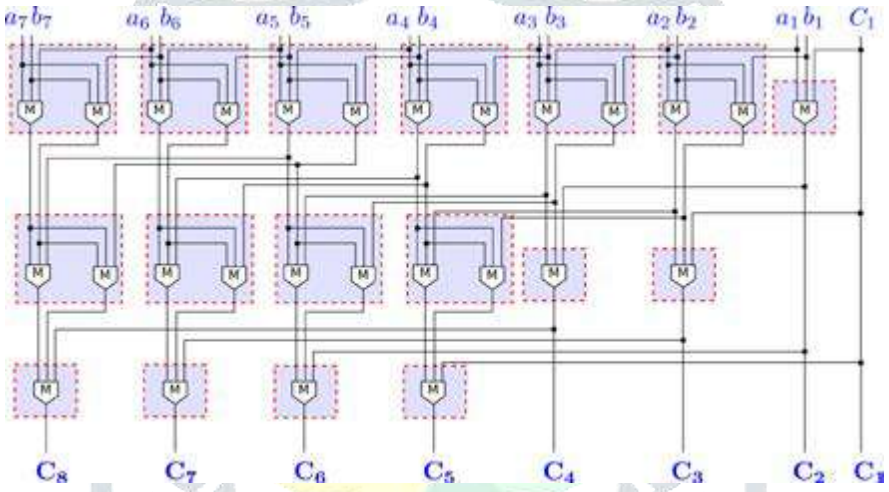

Fig 4: Majority Gate Diagram of 8-bit Kogge-Stone Adder

3.3.2 Carry Generation for Brent Kung Adder

Brent and Kung developed this parallel prefix adder. It requires 5 stages and incurs in a 6 majority gates for the calculation of carries and is shown in figure 5.

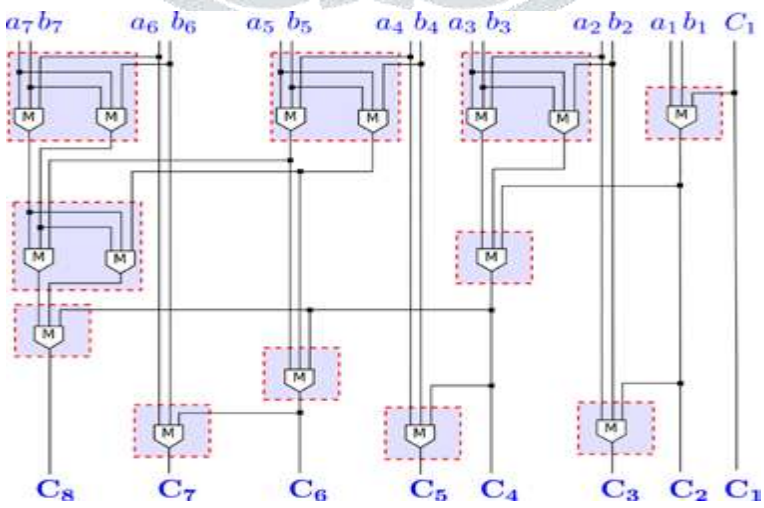

Fig 5: Majority Gate Diagram of 8-bit Brent Kung Adder

3.3.3 Carry Generation for Ladner Fischer Adder

This parallel prefix adder is developed by R.Ladner and M.Fischer. It requires 3 stages and 4 majority gates delay for calculation of all carries. The majority logic implementation for the Ladner Fischer adder is shown in figure 6

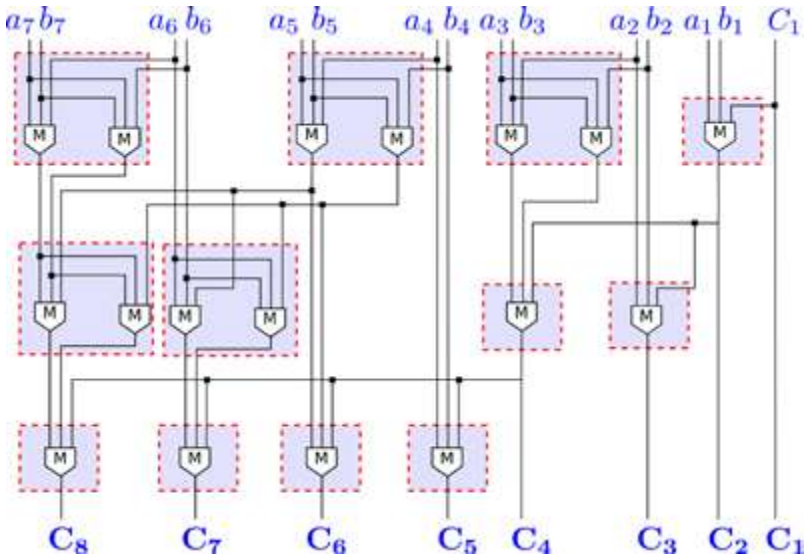

Fig 6: Majority Gate Diagram of 8-bit Ladner-Fischer Adder

IV PROPOSED METHOD

The core components in digital signal processors are multipliers and adders. The speed of the multipliers and adders largely determines the speed of the processors. The common operation of the MAC unit is, it computes the product of two numbers and adds that product to an accumulator. The general architecture of MAC unit is shown in figure7.

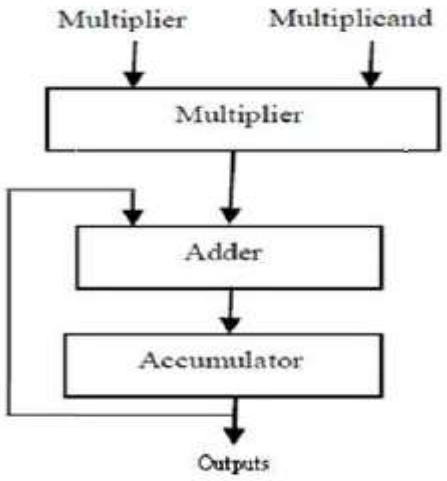

Fig 7: General MAC Unit

4.1 Multiplier

Two different multipliers are implemented in the project are Array and Vedic multiplier. An array multiplier is a digital combinational circuit that is used for the multiplication of two binary numbers by employing an array of full adders and half adders. This array is used for the nearly simultaneous addition of the various product terms involved. To form the various product terms, an array of AND gates is used before the Adder array [4].

Whereas the Vedic multiplier is used for high speed of operation as it reduces the number of partial products. In Vedic multiplier the technique is used is UrdhavTiryagbhyam. Urdhva means “Vertically” and Tiryagbhyam means “crosswise”. It is based on a novel concept, where the generation of all partial products can be done with the concurrent addition of partial products. Anyone can easily realize that this Vedic method probably makes difference for mental calculations.

4.2 Adders

Three different adders are implemented in the proposed MAC Unit. The adders that are used are Kogge Stone adder, Brent Kung adder, Ladner Fischer adders, which are designed using QCA technique as described in section III.

4.3 Accumulator

Accumulator basically consists of register and adder. Register hold the output of the previous clock from adder Holding output in Accumulator register can reduce additional add instruction. In this D flipflop is used for designing the accumulator.

V Proposed MAC Unit with Different Adders

The block diagram for the proposed MAC unit is shown in figure 8.

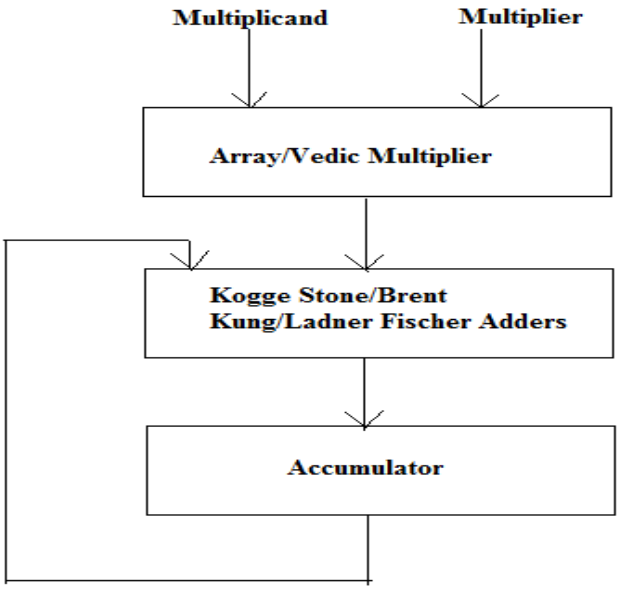

Fig 8: Proposed MAC unit using Different Adders

V. RESULTS AND DISCUSSION

The simulation result of the total MAC unit is given below figure 9. The inputs for the MAC is two 4bit input a and b and one clock and reset. For Every clock cycle the accumulator value is added to the product value as shown in the simulation results.

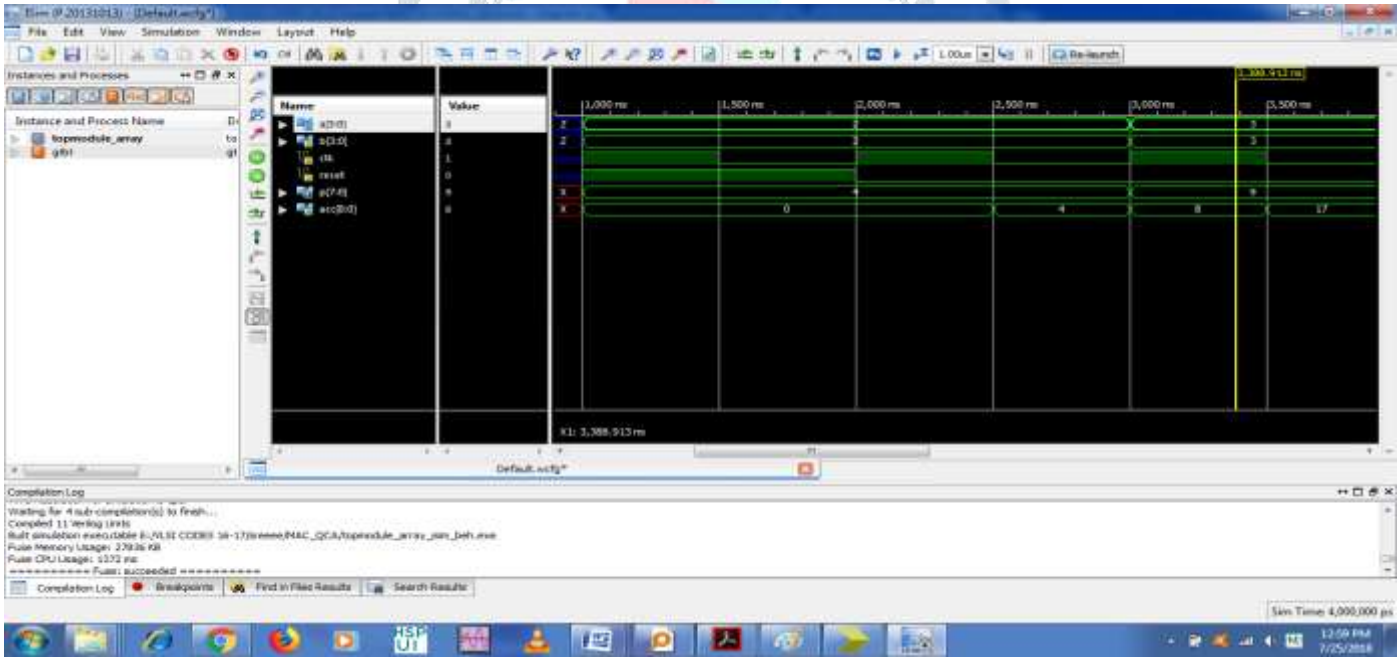

Fig 9: Simulation Results of Proposed MAC Unit

5.1 Comparison Results Parallel Prefix Adders Using Majority Logic Gates

The comparison results shows the device utilization of various parallel prefix adders such as Kogge Stone adder , Brent Kung Adder , Ladner Fischer are shown in below table 2

Family: Spartan 3
Device: XC3S50
Total number of slices available: 768
Total number of LUTs available: 1536
Total number of IOBs available: 124

Table 2: Performance Comparison of Adders Using Majority Logic Gates

PARAMETER	Ripple Carry Adder	Carry Look Ahead Adder	Kogge Stone Adder	Brent Kung Adder	Ladner Fischer Adder
SLICES	9	14	14	8	8
LUT's	16	25	25	14	14
IOB's	26	26	30	30	30
DELAY	17.585ns	13.695ns	13.313ns	15.875ns	16.122ns

The graphical representation for the delay for different parallel prefix adders using majority logic gates is shown below

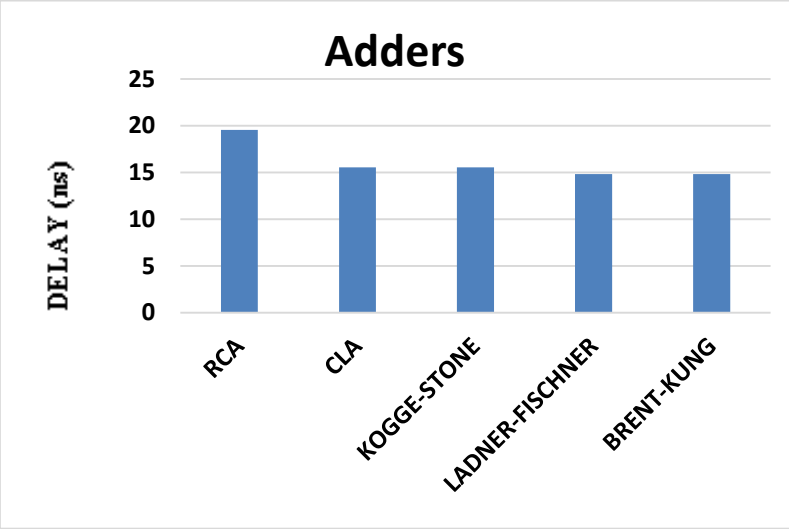

Fig 10: Delay of Majority Logic Adders

5.2 Comparison Results MAC Using Majority Logic Gates

The comparison results shows the device utilization of MAC unit using Array and Vedic Multiplier in table 3

Table 3: Performance Comparison of MAC Using Majority Logic Gates and Array multiplier

Parameter	MAC Using RCA And Array	MAC Using CLA And Array	MAC Using Kogge Stone And Array	MAC Using Brent Kung And Array	MAC Using Ladner Fischer And Array	MAC Using Vedic Multiplier And Ladner Fischer
SLICES	18	16	16	19	19	21
LUT's	32	27	27	33	33	36
IOB's	16	16	16	16	26	16
DELAY	19.546ns	15.547ns	15.547ns	14.838ns	14.838ns	16.396ns

The graphical representation for the delay for MAC unit using majority logic gates is shown below

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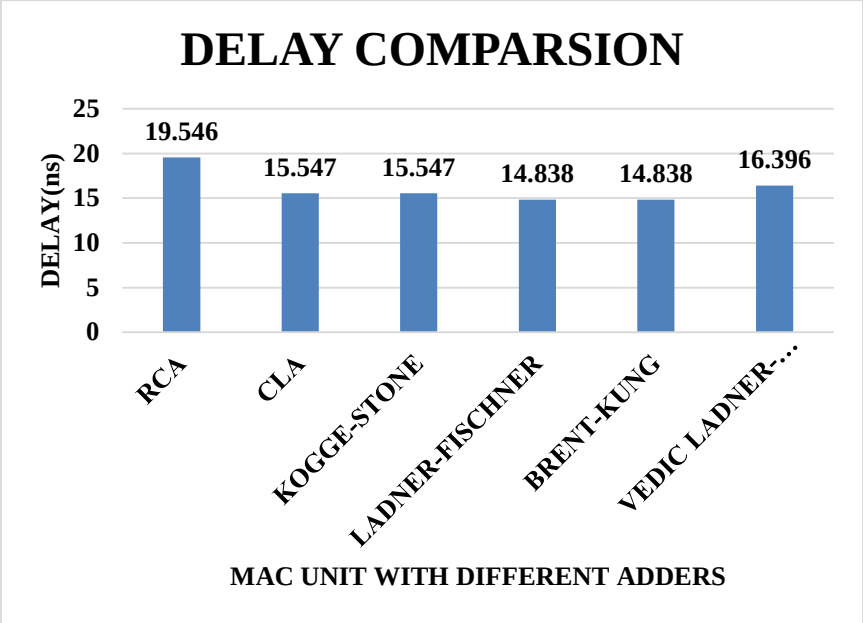

Fig 11: Delay Comparison of MAC Unit

CONCLUSION

The project has been successfully synthesized and simulated by Verilog HDL using Xilinx ISE tool. The comparison results shows that the proposed MAC unit implemented using majority logic gates are efficient in terms of delay and the delay for the parallel prefix adders using majority logic gates are having less delay when compared with the existing adders Ripple carry adder RCA and carry look ahead adder (CLA).

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