

Performance Analysis of O-IDMA with Tree Inter-Leavers using Various Design Topologies of Convolutional Encoder

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Abstract- Optical interleave division multiple access technologies possess good security better interference rejection capability and small probability of interception in noisy environment. Tree inter-leavers having larger memory, less power consumption and simplified design features, makes it useful to improve the quality of O-IDMA system. In present article various architecture of convolutional encoders are designed by varying the feedback connections and are tested for observing the BER performance of O-IDMA system implement on MATLAB.

Keywords- O-IDMA, Network topology, Hamming distance, Tree Inter-leaver, LLR (Long likely hood ratio).

I. INTRODUCTION

Security has long been an emerging issue in modern era digital communication systems. DSSS technologies possess channel bandwidth that complicates the process of decryption or decoding because narrow band message is spread into a wideband signal. Available multiple access techniques used in 1G/2G/3G systems has maximum data rate is nearly 72 Mbps^{1,2,3}. In 4G systems we require more data rates as compared to 72 Mbps.

In IDMA input bit streams are separated by different inter-leavers instead of different spreading codes as used in DS-CDMA. The O-IDMA system possess optical medium of transmission rather than wireless one. As we know that by using optical channel performance of system is improved in various aspect like SNR, BER as well losses. The size and structure of inter-leavers plays a significant role in deciding the performance of system. In tree inter-leaver two master random inter-leavers selected randomly. All the other tree branches which corresponds to different users are combination of these two master random inter-leavers. In this research article the design of convolutional coder is varied by changing the possible feedback connection. The best possible topology of coder design has been identified for of shift registers which BER is minimum.

II. OPTICAL IDMA SYSTEM

The block diagram of optical IDMA system shown in figure-1, having k different users, proposing single path of optical window 1550 nm. All users having converted in fixed code length, which is assumed to be low rate^{4,5}. The chip is interleaved by a chip level inter-leaver. After transmitting through the channel, the bits are reached at the receiver side.

In receiver section, after chip matched filtering, the received signal from the k users are observed. In the receiver side for multiuser detection we have used elementary signal estimator, APP and SDECs having variable iterative mechanisms. The produced LLR are further classified in two ways, one which is produced by PSE and another which is generated by DEC. The function of ESEB and APP decoders are based on users.

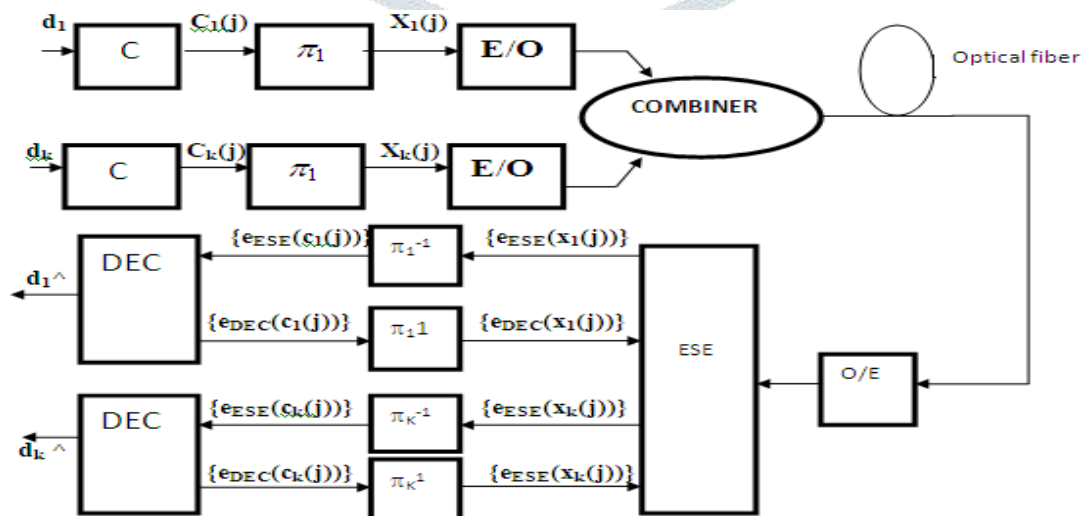


Figure -1: Optical IDMA Transmitter and Receiver Structure.

III. TREE INTER-LEAVER

In case of tree inter-leaver method, two randomly selected master inter-leavers are taken. These inter-leavers possess orthogonally property. The first condition between two chooses inter-leavers ensures the minimal cross correlation between other generated user-specific inter-leavers, using tree inter-leaver generation algorithm^{6,7}. Depending upon data length initially two master inter-leaver are selected randomly. According to the number of users the level of tree is decided, for sake and simplicity we have taken only 14 users which gives the level as 2L where L=2. The various combination of user is separated by 4 on odd and even branches of tree and arranged as shown in figure 2.

Upper branch is selected for odd number of users that is 1, 3, 5...etc. while 2, 4, 6.....etc. is chosen for even users and are counted on lower branches of tree.

In Figure 3, two master sequences are used here so we have to generate two random position sequences for two users all other users are interleaved according to these sequences. Random position setter (RPS) block 1 will create the first sequence and random position setter (RPS) block 2 will provide the second sequence. The LCU block will receive the position from temporary register through RPS block. The LCU block loops the master sequences according to the user number.

These loop count with user block will give the positions that has to be interchanged to the swapper bank.

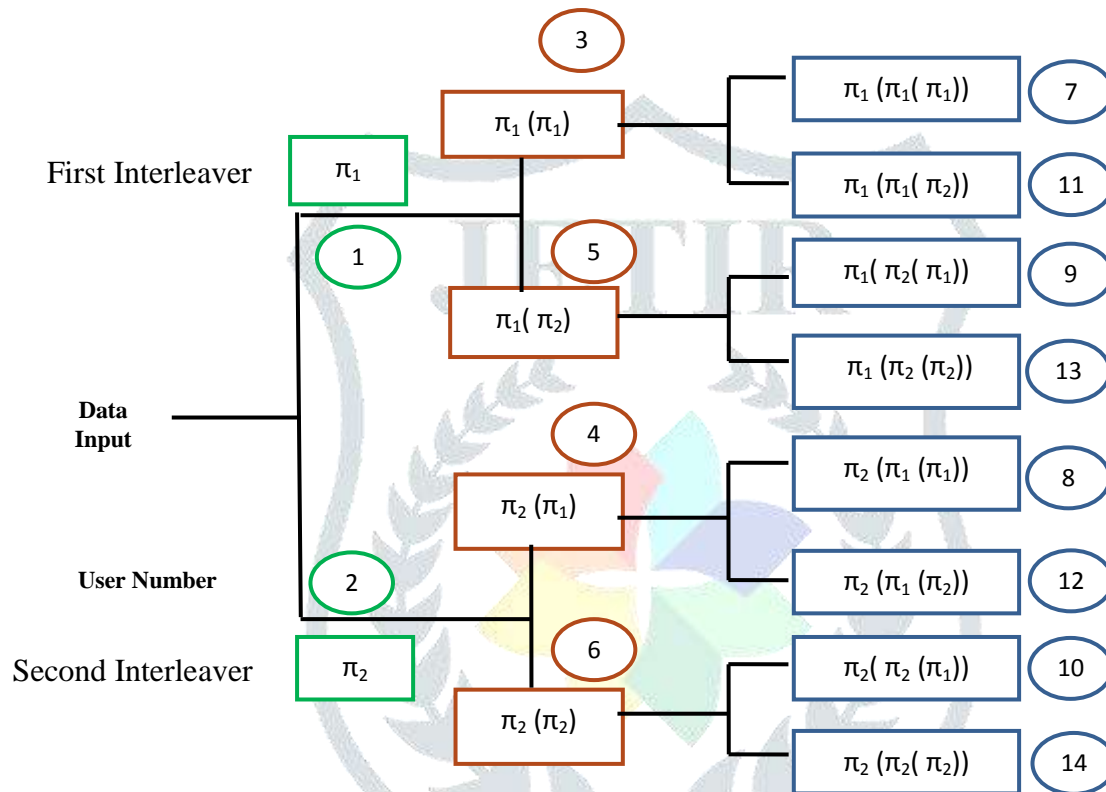


Figure 2: Tree Based Interleaving scheme.

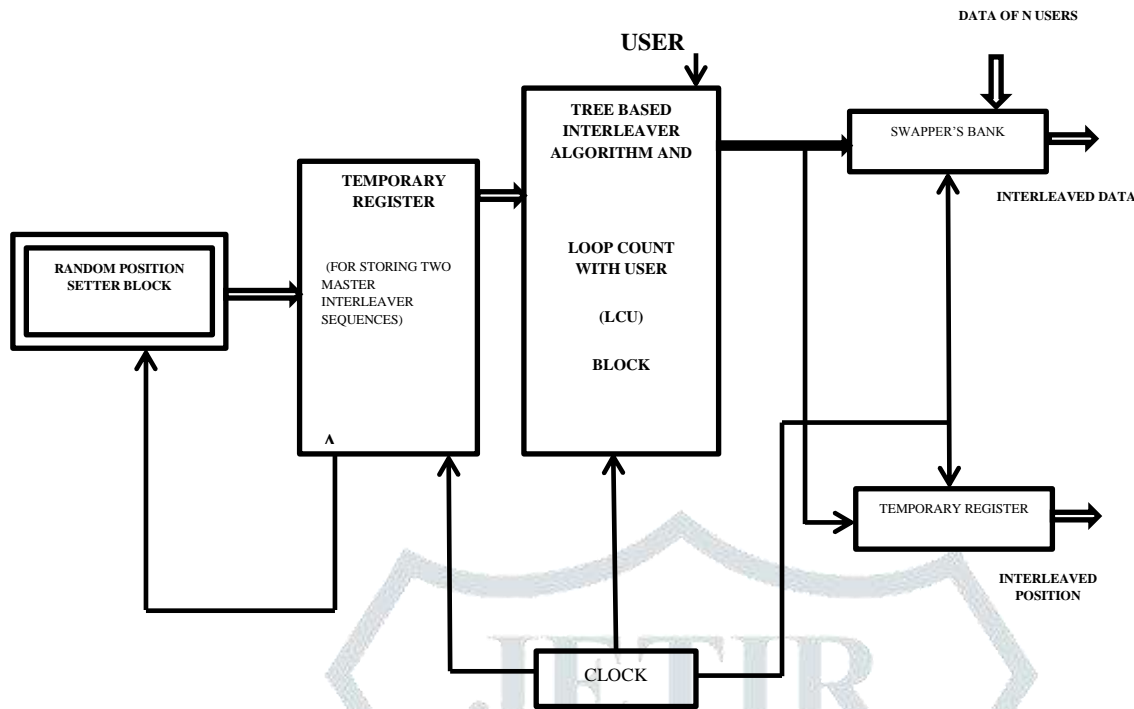


Figure 3: Block diagram of tree inter-leaver

IV. CONVOLUTIONAL CODING

Convolutional codes are used for error correction purpose in mobile and satellite communication. Each k bit code word is lengthened into n bit code words with the help of memory elements and combinational circuits. Code rate is defined as the ratio between k and n . n will totally depend on number of EX-OR gates used in encoder.

It is a measure of the efficiency of the code. Generally, k and n parameters range from 1 to 8, m from 2 to 10 and the code rate from $1/8$ to $7/8$ except for deep space applications where code rates as low as $1/100$ or even longer have been in employment. Here, the quantity, L is called the constraint length of the coder.

The constraint length L denotes the number of bits in the encoder memory that affect the generation of the n output bits. The constraint length L is also referred to by the capital letter K , which can be confusing with the lower case k , which represents the number of input bits.

V. Design of Convolutional Encoder

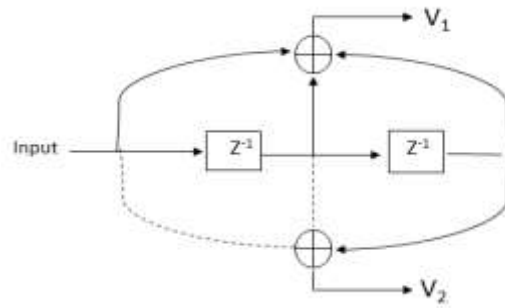
In designing of convolutional encoder there are two prime constraints. First one is number of memory elements and another one is number of EX-OR gates used in encoder circuit. The constraint length L of a encoder is well-defined as number of shift registers where only one message bit can affect the encoder output, designed as $L = m + 1$, where m represents number of memory elements or shift registers used. As more numbers of shift registers are used in encoder more number of output bits are influenced by single bit, which reduces the chance of error in deciding input bits at receiving side. If we increase the number of adders at output then more number of uncorrelated bits as well as code words produces at output, which increases the d_{\min} (minimum hamming distance) between code words and increases the error correcting capability of encoder.

VI. Network Topology Variation of Coders

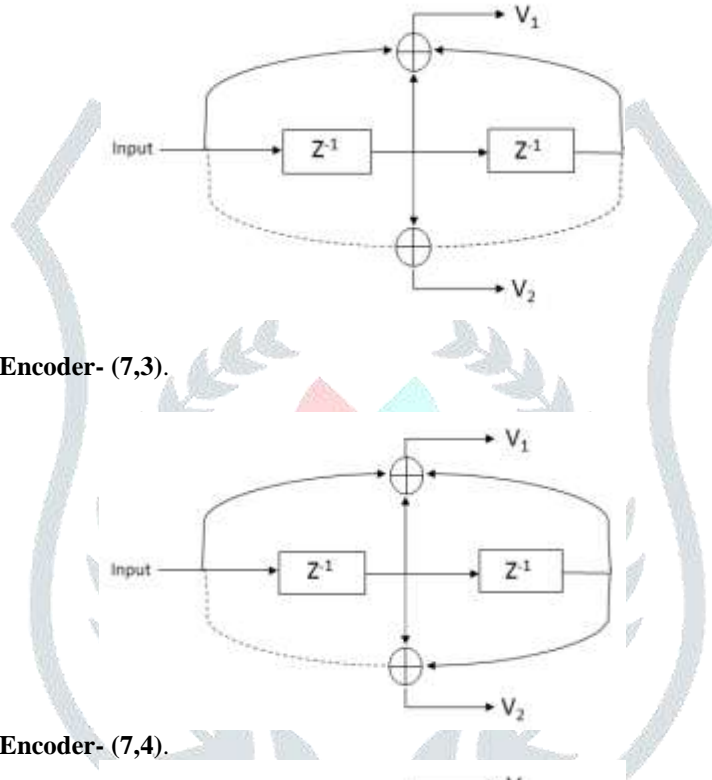
Network topology is the schematic description of a network arrangement connecting various nodes (Sender & Receiver) through lines of connection^{10,11}. In other words, network topology is the arrangement of various network elements used in data transmission and formations of interconnection like node and link with each other.

Variation of network topology means changing the different connections from the input to output and changing the feedback path from fixed hardware component of a convolution encoder. By altering the different possible connection from the memory elements and adders used in convolutional encoder, the number of loops in network topologies are changed. By using various connections and feedbacks in all possible permutations of network topologies the node and loops and possible signal flow graph is changed. In present example of (1,2) convolutional encoder with two shift register and two adder (fixed), one can draw all possible network topology combinations like (7,1) (7,2) up to (7,7) shown in fig. By adding or deleting various paths from input to output these possible topologies are designed. We have introduced all these different network architectures in OIOMA system and evaluated BER for each case. By finding the result of BER in each cases., we have derived the optimum network architecture which will give the best result i.e. minimum value of BER, among all.

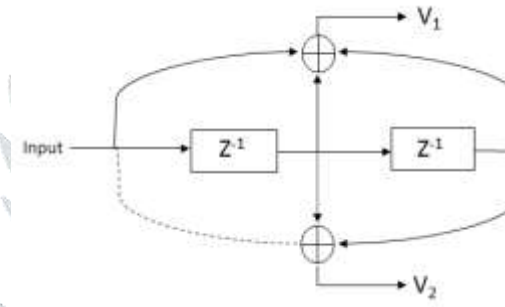
Network topology -1. Convolutional Encoder- (7,1).



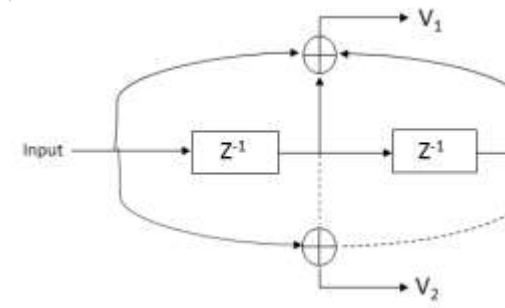
Network topology -2. Convolutional Encoder- (7,2).



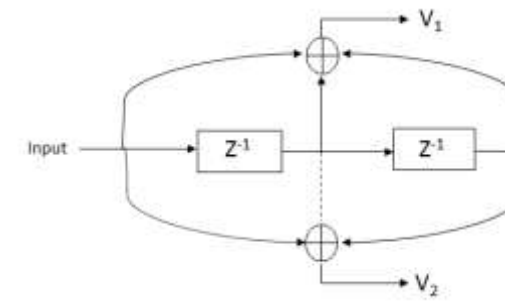
Network topology -3. Convolutional Encoder- (7,3).



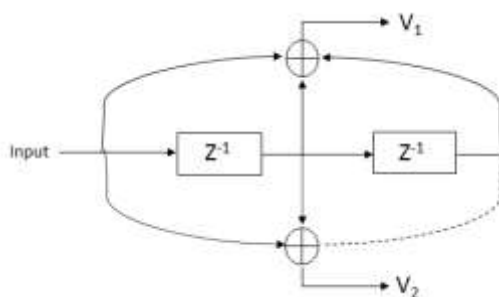
Network topology -4. Convolutional Encoder- (7,4).



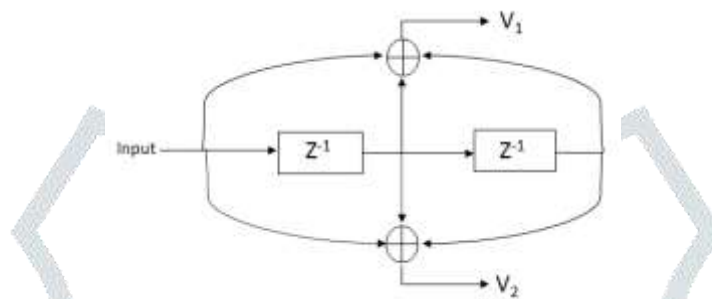
Network topology -5. Convolutional Encoder- (7,5)



Network topology -6. Convolutional Encoder- (7,6).



Network topology -7. Convolutional Encoder- (7,7).



VII. SIMULATION RESULT AND DISCUSSION

The O-IDMA has been implemented on MATLAB programming. The various blocks like encoder, spreader, inter-leavers and optical channels receiver, de-inter-leaver and decoder blocks are programmed collectively to implement whole IDMA system. The input parameters are being fixed as spread length = 16, data length = 512, constraint length L = 3 and block = 50 for fixed users = 100, inter-leaver is tree and channel is optical having source wavelength 1330nm.

In table – 1, BER performance for block = 50 with all possible seven network topologies of convolutional encoder has been shown. The results show that network topologies 4 and 5 having better result comparative to all topologies. The network topology 4 has the second best result that is 3.1402×10^{-5} but it is not considered because it avoids the ethos of hardware design since adds V_2 has no connection to shift register Z_2 . The topology 5 having result 2.1034×10^{-6} is best and optimum one since it satisfies all the design parameter of encoder. So optimum network topology which is considered for design is (7, 5).

The result for table – 2 which is measured for all the same input parameters as in table – 1 but having block is doubled that is 100. The results also suggest the same trend as in table – 1 that is minimum result of BER for topology 4 and 5 where 4 is discarded due to its design constraints and 5 will be treated as optimum one with BER 1.9531×10^{-7} . If we compare this result with [table – 1, BER for topology 5 (2.1034×10^{-6})] it shows improvements which clearly correlates the theoretical aspects that is increasing the block produces more number of uncorrelated words and reduces the BER significantly.

Table-1

Tree Inter-leaver, Convolutional [1,2] Encoding, Spread Length (S.L.=16), Data Length (m)=512, Constraint Length (L) = 3 and block =50 for fixed users = 100				
Network Topology	Generator G_1 G_2	G_1	G_2	B.E.R.
1	(7,1)	111	001	1.4102×10^{-4}
2	(7,2)	111	010	6.7578×10^{-5}
3	(7,3)	111	011	1.2070×10^{-4}
4	(7,4)	111	100	3.1402×10^{-5}
5	(7,5)	111	101	2.1340×10^{-6}
6	(7,6)	111	110	5.3125×10^{-5}
7	(7,7)	111	111	0.0158

Table -2

Tree Inter-leaver, Convolutional [1,2] Encoding, Spread Length (S.L.=16), Data Length (m)=512, Constraint Length (L) = 3 and block =100 for fixed users = 100				
Network Topology	Generator G ₁ G ₂	G ₁	G ₂	B.E.R.
1	(7,1)	111	001	1.3730×10^{-4}
2	(7,2)	111	010	8.5937×10^{-5}
3	(7,3)	111	011	1.1309×10^{-4}
4	(7,4)	111	100	2.1034×10^{-5}
5	(7,5)	111	101	1.9531×10^{-7}
6	(7,6)	111	110	7.4805×10^{-5}
7	(7,7)	111	111	0.0145

VIII. CONCLUSION

The observed results for table – 1, shows that minimum BER obtained for topology 5 which is 2.1340×10^{-6} while it reduces to 1.953×10^{-7} for table – 2 network topology – 5. The improvement of result in table – 2 clearly suggest the fact that as block length is more, the value of encoded bits per sample value is more which increase the SNR and reduces BER. If the number of hardware component in encoder design increases the results may be improved. Overall we concluded that by using tree inter-leaver in OIDMA system and if encoder design is considered in network topology – 5 modes, minimum BER is obtained and such type of systems may be used in future mobile and wireless systems.

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