OPTIMIZATION OF MAC UNIT USING FULL PIPELINED ACCUMULATOR: A REVIEW

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Abstract : With the rapid advancements in real time signal processing and digital signal processing, low power and high throughput circuitry plays a vital and challenging role for the designer. For a high performance digital signal processing system it is essential to have a MAC unit with gigantic speed and enormous throughput. The fundamental motivation of this work is to examine the full pipelined multiplier/ accumulator architecture and circuit design techniques which are suitable for achieving high throughput and with low power consumption. MAC unit comprises of multiplier, adder and accumulator/register. MAC based on the existing techniques has high delay due to accumulator without being affected by the large scale research and models. Henceforth, in this proposed framework we incorporated Carry Save Adder (CSA) technique considering various parametric constraints to assure the feasibility, efficiency and effectiveness in comparison with the existing methods. In a pipelined MAC unit, the delay estimation will assist in identifying the overall delay of the pipelined MAC unit. Many researches on the multiplier architectures including array, parallel and pipelined multipliers validates that pipelining is the most widely used technique to reduce the propagation delays of digital circuits. Therefore, the main motivation of this research is to investigate fully pipelined multiplier/accumulator architecture and circuit design technique which is suitable for implementing high throughput signal processing algorithms and at the same time achieve low power consumption**.**

IndexTerms **-** Multiplier & accumulator (MAC), floating point, booth multiplier, vedic multiplier, array multiplier, verilog HDL.

I. INTRODUCTION

Every digital signal processor contains MAC unit. The MAC unit does the multiplication and accumulation processes continuously in order to perform repeated complex operations in digital signal processing. Multiplication-and-accumulate operations are the basics for digital filters. Therefore, the functionality of the MAC unit ensures high-speed filtering and other processing necessary for DSP applications. Since the MAC unit operates fully independent of the CPU, it can execute data separately and thereby reduce CPU load. A major application like optical communication systems which is based on DSP, require extremely fast processing of large amount of digital data. A MAC unit comprises of a multiplier and an accumulator containing the sum of the previous successive products. The MAC inputs are achieved from the memory location and given to the multiplier block. The existing MAC unit models reviewed are designed using Verilog HDL, simulated and synthesized using Xilinx.

Several methods for optimization of multiplier accumulator (MAC) unit have been proposed in the recent literature. This paper reviews various methods to reduce the power consumption, increasing speed, reducing CPU load and implementing a fast multiplication network. However, there is a huge variety of techniques to implement MAC unit for overcoming the limitations of earlier methods implemented. This paper provides a comprehensive review of the major techniques and an intense classification based on speed, power requirements and efficiency.

II. LITERATURE SURVEY

M.Nasiruddin, Dr. Prashant Sharma, Dr. Vijay Chaurasia [1], *"Implementation of optimized multiplier-accumulator (MAC) unit with vedic multiplier and full pipelined accumulator: a review*" presented a brief discussion on the concept of vedic multiplier with reviewing the various existing methods to implement vedic multiplier for accumulator design. It displays that Vedic mathematic is a fast and efficient method. 'Urdhva Tiryagbhyam Sutra' and Nikhilam Sutra' multiplication methods are used in this work.

Meenu S Ravi, R H Khade and Ajit Saraf [2] describes in their paper entitled *"Design of Fast Floating Point Multiply Accumulate Unit using Ancient Mathematics for DSP Applications.*", a floating point multiply and accumulate unit implemented using ancient mathematics that lessens the number of partial products to be added simultaneously increasing the speed of accumulation of partial products by reducing the number of stages of partial products that is required to be added for making it a high performance unit.

Shaik. Mahaboob Subhani, L.Srinivas Reddy [3], *"Design and Implementation of 64-bit MAC Unit for DSP Applications using verilog HDL"* in this paper, they proposed a high speed MAC adopting the new SPST implementing approach. This multiplier

and accumulator is designed by equipping the Spurious Power Suppression Technique (SPST) on a modified Booth encoder which is controlled by a detection unit using an AND gate. The modified booth encoder will reduce the number of partial products generated by a factor of 2. The SPST adder will avoid the unwanted addition and thus minimize the switching power dissipation.

P. SivaNagendra Reddy, M. Saraswathi [4], *"Design and Implementation of FPGA based 64-bit MAC unit using vedic multiplier and reversible logic gates"* describes Multiply and Accumulate Unit using Vedic Multiplier and DKG reversible logic gates. The Vedic multiplier is implemented by using Urdhava Triyagbhayam sutra and the adder design is done by using reversible logic for performing high speed operations.

K.Prashanth, Shanigarapu Naresh Kumar, B.Pragathi [5], *"Implementation of MAC unit using efficient adders*" uses a 64 bit modified Wallace multiplier which has low delay, this design can be used in the system which needs high performance in processors involving large number of bits of the operation. The MAC unit is designed using Verilog- HDL and synthesized in Behavioral RTL Compiler.

Annapurna Band Tiwari, Saurabh Sharma [6], *"Design and development of hybrid MAC based on CSCS"* incorporated Carry Save Adder (CSA) technique along with several parametric constraints to ensure the feasibility, effectiveness and efficiency of the proposed framework in comparison with the existing methods. The novel structure of CSA exploits the radix-2 based 1's complement with benefits of altered Booth's algorithm hat address the sign expansion while minimizing the bits requirement based on operation constraints.

Weizhen Wang, Jun Han, Jielin Wang, Xiaoyang Zeng [7], *"A SIMD Multiplier-Accumulator Design for Pairing''* shows the detailed architecture of the finite field SIMD MAC unit done with the help of modular reduction algorithms with performance evaluation analysis of their design.

S.Ahish, Y.B.N. Kumar, Dheeraj Sharma, M.H.Vasantha [8], "*Design of High Performance Multiply-Accumulate Computation Unit"* featured the design and implementation of MAC unit by using Verilog coding has been presented. The MAC unit discussed can perform 16-bit unsigned operations. In this work, the multiplier is realized by using different bit-width Carry-Lookahead Adder (CLA) and Brent-Kung adder. The MAC unit implemented with the multiplier using the proposed partial product reduction block achieves better delay, power and area performance when compared to MAC unit consisting of the conventional Booth Multiplier.

Sumit C. Katkar, Prof. Pragati Kene, Prof. Shubhangini Ugale [9], *"Design of efficient 64 bit MAC unit using vedic multiplier for DSP applications – A review"* proposed a MAC unit which reduces the area by reducing the number of multiplication and addition in the multiplier unit by making efficient use of vedic multiplier.

Nagaraj Krishna Naik, Durga Bhavani.A [10], *"VLSI design of low power MAC unit"* gives detailed insight on one bit adder, four bit multiplier and registers considering power consumptions which are verified using CADENCE VIRTUSO tool of 180nm CMOS technology and the design is compared with the normal design implemented.

Prof.Tariquzzaman, Prof. M. Nasiruddin [11], *"Design of High Speed and Low Power MAC Unit with Vedic Multiplier and Full Pipelined Accumulator"* proposes the technique of low power MAC unit with Vedic Multiplier and full pipelined accumulator to boost the speed and reduce power dissipation.

Harish Babu N, Rajeev Pankaj N [12], *"Design of High Speed MAC Unit"* implemented radix-4 technique to reduce power consumption and delay when compared to other techniques while making the use of booth recoding table for obtaining partial products by using carry select adder.

Maroju SaiKumar, D. Ashok Kumar, Dr. P. Samundiswary [13], *"Design and Performance Analysis of Multiply-Accumulate (MAC) Unit"* detailed about various multipliers such as unit model is designed by incorporating the various multipliers such as Array Multiplier, Ripple Carry Array Multiplier with Row Bypassing Technique, Wallace Tree Multiplier and DADDA Multiplier in the multiplier module and the performance of MAC unit models is analyzed in terms of area, delay and power.

Tinju Tresa, M. A.Shameem, Sandeep Sreedharan [14*], "High Performance MAC Unit for FFT Implementation"* proposed an efficient way of implementing a Fast Fourier Transform (FFT) processor using high performance pipelined Multiply and Accumulate (MAC) unit. The multiplication unit is implemented using Modified Radix 4 Booth Multiplier algorithm.

Shaik. Masthan Sharif , D.Y.V.Prasad [15], *"Design of Optimized 64 Bit MAC Unit for DSP Applications"* gives detailed view about MAC unit implemented using Vedic multiplier and the addition is done with ripple carry Adder .The components are reduced by implementing Vedic multiplier using the techniques of Vedic Mathematics that have been modified to improve the performance.

G. Priyanka, D. Poornachandra Reddy [16], *"Implementation of MAC Unit by using Modified Wallace Multiplier For DSP Applications"* presented in International Journal of Scientific Engineering and Technology Research. This paper describes an efficient implementation of a high speed parallel multiplier using both these approaches. Here two multipliers are proposed. The first multiplier makes use of the Radix-4 Booth Algorithm with 3:2 compressors while the second multiplier uses the Radix-8 Booth algorithm with 4:2 compressors.

Vaijyanath Kunchigi, Linganagouda Kulkarni , Subhash Kulkarni [17]*," 32 bit Mac unit design using vedic multiplier"* presented in International Journal of Scientific and Research Publications presents Multiply and Accumulate (MAC) unit design using Vedic Multiplier, which is based on Urdhva Tiryagbhyam Sutra. The paper emphasizes an efficient 32-bit MAC architecture along with 8-bit and 16-bit versions and results are presented in comparison with conventional architectures. The proposed MAC unit reduces the area by reducing the number of multiplication and addition in the multiplier unit. Increase in the speed of operation is achieved by the hierarchical nature of the Vedic multiplier unit. The proposed MAC unit is implemented on a field programmable gate array (FPGA) device.

Soniya, Suresh Kumar [18], *"A Review of Different Type of Multipliers and Multiplier-Accumulator Unit"* presented in International Journal of Emerging Trends & Technology in Computer Science (IJETTCS). In this paper, different types of techniques are presented for improving the speed and low power consumption like pipelined booth multiplication technique in which pipelining is used in booth multiplier to reduce the delay of each stage.

HE Jing-yu, LI Li-li, ZHU Yan-chao, YANG Wen-tao, YANG Jian-hong [19], *"Multiply-Accumulator Using Modified Booth Encoders Designed for Application in 16-bit RISC Processor"* published in 2nd International Symposium on Instrumentation and Measurement, Sensor Network and Automation (IMSNA). This paper, multiply-accumulator (MAC) is designed for application in simple 16-bit RISC processors to enhance the processor's capability by adding new instruction set. The MAC involves 16x16 bit multiplier using modified Booth encoders and the accumulation result is stored in two 16-bit register-pair. The multiplier consists of Booth algorithm, Wallace tree and carry look-ahead adder (CLA). The RISC processor in this paper is a 16-bit pipelined RISC processor using Harvard architecture and the pipeline consists of the instruction fetch unit, decode unit, the front-end logic execution unit, arithmetic execution unit and register access unit.

Shaik Nasar, K. Subbarao [20], "*Design & Implementation of MAC Unit Using Reversible Logic"* presented in International Journal of Engineering Research & Applications. The main aim of the proposed system is to design a MAC unit using reversible logic with least number of gates, number of garbage outputs, delay and quantum cost in order to prove it as an efficient design.

Shanthala S, Cyril Prasanna Raj, Dr. S.Y. Kulkarni [21], *"Design and VLSI Implementation of Pipelined Multiply Accumulate Unit"* presented in IEEE Transactions on Second International Conference on Emerging Trends in Engineering and Technology, ICETET-09" aims to investigate various pipelined MAC architectures and circuit and the design techniques which are suitable for the implementation of high throughput signal processing algorithms. The goal of this project was to design and VLSI implementation of pipelined MAC for high-speed DSP applications at 180nm technology.

Conventional MAC Unit

Multiplication Accumulation is an important part of real-time digital signal processing (DSP) with applications ranging from digital filtering to image processing. Multiply and accumulate is a very common basic-level operation seen in many DSP designs/algorithms. Two numbers are multiplied together, and added into an accumulator register [18]. MAC are the building blocks of the processor and has a great impact on the speed of processor [17].The conventional MAC unit comprises its working in three steps:

1. Multiplication of multiplier & multiplicand
2. Addition of generated partial products
3. Computation of final multiplication

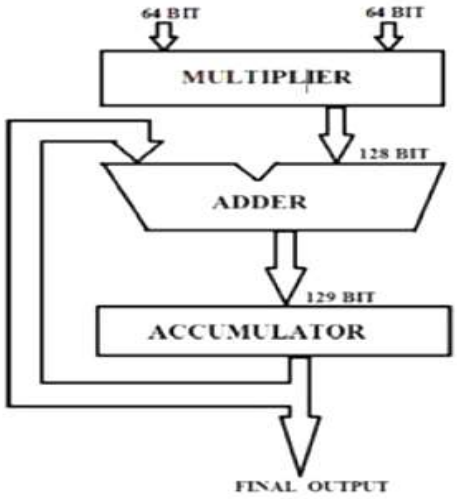

Fig. 1: Basic architecture of MAC unit

Some multipliers used in MAC unit are mentioned below:

Floating point multiplier

Floating point is a way to represent numbers and do arithmetic in computing machines, ranging from simple calculators to computers [16]. Floating point multiplication is similar to integer multiplication. Since floating point numbers are stored in sign magnitude format, the multiplier needs to work only on the unsigned integer numbers.

Wallace tree multiplier

A wallace tree multiplier is an appropriate hardware implementation of a digital circuit for multiplication of two integers. It consists of afore mentioned three step process :

1. The bit product terms are generated after multiplying the bits of multiplicand and multiplier.
2. The bit product matrix is reduced to lesser number of rows using half and full adders, till the last addition remains this process is continued.
3. Final addition using adders is done to obtain the result.

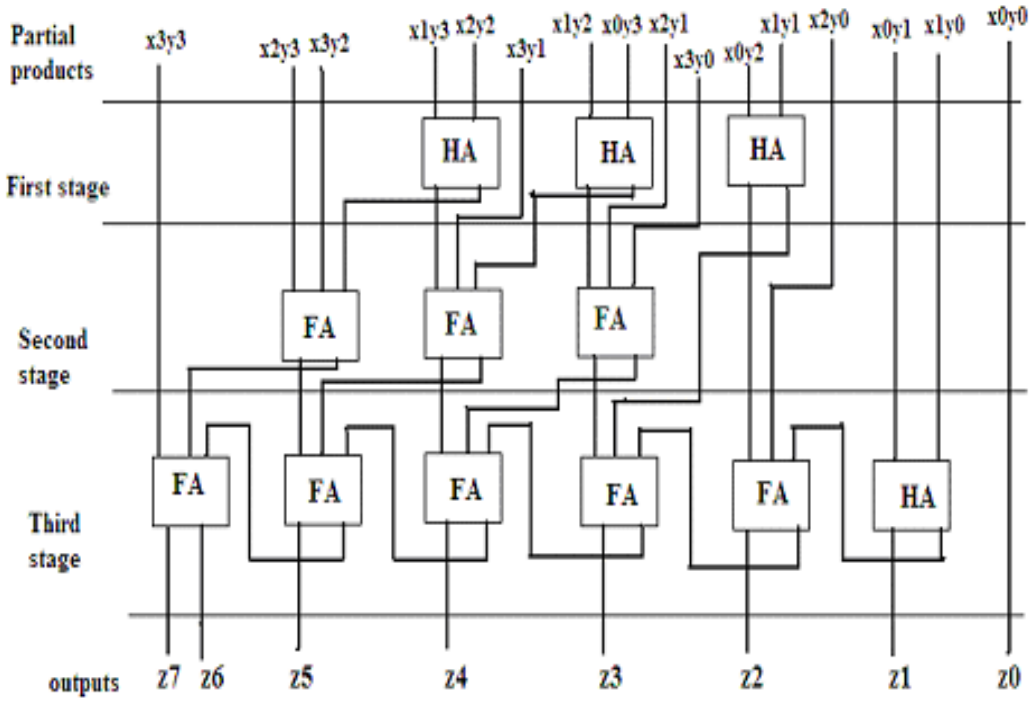

Fig. 2: Wallace tree multiplier

Modified Wallace multiplier

A modified Wallace multiplier is an efficient hardware implementation of digital circuit multiplying two integers. Generally in conventional Wallace multipliers many full adders and half adders are used in their reduction phase. Half adders do not reduce the number of partial product bits. Therefore, reducing the number of half adders used in a multiplier reduction will lessen the complexity. Hence, a modification to the Wallace reduction is done in which the delay is the same as for the conventional Wallace reduction [5].

Vedic Multiplier

The main purpose of Vedic Mathematics is to be able to solve complex calculations by simple techniques. The formula being very short makes them practically simple in implementation. Urdhva-tiryagbhyam (Vertically and crosswise) sutra is general formula applicable to multiplication operation. Its algebraic principle is based on multiplication of polynomials. The Vedic multiplier using Urdhva-tiryagbhyam sutra of width NXN will generate the 2N-1 cross products of different widths which when combined forms (log2N + 1) partial products. The partial products are obtained by vertical and crosswise operations using the Sutra. Hence the delay is equal to adder delay. Critical path would consist of adders adding the maximum number of bits in cross product [18].

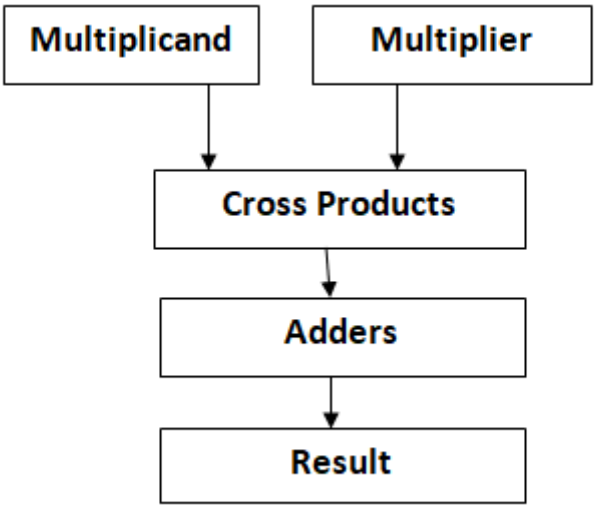

Fig. 3: Architecture of Vedic Multiplier

Booth Multiplier

The Booth multiplier is also known as Recoded booth multiplier, in which the multiplicand is kept as it is and the multiplier is recoded as a recoded multiplier and then the multiplication is done with multiplicand and recoded multiplier. To reduce the number of partial products in the multiplier, the Multiplier uses Radix 2*r* multipliers, which produces *N/r* partial products, each of which depends on *r* bits of the multiplier. Fewer partial products lead to a smaller and faster CSA (Carry Save Adder) array [18].

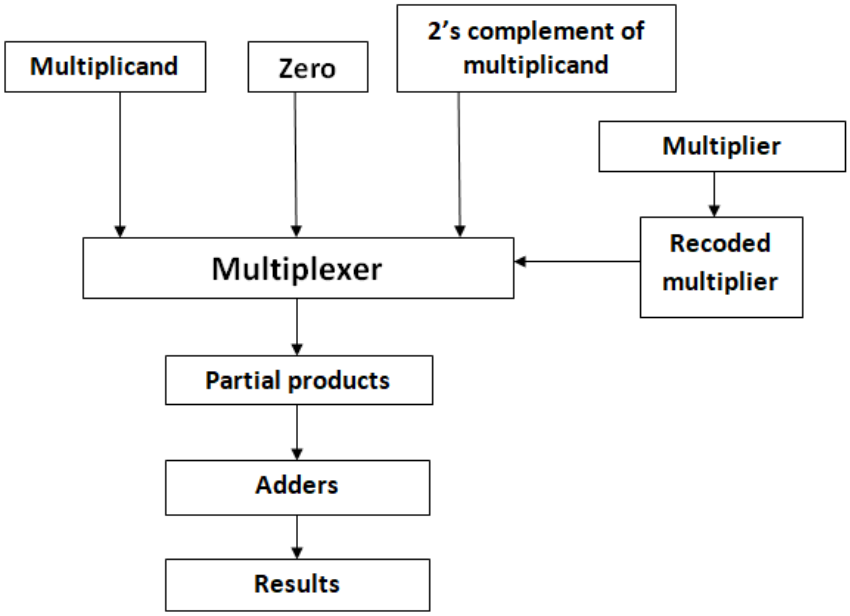

Fig. 4: Architecture of Booth Multiplier

Array multiplier

Array multiplier is well known due to its regular structure. Multiplier circuit is based on repeated addition and shifting procedure. Each partial product is generated by the multiplication of the multiplicand with one multiplier digit. The partial product are shifted according to their bit sequences and then added. The summation can be performed with normal carry propagation adder. N-1 adders are required where N is the no. of multiplier bits [17].

III. RESULTS AND DISCUSSION

In most of the Digital signal processing (DSP) applications, the evaluative operations usually involve many multiplications and /or accumulations. So, for real time signal processing applications, high throughput multiplier –accumulator (MAC) plays the role of a key element to attain a high-performance digital signal processing application. In the past few years, the main consideration of MAC design is to increase its speed. Since speed and throughput rate determines a systems performance they are always the concerns of digital signal processing systems. However due to the vast advancements in portable electronic products, low power designs also become another important consideration. Presently, multiplication time is still the dominant factor in deciding the instruction cycle time of a DSP chip. Higher throughput arithmetic operations are important to obtain the desired output in many real time signals and image processing applications. One of the major arithmetic operations in such applications is multiplication and the development of a fast multiplier circuit has been a subject of interest over decades. Therefore, it is required to design a low power high speed MAC unit.

IV. CONCLUSION

In this paper, a review of various multiplier systems for the designing of MAC unit have been analyzed. A comparative literature survey of various efficient multipliers is done so as to fulfill various parameter requirements such as high speed, low delay, low power consumption and high throughput. We have seen in this paper numerous techniques along with several parametric constraints are worked upon to ensure the feasibility, effectiveness and efficiency of the existing methods.

V. REFERENCES

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