Efficient implementation of double error detection and correcting OLS codes

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Abstract:There is a growing interest in multi-bit Error Correction Codes (ECCs) to protect SRAM memories. This has been caused by the increased number of multiple errors that memories suffer as technology scales. To protect an SRAM memory, an ECC has to be decodable in parallel and with low latency. Among the codes proposed for memory protection are Orthogonal Latin Square (OLS) codes that provide low latency decoding and a modular construction. It is more effective to provide different degrees of error correction for the different bits. This is done with Unequal Error Protection (UEP) codes. In this paper, UEP codes are derived from Double Error Correction (DEC) Orthogonal Latin Square (OLS) codes. The results show that the implemented with lower decoding delay is reduced 30% than traditional SEC-DED codes and with a cost similar to that of both DEC OLS and SEC-DED codes. The Proposed encoder and decoder are done by Verilog HDL and Simulated and synthesized by Xilinx 14.3 tool.

Keywords-- OLS cods, SEC-DED codes, OS-MLD codes, UPE codes.

I. Introduction

There are several sources of errors that affect modern electronic circuits, such as manufacturing defects, circuit ageing, electromagnetic disturbances or radiation induced soft errors. Many different techniques can be used to either prevent failures from occurring or to detect and correct them. Those include modifications to the manufacturing process, circuit level and logic level techniques. Techniques at different levels are commonly combined to achieve the desired reliability target.

In error-correcting codes, parity check encompasses an easy way to detect errors along with a sophisticated mechanism to work out the corrupt bit location. Once the corrupt bit is found, its value is reverted (from zero to one or one to zero) to urge the original message. To detect and correct the errors, extra bits are super imposed to the data bits at the time of transmission. The extra bits are referred to as parity bits. They permit detection or correction of the errors. The data bits in conjunction with the parity bits form a code word.

Traditionally, the ECCs used to protect SRAM memories have focused on providing Single Error Correction and Double Error Detection (SEC-DED). However, as electronic technology scales, there is an increased number of multiple bit errors. For example, for radiation induced soft errors, the percentage of errors that affect more than one memory cell has increased with each technology node. To correct multiple bit errors, more advanced ECCs are needed. Although there are many such codes, most of them do not fit the needs of an SRAM memory. To be used with an SRAM memory, encoding and decoding need to be done in parallel in less than one clock cycle. However, most multi-bit error correction codes are serially decoded or require complex decoding circuitry when the decoder is implemented in parallel. This is for example the case of Bose Chaudhuri Hocquenghem (BCH) codes, for which a parallel decoder requires complex circuitry. However, there is a property called "one step majority logic decodable" (OS-MLD) that only a few ECCs have, that makes them suitable for fast parallel encoding.

The rest of the paper is organized as follows. New designs of OLS encoder and decoder are presented in Section II. Section III details the software requirement Section IV provides the simulation results for the OLS encoder and decoder. Section V gives the conclusion.

II. BLOCK DIAGRAM

A. Encoder for the Proposed (48, 16, 16) DEC OLS Code Single Extended With SEC-DED

The encoder can be implemented as a combination of the DEC-OLS and SEC-DED encoders. DES OLS Encoder its Consist of Sixteen 4 input XOR Gate Design. The Inputs are Combination d and Outputs are Co. Another side we have SEC DED Encoder, It Consist of Four 3 Input XOR Gate design in Four Blocks. Both Encoders results are connected to two inputs XOR Gate and the Parity bits are generated. Parity Bits are named as C. This is illustrated in Figure 1. Basically, the encoders can operate in parallel and the final parity check bits are obtained doing the xor of the DEC-OLS results, (co bits in the Figure) and SEC-DED results, (ce bits in the Figure)

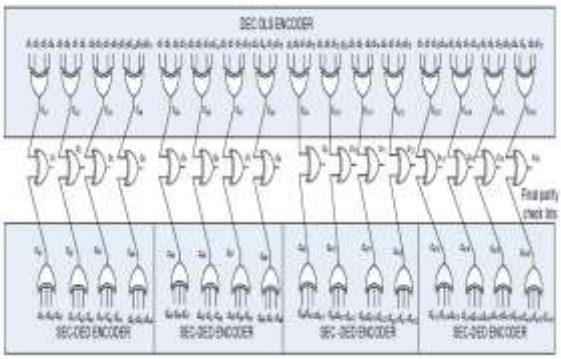

Fig 1 .Encoder for (48,16,16) DEC OLS code extended with SEC-DED.

B. Decoder for the Proposed (48, 16, 16) DEC OLS Code Extended With SEC-DED

The Proposed Decoder Consist of Three Major Units like Syndrome Computation OLS Majority Voters and SEC DED Block.

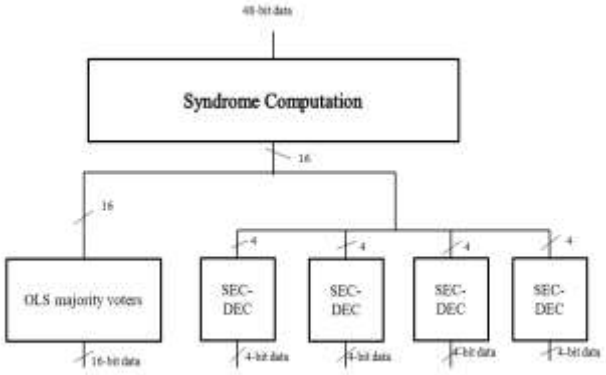

Fig 2 .Decoder for (48,16,16) DEC OLS code extended with SEC-DED.

C. **Syndrome Computation Unit**

For the syndrome computation, the parity prediction can be implemented by checking that the following two equations take the same value

r1 = s1 ^ s2 ^ s3 ^ ▪ ▪ ▪ ^s2tm

r2 = c1 ^ c2 ^ c3 ^ ▪ ▪ ▪ ^c2tm

Where si are the computed syndrome bits.

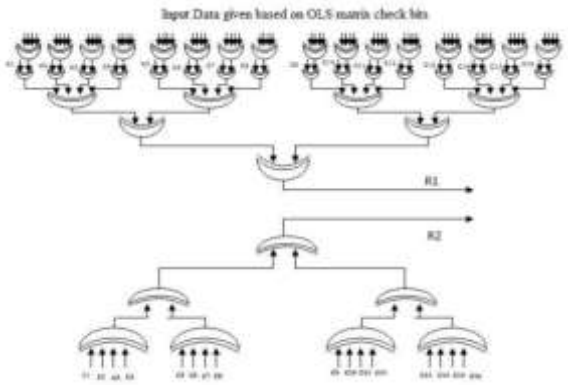

Fig 3. Syndrome Computation

if a fault occurs in the checker, the outputs are 01 or 10 otherwise output is 00 or 11.Based on the syndrome bits error correction is done at decoder.

C. OLS Majority Voter

The OLS Majority Voter it Consist of Four Input Majority Gate and Xor Gate. The syndrome bits (s bits in the Block Diagram) are then used as inputs to the OLS majority voters that determine if the correction is needed for the OLS data bits (d bits in the Block Diagram). The syndrome bits that correspond to each of the sub-blocks are also compared with the SEC-DED syndrome patterns to determine if a correction is needed on the SEC-DED data bits (de bits in the Block Diagram). The Majority Gate Design is Consist of Four 3 Input AND Gate and the results are connected into two inputs OR Gate.

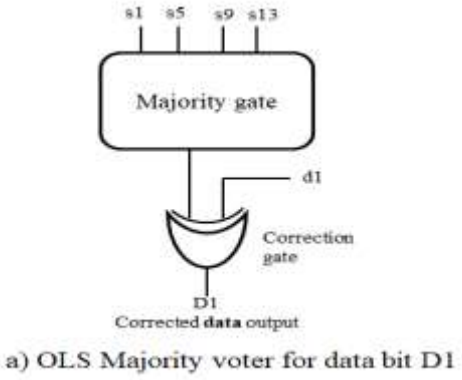

Fig 4. OLS majority voter

E. SEC-DEC Decoder

16-bit data is corrected by using OLS Majority voter. Reaming 16-bit data is corrected by using SEC-DED decoder. Based on the syndrome bits data is corrected in SEC-DED Decoder. By using both decoders we can use 16 check bits for protecting 32-bit information, same number of check bits used for the 16-bit information also.

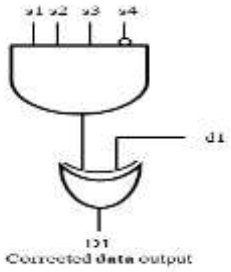

Fig 5. OLS majority voter

F. Orthogonal Latin Squares

The OLS codes were introduced decades ago to protect memories. On the end simultaneously have recently been proposed to protect caches and interconnects. The block sizes for OLS codes are k=m 2 data bits and 2tm parity bits Where t is the number of errors that the code can correct and mis an integer. For memories, the word sizes are typically a power of two and therefore mis commonly also power of two. The main advantage of OLS codes is that their decoding is simple and fast.

1) Each data bit participates in exactly 2t parity check bits;

2) Each other data bit participates in at most one of those parity check bits.

Therefore, for a number of errors or smaller, when one error affects a given bit, the remaining t −1 errors can, in the worst case affect t −1 check bits on which that bit participates. Therefore, still a majority of t +1 will trigger the correction on the erroneous bit. Conversely, when a given bit is correct, the errors on other bits will not cause miss correction as a majority of t +1 is needed.

III. SOFTWARE REQUIREMENT

Xilinx's

- Synthesis Tool
  - Xilinx ISE 14.3.

For two-and-a-half decades, Xilinx has been at the forefront of the programmable logic revolution, with the invention and continued migration of FPGA platform technology. During that time, the role of the FPGA has evolved from a vehicle for prototyping and glue-logic to a highly flexible alternative to ASICs and ASSPs for a host of applications and markets.

VI. SIMULATION RESULITS

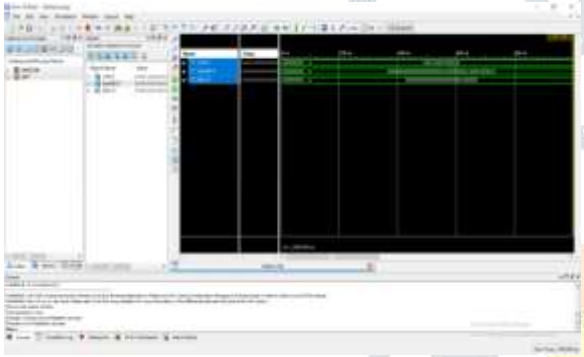

Fig 6. Encoder ouput wave forms

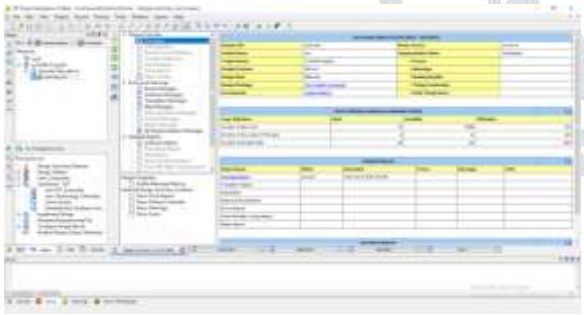

Fig 7. Encoder summery report

Fig 8. Encoder timing report

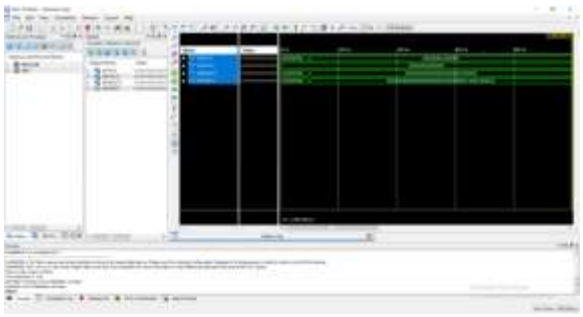

Fig 9. Decoder ouput wave forms without error

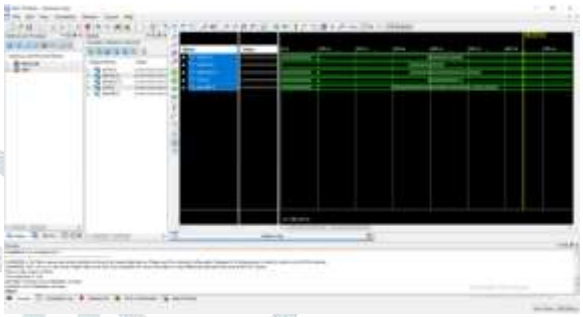

Fig 10. Decoder output wave forms with 2-bit error

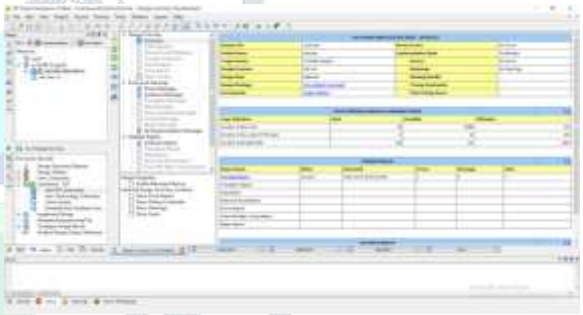

Fig 11. Decoder summery report

Fig 12. Decoder timing report

Encoder area (no. of LUTs) and delay compression:

ECC Type	data Size	LUTs	Delay(ns)
DEC OLS	16	16	0.927
SEC-DEC	32	30	1.88
DEC OLS	32	32	1.17

Decoder area (no. of LUTs) and delay compression:

ECC Type	data Size	LUTs	Delay(ns)
DEC OLS	16	32	1.728
SEC-DEC	32	64	3.52
DEC OLS	32	64	1.99

V. CONCLUSION

This paper consists two techniques to derive Unequal Error Protection (UEP) codes from Double Error Correction (DEC) Orthogonal Latin Squares (OLS) codes have been presented. The derived UEP codes can protect part of the word with DEC and the other part with SEC-DED. The codes can be decoded in parallel with low latency. By using both OLS and SEC-DEC we can use 16 check bits for protecting 32-bit information, same number of check bits used for the 16-bit information also in OLS codes. Encoding and decoding 35% delay is reduced by comparing single error correction-Double Error detection code.

Future work will consider the derivation of UEP codes from OLS codes that can correct more than two errors. For example a TEC OLS code can be extended to also provide DEC for additional bits.

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