PERFORMANCE ANALYSIS OF DOUBLE TAIL COMPARATOR USING CNTFET TECHNOLOGY IN 32nm

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***Abstract*:** This paper proposed a dynamic double tail comparator using CNTFET technology in 32nm. Simulations are carried out in MOSFET 32nm and CNTFET 32nm. In the resultant comparator average power consumption and delay are reduced. The average power and delay is improved by 24.1 % and 21.3% respectively for conventional double tail comparator MOSFET and CNTFET. For proposed double tail comparator, the CNTFET double tail comparator is improved by 22.0% in average power and in delay it is improved by 26.6%. The tool used for simulation is Synopsys HSPICE.

Keywords: Low power, Double tail comparator, CNTFET technology, High speed

I. INTRODUCTION

Today the requirement for ultra-low-power, region effective and the fast simple to computerized converters is in charge of the utilization of dynamic regenerative comparators. ADC's makes an interpretation of simple amount into computerized signals, figuring, and information transmission and control frameworks.

II. CARBON NANOTUBE FIELD EFFECT TRANSISTOR

A carbon nanotube field-effect transistor which is well known as CNTFET also introduce to as a field-effect transistor which uses a single carbon nanotube or an array of carbon nanotubes for make the channel material alternatively of a bulk silicon as we use previously in the traditional MOSFET layout. Its 1st demonstrated in 1998, there have been main considerable developments in CNTFETs.

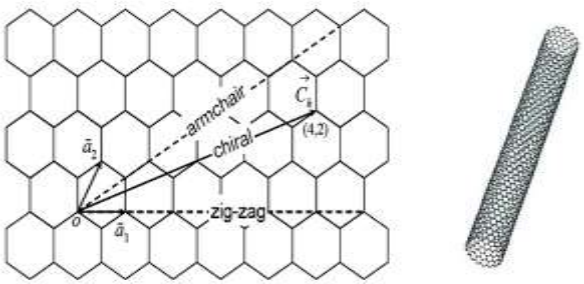

Figure 1. Carbon nanotube lattice structure

The main basic principle of working of the carbon nanotube field-effect transistor which is well known as CNFET is as similar to as the traditional silicon devices. This respected device must having three (or four) terminals of a semiconducting nanotube, and basically acting as conducting channel, which is perfectly maintaining drain and source contacts. The device is turned on or turned off electro statically thru the gate. As the quasi-1D device layout could be provides very good gate electrostatic control compared to the channel region than 3D device (for example we can mention bulk CMOS) and 2D device (for example we can mention fully drain SOI) layouts [4]. Let's talk about the device working mechanism, well known device CNFET can be classified as both the MOSFET-like FET [15][3] and also the Schottky Barrier (SB) controlled FET well-known as SB- CNFET also. However, the conductivity of SB-CNFET is mainly controlled through the majority carriers tunneling thru the SBs at the last end contacts.

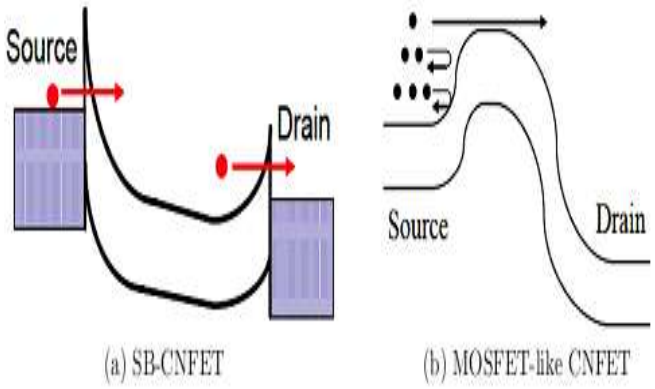

Figure 2. The energy band diagram for (a) SB-CNFET and (b) MOSFET-like CNFET

III. PROPOSED METHODOLOGY

SYNOPSYS HSPICE is the software used and the model for CNTFET is 32nm BSIM-CMG CNTFET Model. A new device can replace bulk CMOS because of the numerous advantages it offers over bulk CMOS. Along these lines, CNTFET DOUBLE TAIL COMPARATOR comes as the other option to substitute Si-bulk DOUBLE TAIL COMPARATOR. CNTFET because of two gates have better control over OFF current is used in memory array. In present scenario, memories occupy a huge part of SOC and mobile applications [3].However, design of DOUBLE TAIL COMPARATOR became more challenging in deep technology.

Due to the better performance of double-tail architecture in low-voltage applications [2], the proposed comparator is designed based on the double-tail structure. The main idea of the proposed comparator is to increase Vfn/fp in order to increase the latch regeneration speed [4]. For this cause, two control transistors (named as Mc1 and Mc2) were introduced to the first stage in parallel to M3/M4 transistors however in a cross-coupled manner.

The working operation of the proposed comparator is described as: at the time of reset phase (as CLK = 0, Mtail1 and Mtail2 are turned off, which avoiding static power), M3 and M4 pulls presented fn and fp nodes to VDD, for this reason transistor which named Mc1 and Mc2 respectively are cut off. Intermediate stage transistors, named as MR1 and MR2 respectively, reset all presented latch outputs to ground.

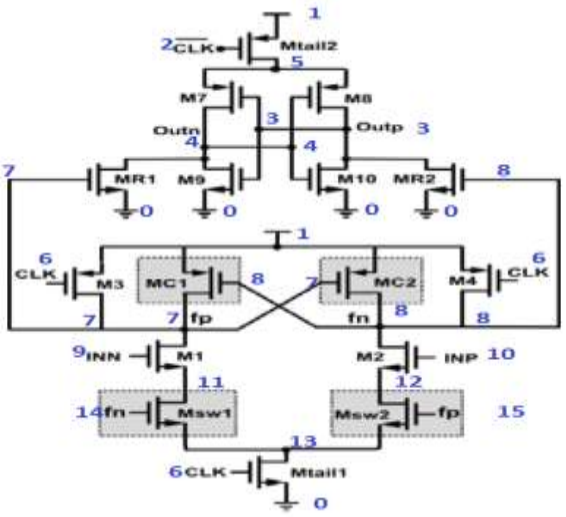

Figure 3. Proposed circuit using CNTFET

When we are in decision-making phase (CLK should be equal to VDD, and Mtail1, Mtail2 must be switched on), transistors which named M3 and M4 respectively are turned off. Additionally we can say, at the beginning of this phase, the control transistors are still off (just because fn and fp are nearly about VDD). Therefore, fn as well as fp start to drop it with different rates which generally related to the input voltages. Let suppose VINP > VINN, accordingly fn drops faster than fp, (seeing that M2 provides more current if we compare it with M1). As long as possible fn continues falling, coincide with pMOS control transistor (named Mc1 for this case) should be turned on, as pulling fp node back towards to the VDD; due to this some other control transistor (like Mc2) must be remains turned off, allowing fn to be discharged fully. In additionally, not similar to conventional double-tail dynamic comparator, which have Vfn/fp is usually just a function of the input transistor trans conductance and the input voltage difference as compared with the proposed structure as soon as possible the comparator detects that for instance node fn discharges considerably faster, and a pMOS transistor (named Mc1) should be turned on, pulling the alternative node fp move back to the VDD.

Accordingly as the time passing, the corresponding difference between the fn and fp (Vfn/fp) enhance in the exponential way, and leading to the reduction of latch regeneration time. regardless of the effectiveness of the proposed idea, one of the points which need to be considered is that in this circuit, while one of the control transistors (which named as Mc1) activates, a current from VDD is drawn to the ground thru input and tail transistor (which named as Mc1, M1, and Mtail1 respectively), resulting in static power intake. To overcome this trouble, two nMOS switches are used underneath the input transistors [named as Msw1 and Msw2]. At the 1st step of the decision making phase, due to the fact that both fn and fp nodes have been pre-charged upto VDD (at the time of the reset phase), both switches are turned off, and fn, fp both start to drop with other type of discharging rates. As quickly possible the comparator detects which one of the fn/fp nodes is discharging remarkably fast, after control transistors surely act in a way which enhance their voltage difference.

IV. SIMULATION AND RESULTS

Figure 4 and Figure 5 shows average power results of MOSFET and CNTFET based double tail comparator in conventional and proposed devices for double tail comparator.

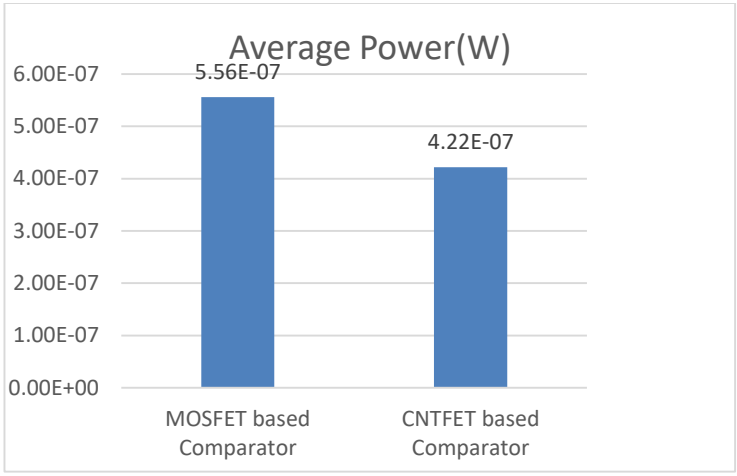

Figure 4 Average power comparisons conventional

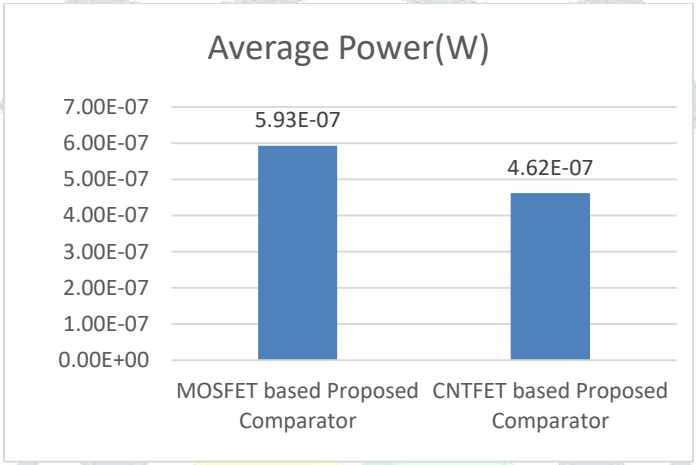

Figure 5 Average power comparison proposed

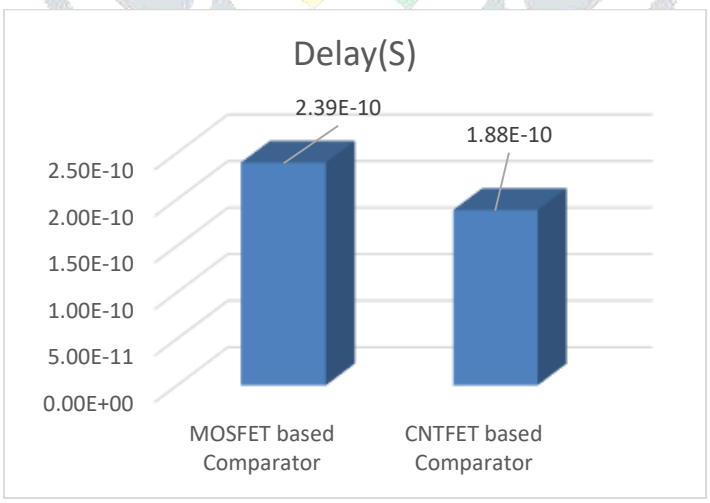

Figure 6. Delay comparison conventional

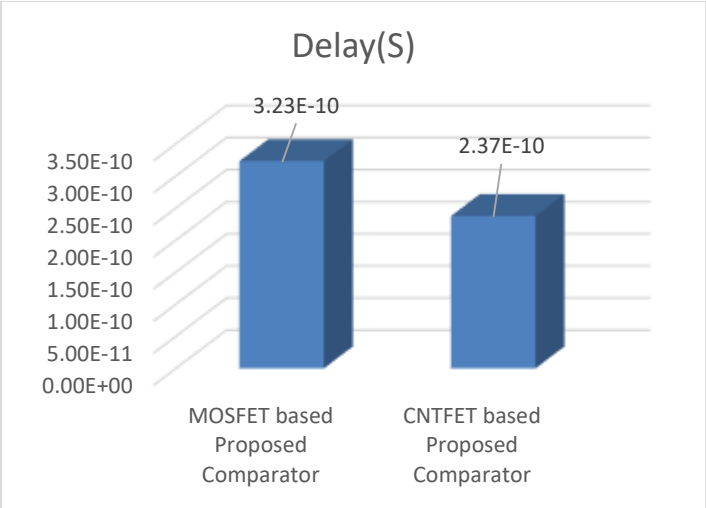

Figure 7. Delay comparison conventional proposed

Figure 6 and Figure 7 shows delay results of MOSFET and CNTFET based double tail comparator in conventional and proposed devices for double tail comparator.

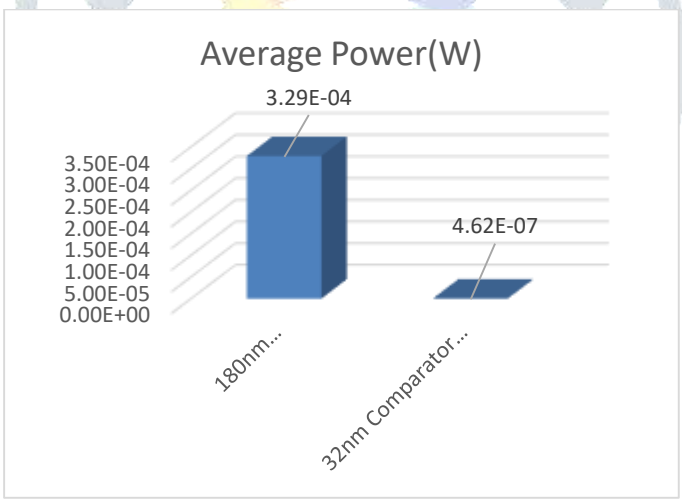

Figure 8. Average power comparison base 180 nm to 32nm

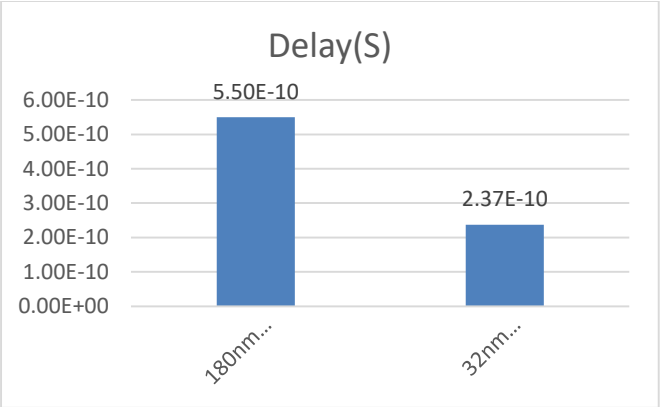

Figure 9. Delay comparison base 180 nm to 32 nm

Table1 Results of conventional comparator

Circuit1	MOSFET based Comparator	CNTFET based Comparator
Average Power(W)	5.56E-07	4.22E-07
Delay(S)	2.39E-10	1.88E-10

Table 2 Results of proposed comparator

Circuit 2	MOSFET based Proposed Comparator	CNTFET based Proposed Comparator
Average Power(W)	5.93E-07	4.62E-07
Delay(S)	3.23E-10	2.37E-10

Table 1 and Table 2 shows average power and delay results of MOSFET and CNTFET based double tail comparator in conventional and proposed devices for double tail comparator.

V. CONCLUSION

Simulations results show that double tail comparator conventional and proposed have improved speed and a lower consumption of average power. The average power and delay is improved by 24.1 % and 21.3% respectively for conventional double tail comparator MOSFET and CNTFET. For proposed double tail comparator, the CNTFET double tail comparator is improved by 22.0% in average power and in delay it is improved by 26.6%.

VI. REFERENCES

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