CURRENT-FED MULTILEVEL CONVERTERS: AN OVERVIEW OF CIRCUIT TOPOLOGIES, MODULATION TECHNIQUES, AND APPLICATIONS

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ABSTRACT

Multilevel converters (MLCs) have emerged as standard power electronic converters in high power as well as quality demanding applications. They are classified into current-fed MLCs and voltage-fed MLCs. Voltage-fed MLCs have widely researched whereas the current-fed MLCs are the recent topic of research. Based on the principle of duality between voltage and current sources, several current-fed MLCs analogous to voltagefed MLCs have been identified. Current-fed MLCs offer several advantages in terms of high power capability, transformerless operation, short-circuit protection, and excellent quality of output current waveform. The goal of this paper is: 1) to present review of circuit topologies, modulation schemes, and applications of current-fed MLCs; and 2) to review an emerging lowdevice switching frequency modulation technique known as synchronous optimal pulsewidth modulation for current-fed MLCs. The circuit configuration and advantages of each topology along with various modulation techniques are discussed in detail. Compared to voltage-fed MLCs, the operation of current-fed MLCs need to satisfy additional switching constraints. A survey of classical methods for realization of these operational constraints has been done and a new generalized method has been proposed. Finally, future scope of research has been presented to encourage further development of topologies and modulation techniques for current-fed MLCs.

Keywords: Current-fed multilevel converters, low switching frequency modulation techniques, modulation techniques, solar power integration, synchronous optimal pulsewidth modulation (SOP).

1.INTRODUCTION

The research on multilevel converters (MLCs) began with introduction of three-level neutral-point-clamped (3LNPC) converter in 1980s. Depending on the input source,MLCs can be categorized as voltage-fed MLCs and currentfed MLCs. In voltage-fed MLCs, the output voltage waveforms contain multilevel structure, whereas the current-fed MLCs generate multilevel structure in the output current waveforms . The topologies of voltage-fed MLCs such as NPC, flying capacitor (FC), cascaded H-bridge (CHB), active NPC and modular multilevel converters (MMC), have been extensively studied in the last few decades . Many of these topologies have been commercialized by number of companies and thus, it can be said that they have reached a mature stage. On the other hand, current source converters (CSCs) have been found as better option in various applications. Though CSC has slow dynamic response, they have found in application such as high power drives for fan in which fast dynamic response is not needed. For high power drives, it provides advantages of inherent four quadrant operation. Especially the regeneration mode of operation is so important in which the polarity of voltage at the converter will be reversed to transfer power back to source. For operating this mode CSC does not require any

additional circuit. Moreover the inductors in the CSC provide longer lifetime compared to capacitors as in VSC. Another notable advantage of CSCs is that it provides short circuit protection to drives as the dc link reactor limits the rate of rise of current and, hence, it improves the reliability of the drive [6]. In case of low voltage applications such as fuel cells and solar photovoltaic (PV), CSC provides inherent voltage boosting capability as the inductors in the circuit help in stepping up voltage. Moreover, the direct current control property of CSC enables grid integration without any ac current feedback control . In case of high-voltage direct current (HVDC) system, the short-circuit protection is major concern and also it requires converter that provides higher mean time between failure (MTBF). The inductors in CSC can with-stand high voltage ripple without affecting its performance and hardly suffer from degradation. Hence, the CSC provides longer MTBF which suits for HVDC application. Most of the installed HVDC systems are CSCs because of SCR semiconductors which are higher power and voltage ratings compared to VSCs. Various fully controllable CSCs have also been found in HVDC and FACTS applications . CSC also provides advantages such as independent control of the active and reactive power, the converter can be operated in weak grids or with passive loads and ac-side filters can be eliminated due to low harmonic distortion. Because of these various advantages and applications of CSC, researchers have focused on developing multilevel topologies for CSC in recent years. The basic advantage of multilevel operation with CSC topologies is high operating current capability with low or medium current semiconductor devices. Vazquez et al. surveyed the current-fed MLC topologies and classified them into embedded, two-stage and paralleled MLCs . The embedded current-fed MLCs are suitable for high current and high power applications such as super-conductive magnetic energy storage (SMES) . The paralleled current-fed MLCs with several current sources are recommended for high-power ac drives . The two-stage current-fed MLCs achieve smooth input current with less number of semiconductor devices and they are more attractive power electronic converters for solar power integration . Even though few converters have been identified in, for researchers to understand and to develop new current-fed MLCs, there is a need of complete survey of existing current-source MLCs, modulation of these classical MLCs and their applications. Hence, the contribution of this paper are as follows.

1) Identification and classification of CS MLC topologies: Provides a detailed discussion of all existing currentfed MLC topologies that are derived using duality principle from voltage fed MLCs. Highlighting their issues in the operation and listing out various suggested solutions.

2) Conversion methods: The modulation of current-fed MLC is not straightforward as compared to voltage-fed MLC. The modulation techniques are required to satisfy set of operation constraints such as continuous path for input current and output current should be defined in order to modulate the current-fed MLCs. To achieve these constraints there is need of additional conversion method in the modulation process. This paper surveys various classical conversion methods developed for CSC and also proposes a generic conversion method which can be applied for reference based modulation technique.

3) Modulation techniques: This paper surveys various classical modulation techniques that utilize different conversion methods. In addition, this paper also reviews the modified synchronous optimal pulse width modulation (SOP) technique for CS MLC that utilizes the proposed conversion method for operating current fed MLCs. The SOP stateof-the-art has been so far applied only on voltage-fed MLCs. The contents of this paper are organized as follows: topologies of current-fed MLCs are described . Several modulation techniques have been discussed and compared. Applications of current-fed MLCs are explored and finally, the future scope of research to further enhance current-fed MLCs is suggested

TOPOLOGIES AND CLASSIFICATION

Current-fed MLC topologies utilize combination of multiple inductors for splitting input current into equal parts for achieving current multilevel with the help of power semiconductor devices. Usage of current-fed MLC has been started with thyristorbased paralleled CSI at the late 1970s by Nabae et al. . Pulse width modulation (PWM)-based higher level current-fed MLC has been identified for SMES application in. Later, this topology has been referred as single-

rated inductor currentfed MLC . Following this, a generalized current-fed MLC topology has been proposed [16], which is referred as embedded current-fed MLC in . Recently, current-fed MLCs have been derived from classical voltage-fed MLCs such as CHB, FC, and NPC topologies, based on principle of duality . In addition, several other current-fed MLC topologies have been found through literature study. The classification of various current-fed MLC topologies is shown in Fig. 1 and more details about each topology will be given next.

The current-fed MLC topologies are operated from either single source or multiple sources. The topologies of singlerating inductor, multi-rating inductor, and paralleled H-bridge current-fed MLC topologies are obtained from classical voltagefed MLCs by using principle of duality. These topologies are suitable for applications such as active filter , power converters for grid-connected PV panels , fuel-cell power grid integration , wind energy conversion , SMES AC motor drives, and HVDC applications . A detailed discussion about various current-fed MLCs including emerging topologies is given next.

Single-Rating Inductor MLC

A seven-level (7L) topology of single-rating inductor MLC is shown in Fig. 2(a) and it consists of three modules for producing 7Ls (±Idc , ±2Id c 3 , ±Id c 3 , and 0) in the output current waveform. It could be extended to any number of output current levels by adding more modules. If the number of modules in the converter is denoted as S, then the output current will have 2*S+1 levels. Because of this modularity nature, this topology has been treated as MMC in . However, it differs from conventional voltagefed MMC in terms that these modules share load current equally among modules irrespective of modulation index whereas in the voltage-fed MMC the load current is shared by few modules and the remaining modules are stopped at lower modulation range .

Each module in the single-rating inductor MLC contains three phase legs with top and bottom inductors, and each leg has one top and bottom semiconductor devices. The inductors reduce the current ripple of the module and also provides equal impedance among phases. The diodes are connected in series with switches to provide unidirectional current flow and bipolar voltage blocking capability. The converter has been named as single-rating inductor Multilevel current source converter (MCSC) by Zhihong Bai because input dc current is distributed equally among the inductors and, hence, all the inductors are of same current rating . This converter is identified as dual of voltage-fed diode-clamped MLC. If the five-level (5L) configuration of this topology with the fully controlled switches are replaced by half-controlled thyristors then the topology resembles multiple current source inverter invented by Nabae in 1977 and later in 1995 Uchino has patented this topology which has gate turn-off thyristors (GTO) . The notable advantages of the single-rating inductor topology are increased current capacity, reduction of conduction losses as the current through devices are reduced, meeting harmonic standards without the need of expensive filters, etc. . The major issue with this converter is balancing inductors currents of modules otherwise the unequal current increases the output total harmonic distortion (THD) and introduces loworder harmonics which require higher value of capacitor for filtering them out. A carrier-phase-shift modulation technique can be adopted to overcome this issue by swapping carrier waves on consecutive fundamental cycles . However, this approach cannot be applied for higher levels as the increase in number of levels results in increased swapping periods. In a vector-based inductor current balancing has been achieved for 5L converter by utilizing redundant vectors, however, this methodology increases the complexity for higher levels as the number of redundant vectors is increased. The module current balancing control methodology approached by these modulation techniques is focused on controlling current flowing in the top inductor with the assumption that both the top and bottom inductor current are same. However, the imbalance in inductor currents within a module has been studied in , and proposed a novel method for balancing inductor currents. This method utilizes zero vectors for balancing when there is a deviation in the inductor currents and output filter capacitor voltage. This also brings additional damping for the resonance raised from inductor–capacitor filter. The another limitation with the singlerating inductor MLC topology is the more number of inductors and, hence, the size of converter will be bulkier. The

inductors count within a module cannot be reduced in order to keep the advantage of power balancing. Palaniappan et al. have suggested improvement of 5L configuration of this topology by wounding two top inductors in one core and two bottom inductors in another core which was termed as interphase inductors as shown in These interphase reactors on single-rating inductor MLC help in reducing the overall size of the converter by four times . In normal scenario, the inductors in the modules face the switching frequency of the semiconductor but with this interphase reactors the switching frequency faced by the module inductors get twice and, hence, the overall volume is reduced .

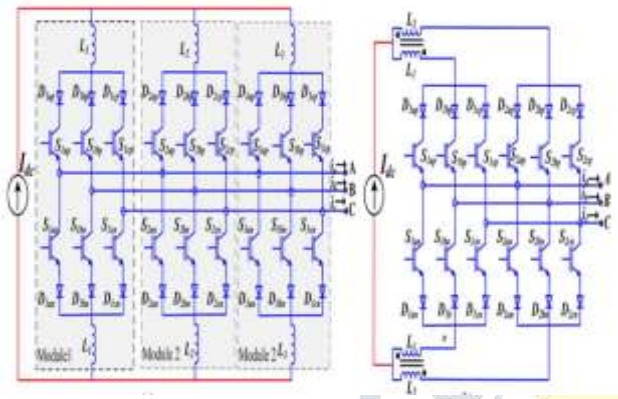

Fig. 1. Single-rating inductor MLC. (a) 7L inverter (b) 5L inverter with interphase inductors.

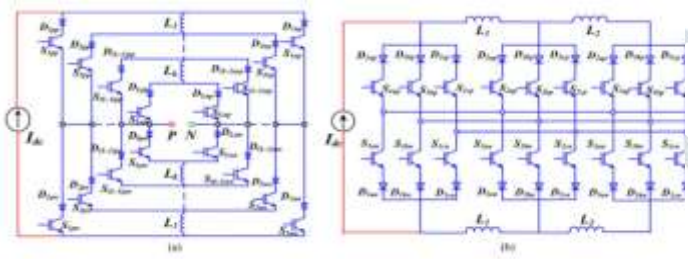

Fig. 2. Multi-rating inductor MLC. (a) Single phase (embedded). (b) Three phase

has been derived from parallel commutation cells identified for dc–dc converters by making use of inductors as current sources. The two sets of parallel commutation cells are reoriented and one set is connected to positive rail and another one for negative rail to derive single-phase multilevel current source inverter. The single phase multi-rating inductor MLC is also named as embedded MLC as in and the arrangement of inductors with semiconductor devices The topology utilizes intermediate inductors that split input current into multiple currents at different magnitude, thus avoiding the need for isolation coupling transformer . The converter can be operated at low-frequency modulation to achieve an output current with some harmonic elimination. To make sure there is equal current distribution among switches, the duty cycle and resistance of semiconductor devices has to be same. To ensure this requirement, two switching strategy has been identified . One is symmetric switching strategy which operates the semiconductor devices with 50% duty cycle and achieves the current balance within two cycles. However, if this strategy applied for higher level converters then the inductors current ripple will increase which may cause the imbalance in the current among semiconductor devices. This has been avoided using asymmetric switching strategy which provides unequal duty cycle among semiconductor devices and achieves current balancing within a fundamental period. This strategies ensure current balancing under open-loop condition, however, for higher levels of this topology, it needs higher computation in identifying the balancing situation. a generic combination strategy has been framed for single-phase multi-rating inductor MLC for L-level which utilizes four steps to achieve zero inductor voltage, 50% conduction period of each switch, and minimum current ripple on inductors . The four steps involve determination number of combinations (2L−1), populating states of switches that are connected to output phase terminal (Sipn , Sipp , where i = 1, 2, 3,...,L) for each combination, identifying output current and voltage states, and finally the combination sequences with minimum frequency is selected with a computation algorithm. The three phase version of this multi-rating inductor has been developed in and the topology which can produce 32∗L number of switching combinations.

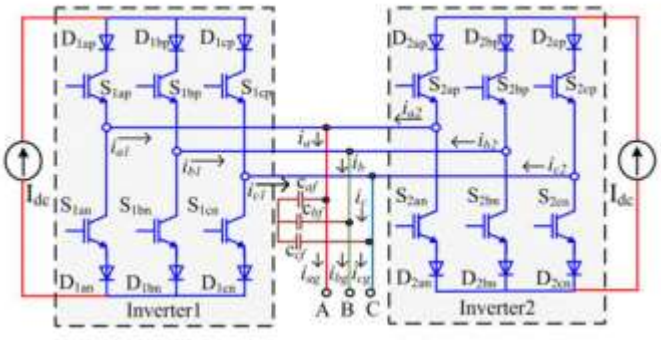

Fig. 4. Paralleled H-bridge MLC.

Similar to single-phase version of multi-rating MLC, the inductor current balancing is one of the key issue in the three phase version of multi-rating inductor MLC. Though the fundamental frequency switching method explains about the inductor current balancing based on developing combination table, the dynamic performance study performed in shows that a slight variation in the resistances of the inductor will cause imbalance and it requires load impedance domination to nullify the effect of differences in resistance of the inductors. The another way to avoid the effect of inductor resistance mismatch is either by choosing appropriate modulation technique or by developing closed-loop techniques . Since this topology is a dual of FC voltage-fed MLC, the natural current balancing approach by a carrier phase-shift method has been applied and verified in a closed-loop control is proposed by utilizing redundant switching states for balancing the inductor currents. The voltage across intermediate inductors is fed back to the controller for determining the state selection. In case of converter modulated with Space vector modulation (SVM), a vector-based current balancing is achieved by choosing zero vector based on the polarity of the voltage across intermediate inductor. Another notable issue in the multi-rating converter is the number of semiconductor devices, a modified version of this topology has been proposed in for achieving same performance of conventional multi-rated converter at the cost of increased current

Paralleled H-Bridge MLC

The first type of paralleled H-bridge MLC was introduced by Palaniappan during 1979 using thyristors and called it as dual CSC for ac drives applications . Later, it is identified as dual of voltage-fed CHB VMLC . It could also be observed that the paralleled H-bridge topology MLC resembles the single-rated MLC. However, it differs in the sense of independent current sources whereas single-rating MLC uses single dc source and, hence, the parallel H-bridge MLC does not face circulating current and current imbalance issues . However, deriving multiple current sources is another complex task. Especially in drive applications, these dc current sources need to be obtained from multiple current source rectifiers with phase-shift transformer. Hence, equal dc currents can be obtained by controlling the rectifier which avoids imbalance issue and also the inverters can be operated with fixed gating patterns . This combination of rectifier and parallel inverters have been treated as modular CSC, however, for consistency in nomenclature this topology is referred as parallel H-bridge MLC in this paper. The complete switching operation of 5L-paralleled H-Bridge converter can be referred from . A 7L converter of this topology has been suggested for super high-power ac drives (>20 MW) as in , in which multiple dc current sources are obtained through 18 pulse transformer with identical SCR rectifiers.

Another well-known resources of multiple current sources are solar PV application, and parallel H-bridge MLC is a suitable candidate for this application . However, the PV sources produce unequal dc currents due to partial shading and varying insolation. Under such variation, the parallel H-bridge output current will have low-order harmonics. To handle unequal currents a closed-loop controller with modulation strategy is needed for keeping output ac current within required THD standards the combined current control with dq-frame control strategy using carrier-phase-shift-modulation technique has been approached to handle unequal currents. This control strategy has achieved seventh-order harmonic elimination, better output quality waveforms even at low switching frequency with inexpensive capacitive filter . In another paper space vector-based strategy has been approached to operate converter under unequal input currents. In this approach, two methods of selecting switching state vectors has been obtained and the low-frequency pulsation in the dc-link voltage has been eliminated for achieving better THD. Another notable issue with this converter

topology is the resonance due to inductor and filter capacitor which will introduce the lower order harmonics in the output current. The resonant issue has been overcome in by introducing active damping in the controller design using a virtual resistor. The main disadvantage of this topology is the requirement of many isolated dc-current sources in terms of ac drive applications. This results in bulky, complex, bigger inductors, and high-cost isolation transformers . However, in case of solar applications, the space is not constraint and also there is no need for transformers as the solar power is obtained through multiple PV sources. For ac drive application, Kwak and Toliyat have proposed a modified version of this topology by replacing one PWM CSI module by load-commutated inverter (LCI) module . The modified topology combines semi controlled LCI as one module and fully controlled GTO inverter as another module. By doing so, the advantage of soft switching in LCI module is achieved and in addition the combination has also reduced the filter size and overall cost.

Emerging Multilevel Topologies

Developing new current-fed multilevel topologies has become main focus by various researchers for reducing the number of passive and active devices, to apply duality principle in obtaining current-fed MLC from well-established voltage fed MLCs and also to increase the reliability of the converter. 1) Two-Stage MLC: One of the emerging topology is a twostage MLC which is also named as boost MLC. The single-phase configuration of this topology is shown in Fig. 5(a). It is made

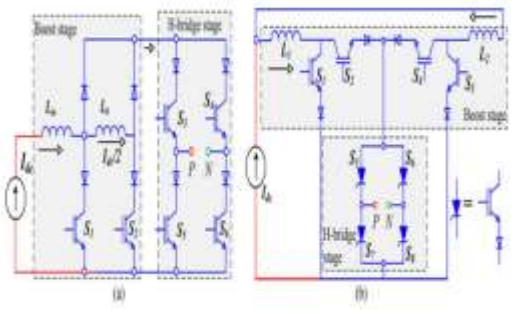

Fig. 5. Two-stage current-fed MLC. (a) Boost stage using multi-rated cell. (b) Boost stage using single rated cell

up of a three-level dc–dc boost converter stage with four semiconductor devices and an H-bridge inverter stage. The boost stage is operated at designed switching frequency whereas the H-bridge is operated at fundamental frequency. The intermediate current levels are achieved by the inductors and they help in balancing the different current levels. The topology has been introduced by Yu using the generic multilevel inductor cells. As explained in Section II-B that multi-rated MLC also have been derived using multilevel inductor cells. In case of multi-rated MLC topology, to make a generic L-level it requires 2* (L − 1) semiconductor devices and (n − 3) current sharing inductors, whereas with the two-stage MLC topology only (L + 3) semiconductor devices and L−3 2 current sharing inductors are needed. A detailed modes of operation of two-stage MLC can be referred from. To further reduce the number of switches in the converter by half in number, the top switches in the boosting stage of the topology can be replaced by power diodes. The mathematical derivation for the design of the intermediate inductors for 7L two-stage converter can be referred from. It shows that the value of main inductor (connected to dc side) depends on the inverter fundamental frequency, whereas the intermediate inductors value depends on switching frequency. In, the boost stage of twostage MLC has been achieved by single-rated 3L current cell instead of multi-rated inductor cell and the diodes are replaced by semiconductor switches as shown in Fig. 5(b).

2) H-Bridge With Inductor Cell MLC:

Another emerging topology, which has been recently proposed based on common emitter arrangement with inductor cells is shown in Fig. 6. Common emitter arrangement of switches reduces the number of driver circuits. By incorporating this advantage, Naguchi and Suroso have developed the H-bridge with inductor cell topology by introducing inductors as dc current sources in the common emitter configuration. The CSI H-bridge acts as the main inverter of the topology followed by parallel connection of single or more inductor cells which act as auxiliary circuits. Each cell is composed of an inductor with four unidirectional semiconductor devices. If number of level is represented as L-level and number of auxiliary inductor cells is represented as Ncell then the relationship is given by L = (2N +1 + 1) and the current flowing in the inductor

cell i is given by Id c 2i , where i = 1, 2,...,L. Due to this modularity nature, the topology has been classified as hybrid MMC. The major operation a difference between this topology and rest of the topologies discussed so far, is that the inductors in the cell have three states such as charging (positive current slope), discharging (negative current slope), and constant current circulation (inductors shorted) whereas the other topologies have only charging or discharging states. The modes of operation can be referred from . The additional advantage of this topology are smaller di/dt, reduced output filter size, small value of inductors compared to multi-rating inductor and single-rating inductor MLCs and avoidance of isolated gate driver due to common emitter configuration. 3) Buck–Boost and Cuk Derived CS-MLC: ´ Buck–boost derived 5L CSI is shown in Fig. 7(a). Unlike other current-source MLCs which are aiming at voltage boost, this converter employs buck–boost technique to realize low voltage output. The buck–boost derived converter utilizes voltage source and two inductors with two CSIs to achieve multilevel in the output current waveform. Additional semiconductor devices SW and SW are employed to effectively isolate the input dc rails from unnecessary circulating currents between CSIs. The topologies discussed so far face difficulties in maintaining a constant output voltage if the input side voltage rises or lowers. However, with the buck–boost topology this difficulty can be overcome as it can operate with wide voltage-conversion range with minimal number of components. In addition to this, the topology has natural balancing of dc-link inductor currents within each switching cycle without additional hardwares . With the alternative phase opposition disposition (APOD) modulation, the shoot through path is achieved during which one of the inductor free wheels and the other one can charged through source. This helps in reducing the component count by removing the semiconductor device SW and the modified topology. The input current in the buck–boost 5L CSI is of discontinuous nature and, hence, in order to maintain smooth input current a current-source version has been suggested as shown in Fig. 8(a). This topology is named as Cuk-derived 5L ´ CSI and it differs from buck–boost derived topology by replacing the voltage source by the current source and an ac capacitor. The operating principle and switching patterns of both buck–boost derived and cuk-derived 5L CSIs are similar except ´ that inductive charging energy is derived through capacitor C in case of Cuk-derived topology. Detailed switching operation ´ and mathematical analysis can be referred from

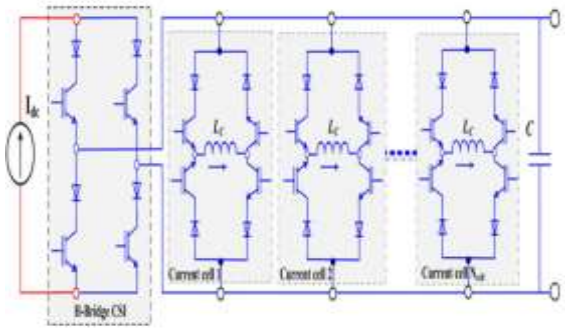

Fig. 6. H-bridge with inductor cells

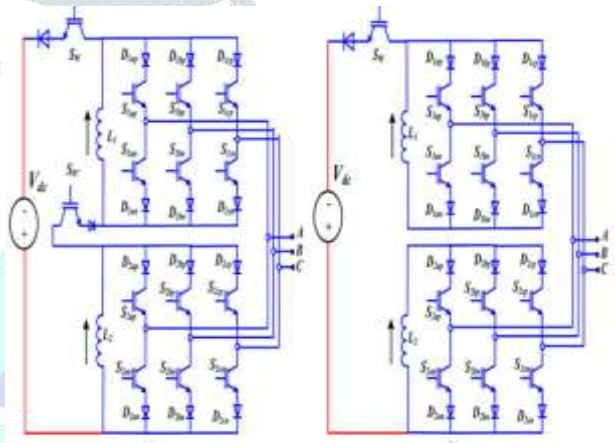

Fig. 7. Buck-boost derived 5L CSI (a) with two switch arrangement. (b) with reduced component count.

4) Modular Multilevel Converter:

MMC has been in the recent research trend and it has received high attention from academia as well as from industry. Current source MMC has been proposed recently by Liang et al. In general, the circuit configuration of MMC has three arm-legs for three phase and each leg has two arms one for positive rail and another for negative rail. The arm comprises of several modular cells to produce multilevel output waveform. In case of voltage fed MMC, the modular cells are made of capacitor and semiconductor device combinations, and they are connected in series to produce multilevel voltage. In other words, connecting modular cells made of inductors and semiconductor devices in parallel on each arms produces multilevel current waveform. The MMC topology with the inductor modular cells is shown in Fig. 8(b) [25]. The basic inductor-based modular cells such as half-bridge

cell and full-bridge cell are shown in Fig. 8(b) and these cells are inserted or bypassed in each arm of the converter to control the output current. A detailed analysis and operation of the current source MMC can be referred from [24]. The dangerous fault that could happen for current source MLC is open-circuit fault which is common for all current source topologies, especially in the modular topology its possibility of occurrence is high due to more inductors. This could be avoided by modifying the inductor cells with antiparallel connection of press-pack diodes or thyristors to provide emergency current path during short interval of time . Another common issue that could be faced by current-fed MLC listed in Sections II-A to II-C on high-voltage application is that semiconductor devices have to face full ac voltage. In this issue has been overcome by the voltage scaling methodology for current source MMC by modifying the modular cells to have both inductor and capacitor. Circulating current is a commonly found issue in MMC, in case of current source MMC this is caused by the ripple current in the sub-module inductor. Bhesaniya and Shukla have proposed inductance selection method on currentfed MMC which ensures the minimization of inductor ripple current and thereby it reduces the circulating

current. E. Comparison of Topologies The overall comparison with advantages and challenges of the presented topologies is shown in Table I. Since some of the emerging topologies are only applicable for single-phase

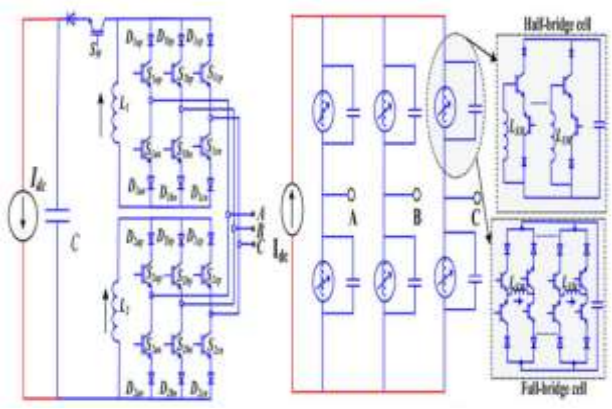

Fig. 8. Emerging topologies. (a) Cuk derived 5L CSI. (b) Current-fed MMC.

operation, the comparison table is made based on single phase version of the presented topologies. The details related to the inductors are formulated by only considering sharing inductors or cell inductors. The input side inductors are not included since they are found in all the current-fed converters. It could be observed that the classical topologies such as single-rating inductor, multi-rating inductor, and parallel Hbridge are utilizing same number of semiconductor devices for obtaining L levels in the output current waveform. This is because all three are H-bridge modules based inversion. For single-rating inductor and multi-rating inductor topologies, current balancing is the main challenge for the inverter operation. The sharing inductors in the modules are in the order of 100 s of mH to reduce low-frequency ripple in the module currents. However, for single-rating inductor MLC, the ripple current amplitude is half that of multi-rating inductor MLC for same values of sharing inductors. This is because the low-frequency ripple current flows through four sharing inductors in 5L single-rating inductor MLC whereas in case of 5L multi-rating inductor only two inductors appear in the current path. The low-frequency ripple issue can be eliminated in single-rating inductor topology by utilizing interphase trans-formers and with that inductances size depend only on switching frequency. In case of parallel H-bridge, the dc input current ripple is controlled by the dc–dc converter or current-source rectifier at the front end. In case of rectifier-based input dc source, the inductor size will be of the order of 100 s of mH whereas in case of dc–dc converter the input inductor size is decided by the switching frequency. Two-stage MLC also utilizes large inductors since the switching operation of the single-phase H-bridge introduces second-order frequency ripple in the input current . For MMC topology, the cell inductors act as storage element and the size of the submodule inductor LSM is decided by the amount of energy need to be stored in the submodule. The value can be calculated as

$$L_{\mathrm{SM}} = \frac{\triangle E}{2N_{SM} i_L^2 \triangle i_L}$$

where

E represents the peak-to-peak energy variation in the arm,

iL represents per-unit current ripple in the submodule inductor, NSM represents number of submodules per arm, iL is the inductor LSM

current, and the value of LSM will be in the order of 100 s of mH. In case of buck–boost derived and H-bridge with inductor cell converters, the inductors values are dependent on the switching frequency of the converter. The size and volume of the converter can be analyzed by considering parameters such as the number of devices, number of sharing inductors, current rating of the inductors, and value of the inductor. With the advanced development in the semiconductor devices, the insulated-gate bipolar transistor (IGBT)/metaloxide-semiconductor field-effect transistor (MOSFET) devices are available in different configurations such as three-phase bridge, single-phase bridge, half bridge, etc. The size of these package modules are more compact and, hence, in the overall converter size, the devices size is minimal when compared to the inductor size. For current-fed converters, the size of the inductors decide the overall size of the converter. From the Table I, it could be observed that the MMC topology is having more number of inductors as well as the values of inductors are in the order of 100 s of mH and, hence, the MMC is larger in size among all the topologies. Single-rating inductor is the next topology with higher number of inductors and the inductors sizes are also in the order of 100 s of mH, however, 28.2% volume can be reduced if interphase transformers replace the inductors. MultiRating inductor MLC and buck–boost derived MLC have same number of inductors but buck–boost derived value depends on switching frequency and, hence, the converter volume can be reduced. Even though parallel H-bridge has no sharing inductors but it needs multiple dc sources which makes it the largest among other converters. Two-stage and H-bridge with inductorcell MLC topologies achieve required current level using single sharing inductor, however, the two-stage inductor value is larger compared to the H-bridge. The current-fed multilevel topologies utilize fully controllable switches in order to achieve the better quality waveforms. The reverse voltage blockage capability and unidirectional current flow are the minimum criteria for semiconductor devices selection. A series diode with IGBT or MOSFET device can achieve

the reverse voltage blocking at the expense of losses and cost. The semiconductor devices such as reverse block (RB) IGBTs and integrated gate-commutated thyristors allow reverse voltage blocking operation and, hence, the series diodes can be avoided.

MODULATION TECHNIQUES

The aim of the modulation techniques for current-fed MLCs is to produce stepped waveform for given operational condition (frequency, amplitude, and phase fundamental component) and also to minimize the input current ripple. Other criteria of modulation technique include achieving current balance between multiple inductors, minimizing the harmonic distortion of output current, maintaining equal distribution of power losses among modules or semiconductor devices, and so on. The modulation techniques that are widely used in voltage-fed MLC have been modified and proposed for current source MLCs. Compared to voltage-fed MLCs, modulation of current-fed MLC needs to satisfy additional set of constraints, hence an extra conversion method need to be included in order to implement the constraints. The various conversion methods are surveyed and are explained in this section. This section also explains how these methods are extended to multilevel operation from CSI operation. In addition, a generic conversion method for realizing the operational constraints on current-fed MLC is proposed in this paper. Finally, various modulation schemes that utilize these conversion method is discussed in detail.

Proposed Modified SOP

SOP technique is a combination of synchronous PWM and optimization. A generalized methodology has been developed for voltage-fed MLCs with any number of voltage levels. Synchronous refers to the ratio of switching frequency fs to operating frequency f1 is an integer and by doing so the subharmonics can be eliminated. The step by step procedure of classical SOP technique can be referred. In short, SOP technique determines number of switching angles for each steady-state operating point and, then, optimization is performed to obtain switching angles that minimize the harmonic distortion of output current. At the last step of SOP, the optimal switching angles are assigned to each semiconductor device to realize optimal current waveforms based on a systematic procedure. The classical SOP technique cannot be directly applied for CSI and it needs some

modification to include the operational constraints mentioned. One possible option is, to modify the last step of SOP technique to convert optimal switching angles into constraint optimal switching angles using conversion method explained. Parallel H-bridge 5L CS MLC is considered for proposing SOP modulation technique. As per conversion method discussed III-A5, it requires 3L reference waveform for producing 5L constraint current waveform. Consider 3L reference current waveform i3L. 14 with switching angles at α1 to α6 in a quarter period. In general half-wave and quarter-wave symmetries is introduced in the switching pattern to eliminate all even-order harmonics. Using the proposed conversion method,

CONCLUSION

The multilevel operation of CSCs provides advantages such as high current operation, reliability, ripple-free current, and high performance. This paper has provided review of various classical as well as emerging topologies of current-fed MLC topologies by highlighting merits and demerits of each topology. Modulation of current-fed MLC requires additional conversion stage compared to voltage-fed MLCs. This paper has covered most of the classical conversion technique for realizing operational constraints on CSI and how these methodologies are extended to current-fed MLCs. A generic conversion method has been proposed which can be utilized for any reference-based modulation techniques. In addition, the paper has also surveyed about existing modulation techniques for current-fed MLCs and proposed an emerging modulation technique named SOP for low-device switching frequency operation. Finally, several prospective applications for current-fed MLC topologies have been presented. Being an emerging topic for research, there exists huge scope of research to further develop new topologies and modulation techniques for these topologies.

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