DESIGN AND IMPLEMENTATION OF 4-BIT SHIFT REGISTER USING DOMINO AND DOIND LOGIC TECHNIQUES

Dr. S. Aruna[1],B.Kiran Teja [2], K. Srinivasa Naik[3]
Assistant Professor[1], M.Tech Scholar [2], Associate Professor[3]
[1,2,3]Department of Electronics and Communication Engineering
[1,2]Andhra University College of Engineering, India
[3]VIIT, India

Abstract: Dynamic CMOS logic circuits are utilised in the VLSI ICs to get the high performance of systems. But the parameter variations are serious problems in the deep sub-micron Technology by scaling down dimensions of transistors. Power consumption ,delay and leakage current are the performance parameters of any logic circuit. The performance of circuit reduces by the increment of power, delay and leakage current. To overcome these transistor parameter variations in nanometer technology design should be conscious of fluctuations.

In this DOIND logic design and domino logic design are used to study the variances issue. DOIND logic is designed from domino logic. DOIND logic design minimises leakage current as well as it minimises the variances issue with less delay disadvantage. Several processes, Voltages and Temperatures (PVT) variances studied at 60nm technology node for a domino logic and DOIND logic for Serial in Serial out (SISO) 4-BIT Shift Register, Parallel in Serial out (PISO) 4-BIT Shift Register and Parallel in Parallel out (PIPO) 4-BIT Shift Register, using Tanner EDA tool.

Keywords DOIND logic, Leakage current, PVT, nanometer Technology, domino, Scaling

I. INTRODUCTION

Dynamic CMOS logic circuits are generally utilized in current computerized VLSI circuits on account of preeminent speed and size features of dynamic CMOS logic circuits as contrast with static CMOS logic circuits. Anyway dynamic CMOS logic circuits have less resistant to noise and expanded power dispersal than static CMOS logic circuits.

objective in the present VLSI circuit structures. So unique cooling hardware is important to eliminate more temperature delivered during the time of circuit operation. Power utilization in CMOS circuits can be dynamic or static. Dynamic power dissemination happens because of exchanging activities of short circuits current and charging and releasing load capacitances. Static power utilization is another sort of intensity dissemination in CMOS circuits. Discharge current flows with sub threshold source-to-drain discharge, reverse biased junction band-to-band burrowing, gate oxide burrowing, and other current drawn constantly from the power supply cause static power dissolution [7].

Today, the need of versatile frameworks and at the same time enhancement in battery execution delineates the power utilization is main consideration in CMOS VLSI circuits parameters [3]. To lessen dynamic power dissemination it is important to decrease the supply voltage of the circuit, decrease of supply voltage after a precise point influences the execution of the circuit, to keep up circuit execution of the circuit it is important to diminish the threshold voltage too, however it prompts leakage power dissolution. Leakage power can be lessened by expanding the threshold voltage [5].

II.RELATED WORK

There are some methods to control inconstancy issue at transistor level structure. Body biasing is one of the method to relieve

fluctuation issue.

INDEP approach [3] is the method which has less impact of parameter variety in profound sub-micron region. This method has two additional embedded transistors between draw up and draw down systems which are input logic subordinate. Versatile body biasing is the method which reimburse impact of PVT fluctuations. For exactness and run time exchange off two calculations, process temperature versatile body inclination and process versatile body predisposition temperature versatile body inclination were proposed [4].

Sleep method [5] is the procedure for leakage control decrease. In the sleep method two sleep transistors (a PMOS and a NMOS) are included the circuit. The sleep transistor is switch on when circuit is dynamic mode and switch off when circuit is inactive mode[6] [7]. Ideal sleep vector is resolved for double Vth domino circuit under PVT changes [8].LECTOR-B system [9][10] is investigated under PVT varieties and has less impact parameter fluctuations

III. PROPOSED LOGIC DESIGN

In this paper Design of 4-Bit shift register using Domino logic and DOING logic are explained below. The operation of 4-Bit shift register in both the logic designs are discussed.

A. Design of 4-Bit shift register using Domino logic

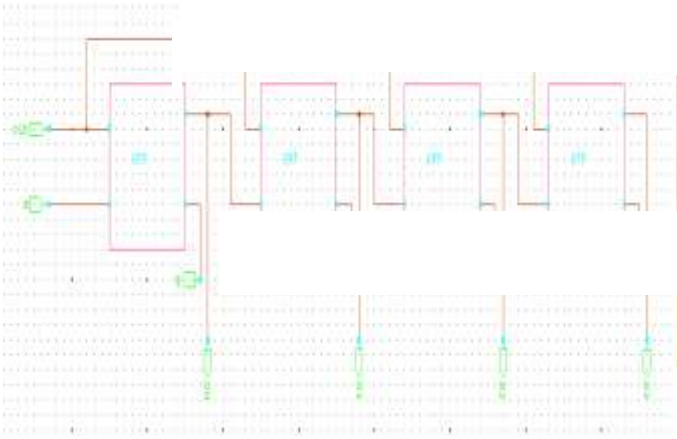


Fig 1.Domino logic 4-Bit Shift Register using Domino D-FF

Domino logic 4-Bit shift register using Domino D-FF is of serial input serial output type of shift register shown in fig 1.In this when clk signal is low, then d input should be 1 so that output s is 1.when the clk signal is high, then d input should be 0 so that output is 0.when both clk signal and input is same the output is undefined. n Bit-shift register designed using ‘n’ number of D-FFs. Each D-Latch designed using two 2-input nand gates followed by an inverter.

B. Design of 4-Bit shift register using DOIND logic

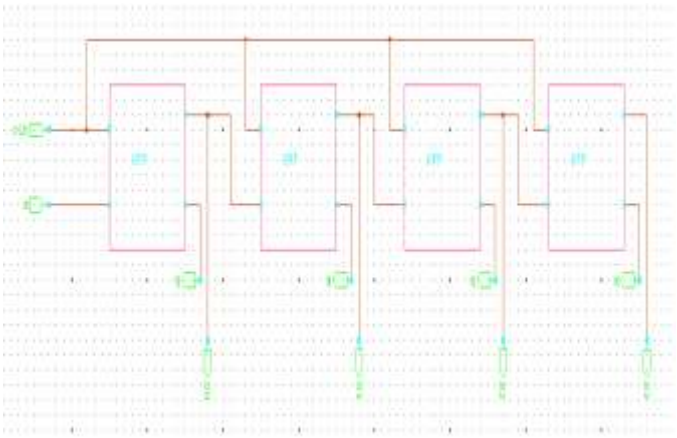


Fig 2.DOIND logic 4-Bit Shift Register using DOIND D-FF

DOIND logic 4-Bit shift register using DOIND D-FF is of serial input serial output type of shift register shown in fig 2. The Design and operation of DOING logic Design is in the same way as Domino logic design.

IV. SIMULATION RESULTS

The TSPICE simulator is taken for the determination of power consumption, delay and leakage current of various types of 4-Bit shift registers. Here discussed about the Domino logic and DOIND logic serial in serial out (SISO) 4-Bit shift register, parallel in serial out (PISO) 4-Bit shift register and parallel in parallel out (PIPO) 4-Bit shift register.

C. Different types of Domino logic 4-Bit shift registers

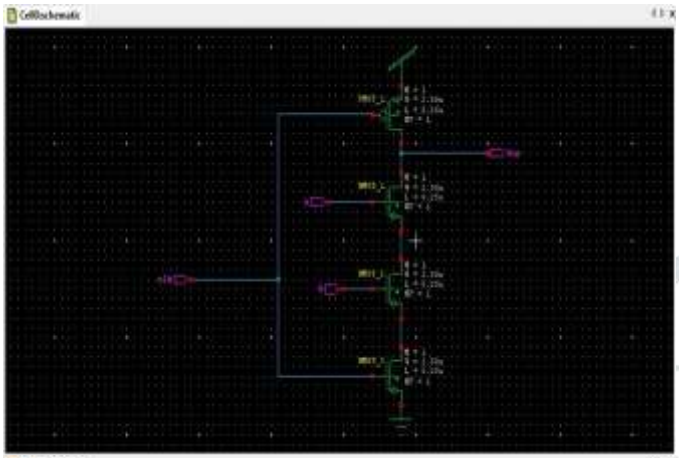


Fig 3.Schematic diagram of Domino logic NAND gate

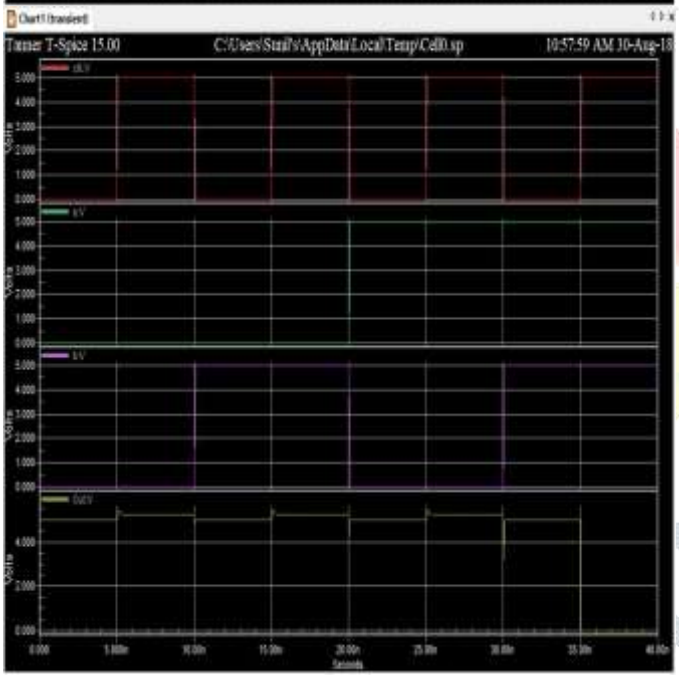


Fig 4. Output waveform of Domino logic NAND gate

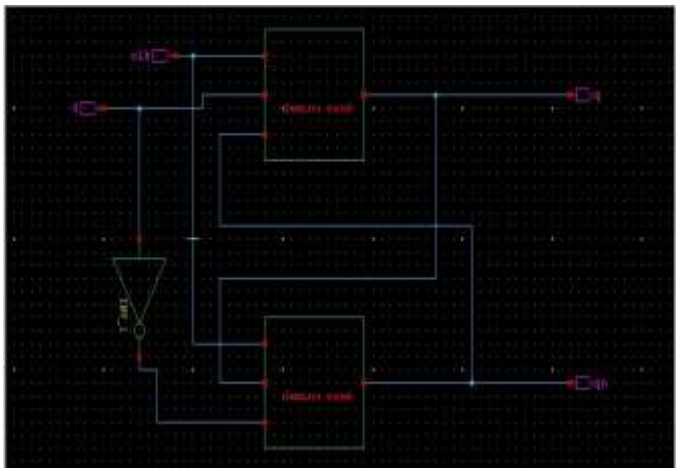


Fig 5. Schematic diagram of Domino logic D-Latch

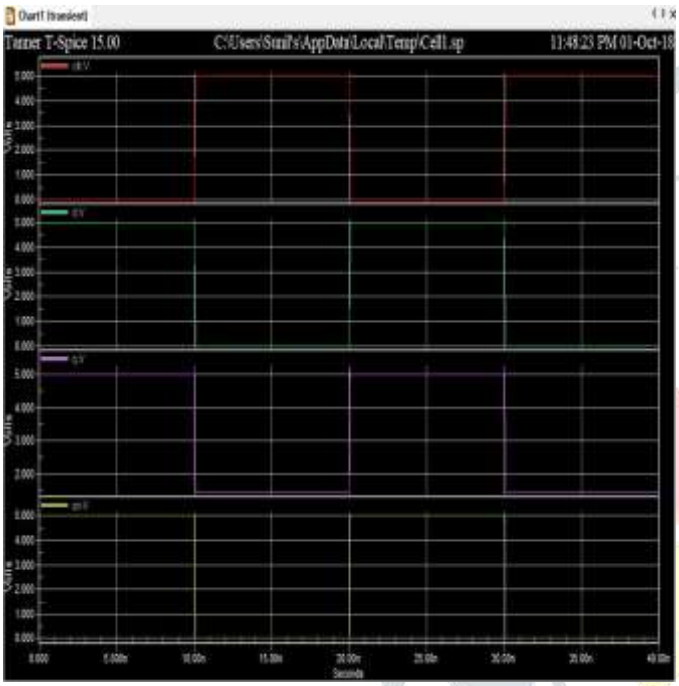


Fig6. Output waveform of Domino logic D-Latch

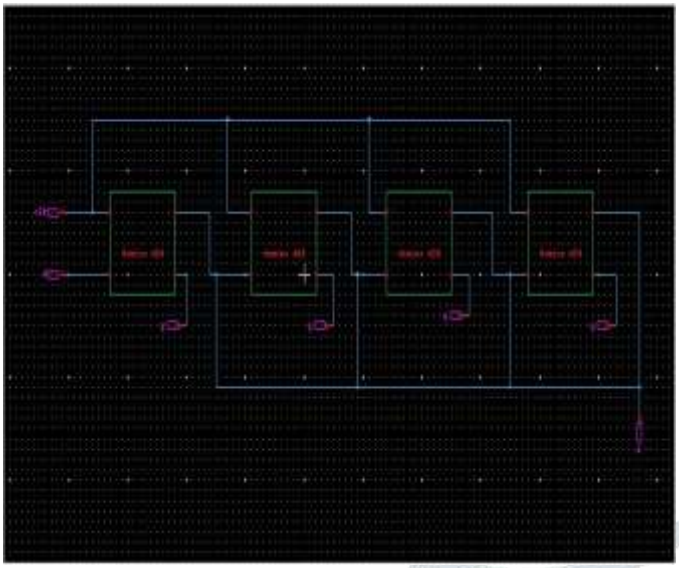


Fig 7. Schematic diagram of Domino logic 4-Bit shift register (SISO)

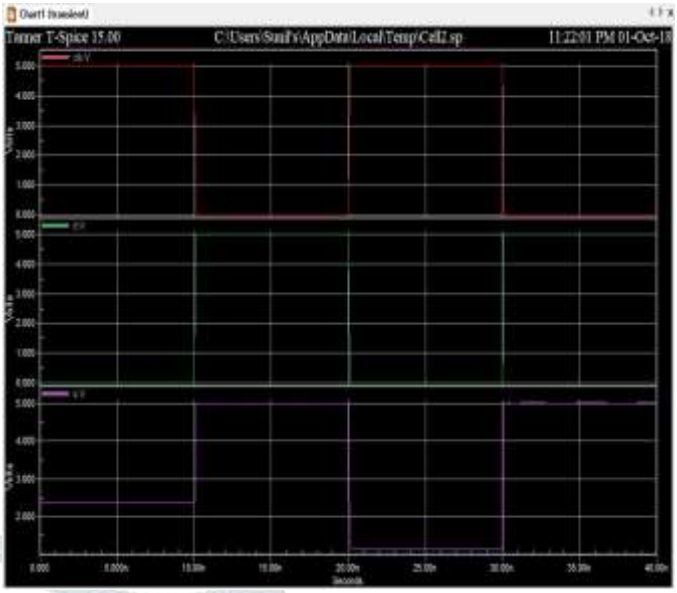


Fig 8. Output waveform of Domino logic 4-Bit shift register (SISO)

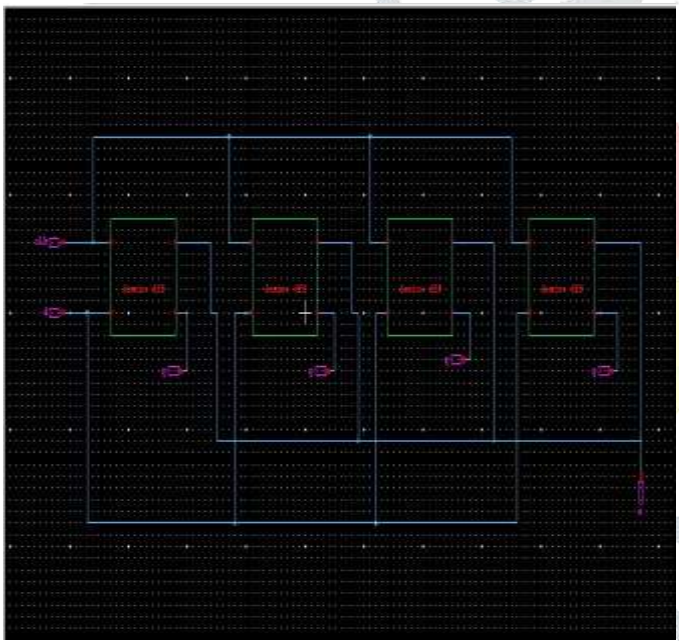


Fig 9. Schematic diagram of Domino logic 4-Bit shift register (PISO)

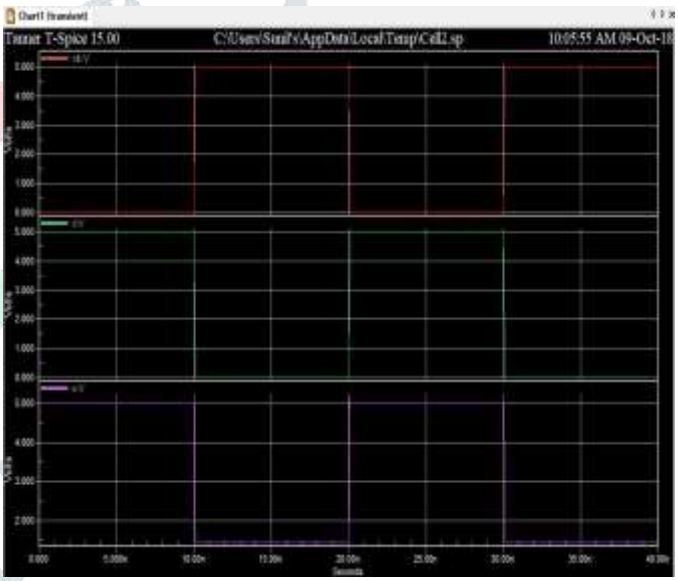


Fig 10. Output waveform of Domino logic 4-Bit shift register (PISO)

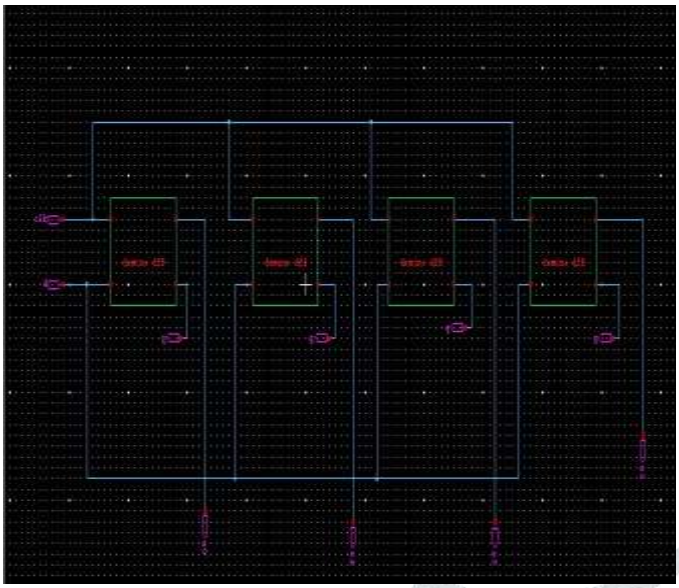


Fig 11. Schematic diagram of Domino logic 4-Bit shift register (PIPO)

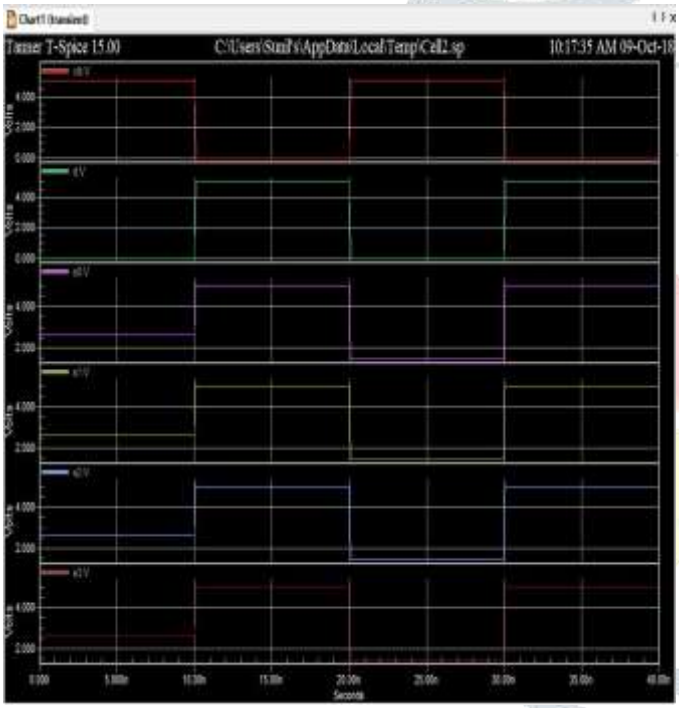


Fig 12. Output waveform of Domino logic 4-Bit shift register (PIPO)

D.Different types of DOIND logic 4-Bit shift registers

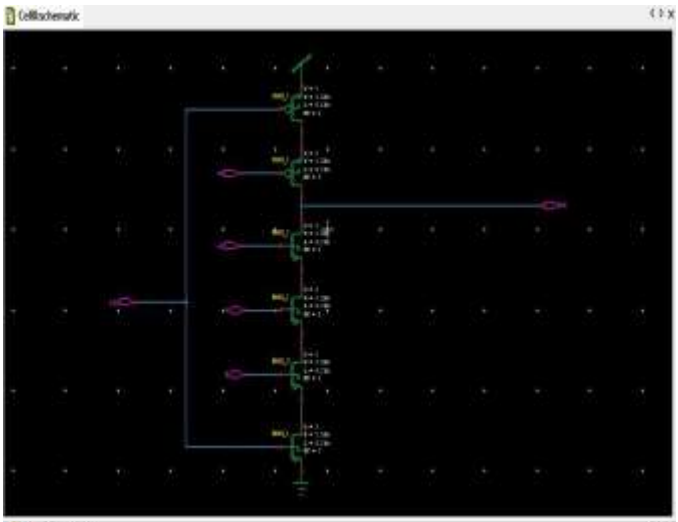


Fig 13. Schematic diagram of DOIND logic NAND gate

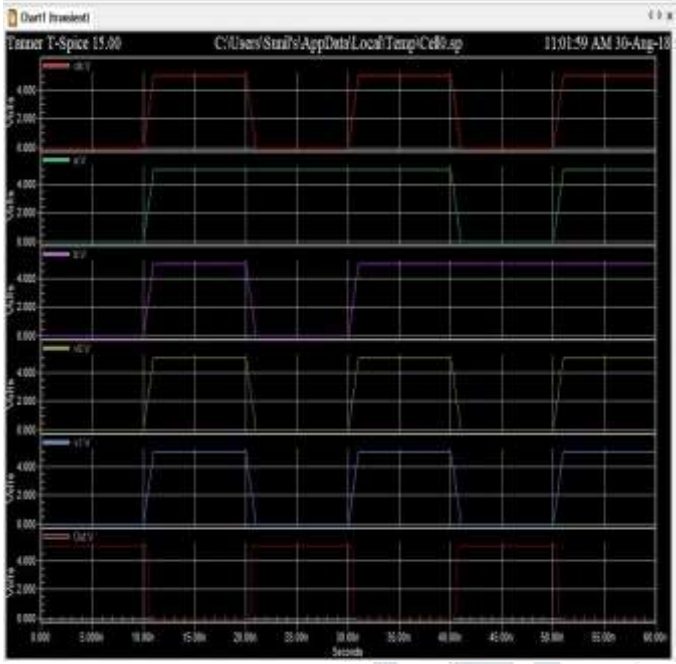
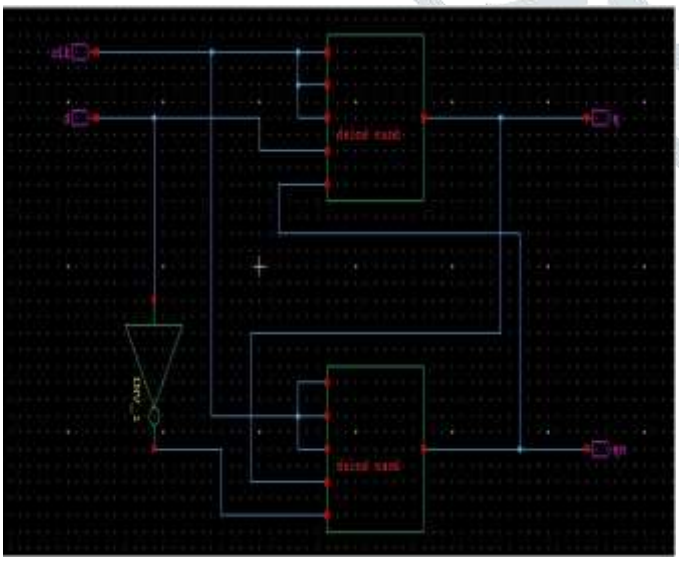


Fig 14. Output waveform of DOIND logic NAND gate



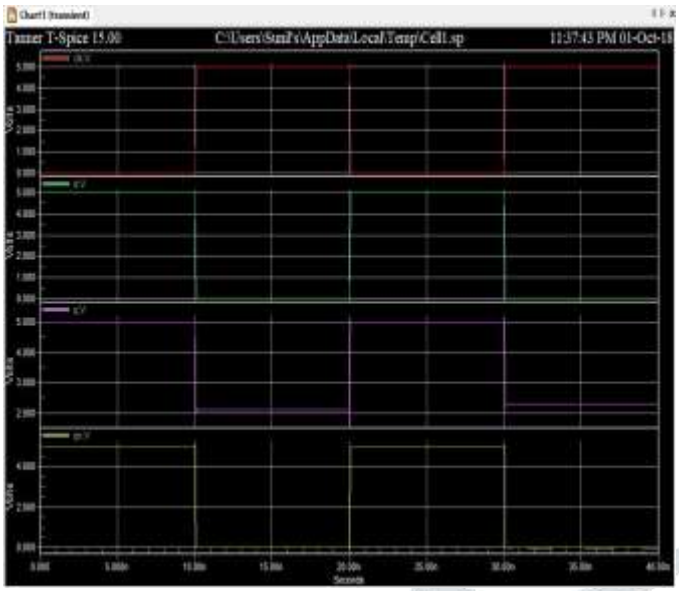


Fig 15. Schematic diagram of DOIND logic D-LATCH

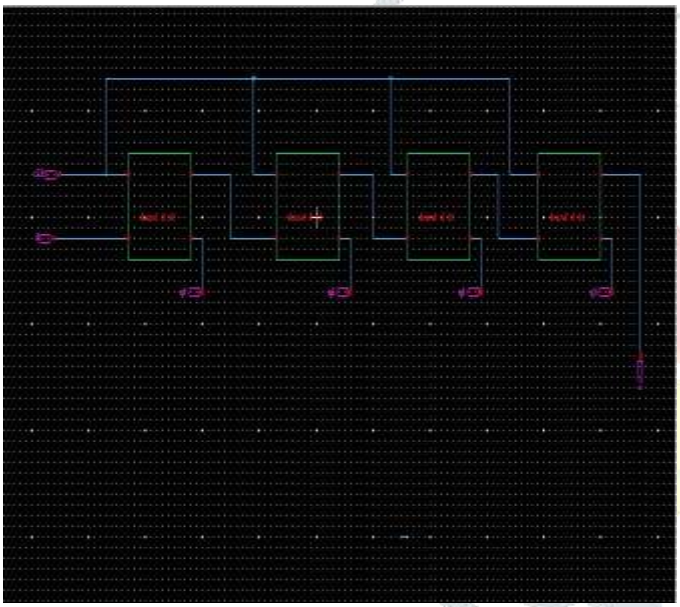


Fig 16. Output waveform of DOIND logic D-LATCH

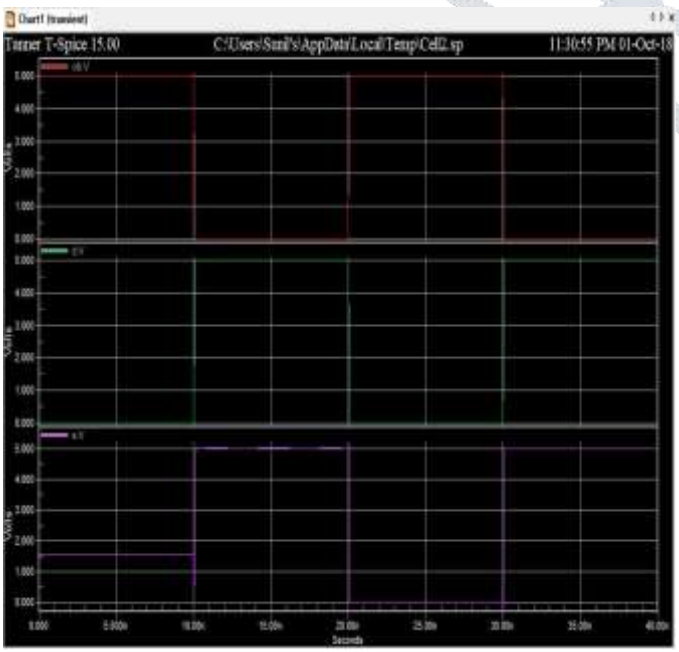


Fig 17. Schematic diagram of DOIND logic

Fig 18. Output waveform of DOIND logic

4-Bit shift register (SISO)

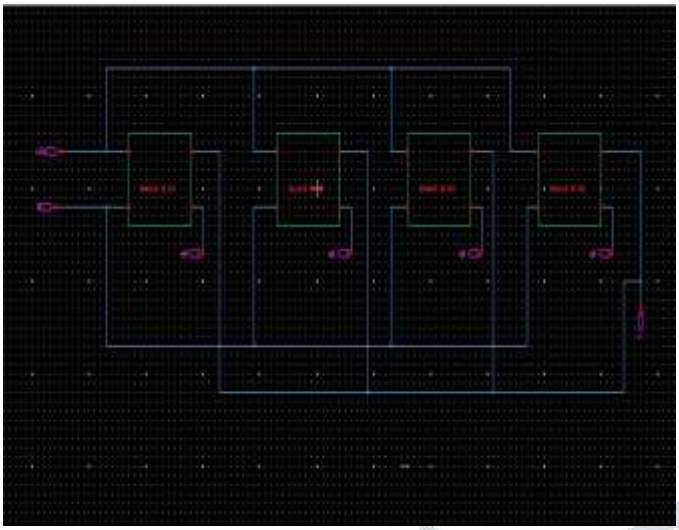


Fig 19. Schematic diagram of DOIND logic

4-Bit shift register (SISO)

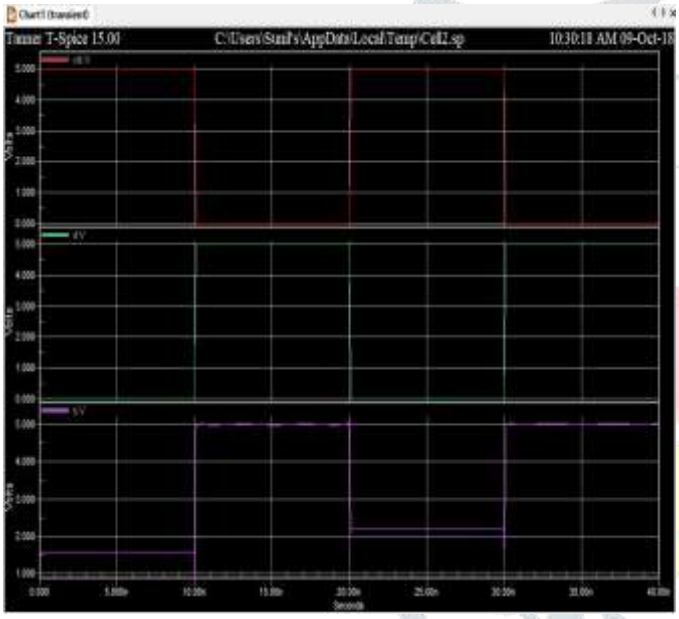
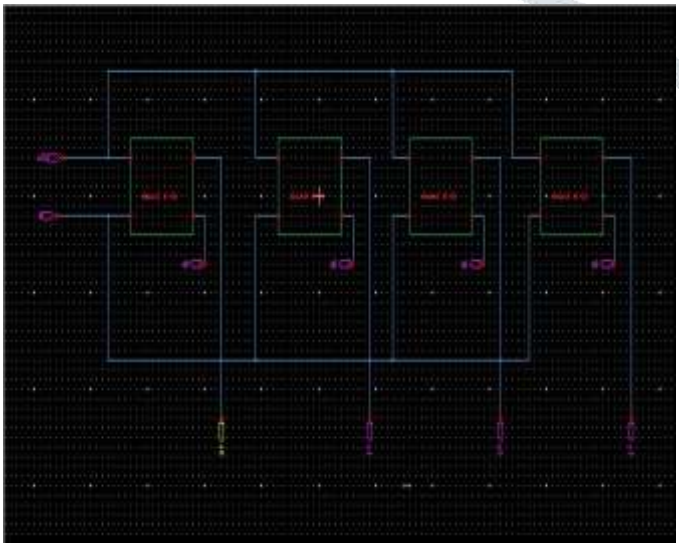


Fig 20. Output waveform of DOIND logic

4-Bit shift register (PISO)



4-Bit shift register (PISO)

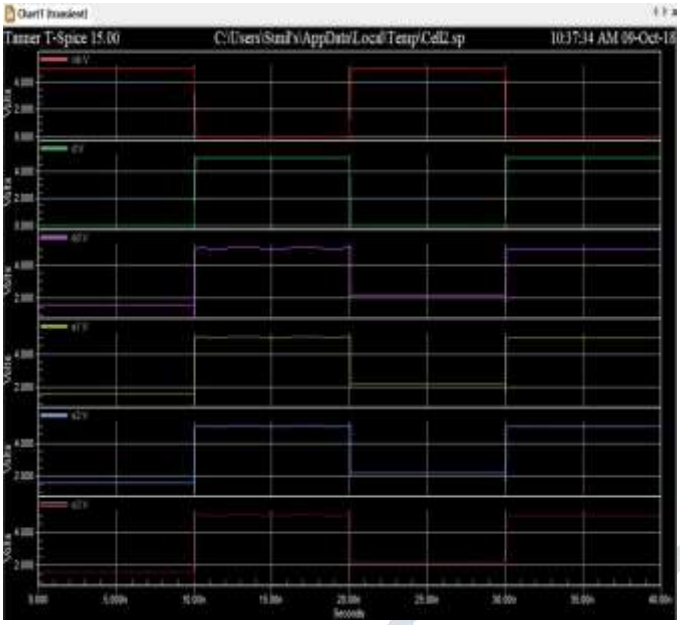


Fig 21. Schematic diagram of DOIND logic 4-Bit shift register (PIPO)

Fig 22. Output waveform of DOIND logic 4-Bit shift register (PIPO)

E.Comparision of power, delay and leakage current for Domino and DOIND logic 4-Bit shift registers

Parameter	**Domino logic**	**DOIND logic**
POWER	19.8876nW	11.5285Nw
DELAY	10.0285nS	10.0113Ns
LEAKAGE CURRENT	1.40mA	1.285Ma

Table 1. Comparision of power, delay and leakage current of Domino and DOIND 4-Bit shift registers

VI .CONCLUSION

In this paper different types of 4-Bit shift registers are designed in Domino and DOIND logic designs. from the measurements of power, delay and leakage current DOIND logic gives good results compared to Domino logic. Variation in temperature from zero degrees to 120 degrees performance of DOIND logic far better than the Domino logic 4-Bit shift register.

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