IMPLEMENTATION OF HUE, MAX, MIN, DIFFERENCE CONVERTER FOR COLOURED IMAGE BASED ON REVERSIBLE LOGIC

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Abstract : Emerging technologies in VLSI, enables to integrate huge devices on single unit area to build lower power portable devices. In order to build low power systems there is a need for new technology which adapts logic that conserves energy and dissipates no power. Reversible circuits are designed using reversible gates in which number of outputs is equal to the number of inputs and there is a one to one correspondence between the vector of inputs and outputs. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs. In our proposed method each module and sub-modules of HMMD converter based on reversible logic is designed using reversible gates. In this we had tried to optimize the parameters such as area, number of constant inputs, garbage outputs, power and delay associated with the circuit. The experimental results obtained by implementing HMMD converter in CADENCE EDA 90nm technology shows the considerable reduction in power, area and delay in comparison with the HMMD converter designed using conventional gates

I. INTRODUCTION

The integration of many devices in a single unit area is possible due to emerging technologies. However, dissipation of heat due to power loss is still a major problem. Physical limit also exists in the decrease of heat. In order to build low power systems there is a need for new technology which adapts logic that conserves energy and dissipates less power. These circuits are similar to conventional logic circuits except that they are built from reversible gates.

Colour is one of the essential visual attributes for human vision and image processing. Colour histograms are widely used in content-based image retrieval techniques and they are invariant to rotation, scaling and other spatial transformations on the images. The HMMD have better results in applications for image retrieval. The transformation from RGB to HMMD is a non-linear reversible transformation. The recent researches in the field of HMMD converter proves the significant purpose of converter in the field of nanotechnology, image processing and in design of low power electronic devices.

The idea of reversible circuits comes from Landauer's principle. According to this, at least kT ln (2) joule of energy is dissipated for each bit of information that is lost where, k is the Boltzmann's constant and k=1.38x10 -23 J/K, T is the absolute temperature in Kelvin Ideally a reversible circuit has no information loss so that there will be no power loss.

The important terms in reversible logic circuits are the quantum cost, the delay, and the number of garbage outputs. Garbage outputs are the unutilized outputs in reversible circuits which exist just to maintain reversibility but do not perform any useful operations.

The reversible logic should have these features like they do not allow fan-outs. The logic circuits should have minimum QC. The design can be optimized so as to produce minimum number of garbage outputs. The reversible logic circuits must use minimum number of constant inputs. The reversible logic circuits must use a minimum logic depth or gate levels.

In paper [1], the authors proposed the design of RGB to HMMD converter using reversible adders, registers, dividers and multipliers. The block for HMMD converter that is useful in the field of reversible real time video treatment. In papers [2],[3] the authors proposed the design and evaluation of optimised reversible multiplier and divider that is used in low power dissipation and high speed applications.

II. LITERATURE SURVEY

The block consists of many sub blocks which are constructed individually using reversible gates and are then integrated into single block. In this paper the quantum cost, garbage outputs and constant inputs are reduced. The demerit is that this converter cannot be modified for conversion of other colour spaces[1]. The reversible divider is constructed using multipliers, adder/subtractors and registers. Along with these, new gates such as BHA, BHB, BHC and BHD are introduced. Even it is a large block of implementation; it is focused on reducing quantum costs, hardware complexity and garbage outputs. Despite of this, the area should be lowered in this circuit since more area is consumed by the divider circuit since it has more logic blocks[2]. The proposed design in this paper for divider is having a better quantum cost than compared to other designs. But, the worst case is that it gives out large number of garbage outputs[3]. Two methods of fault tolerant systems are introduced. The fault level is very much reduced but the area still matters. There is a huge area consumed by this circuit and there is more hardware complexity. Even though this method reduces the garbage outputs and provides better quantum cost[4] for the divider circuit.

III. REVERSIBLE LOGIC GATES

Reversible logic is an important approach to reducing energy consumption and improving the design of low power VLSI and ULSI circuits. Power consumption is a significant issue in modern microprocessor design and a major challenge in digital system design. Reversible logic is a promising design which presents a method for constructing circuits that produce no heat dissipation. Reversible computing emerged as a result of the application of quantum mechanics, image processing and nanotechnology.

According to Landauer's principle, the loss of one bit of information will dissipate *kT ln2* joules of energy. The basic combinational circuits dissipate heat energy for every bit of information lost during the operation. This is because according to second law of thermodynamics, information once lost cannot be recovered by any methods. In 1973, Bennett, showed that in order to avoid *kT ln2* joules of energy dissipation in a circuit it must be built from reversible circuits.

According to Moore's law the numbers of transistors will double every 18 months. Although this time-line varies up to 24 months, regardless of exact number. From this it is agreed that the rate of growth is rapid. New processing technologies are being developed. The conventional devices are eliminated and a need for low power chips arose to keep the power density of IC's within tolerable limits.

While the power dissipation increases linearly with advanced version processors, the power density increases exponentially, because of ever-shrinking size of IC's. If this exponential rise in power density continues, the µp designed a few years later would have the same power of the nuclear reactor.

Another important factor that fuels the need for low power chips is the increased market demand for portable consumer electronics powered by batteries. Battery life is becoming the product differentiator in many portable systems. Digital systems such as cellular phones, notebook computers and digital assistants are running on batteries. For these systems, low power consumption is a major concern, since it directly affects the performance of the battery permanence.

Table 1: Gates and its equations:

Gates	Inputs	Output Equation
Feynman	A,B	$P=A$; $Q=A$^B
Double Feynman	A,B,C	$P=A$;$Q=A$^B;$R=A$^C;
NOT gate	A	$P=(\sim A)$;
Tofolli gate	A,B,C	$P=A$; $Q=B$;$R=((A\&B)$^$C)$;
TR gate	A,B,C	$P=A$;$Q=A$^B;$R=(A\&(\sim B))$^C;
Peres gate	A,B,C	$P=A$;$Q=A$^B;$R=(A\&B)$^C;
Fredkin gate	A,B,C	$P=A$; $Q=(((\sim A)\&B)$^$(A\&C))$; $R=(((\sim A)\&C)$^$(A\&B))$;
Islam gate	A,B,C,D	$P=A$;$Q=A$^B; $R=(A\&B)$^C; $S=(A\&B)$^$((\sim B)\&(A$^$C))$
BJN gate	A,B,C	$P=A$;$Q=B$;$R=(A|B)$^C;
BHA gate	A,B,C	$P=A$:$Q=(A\&B)$^$((\sim A)\&(\sim C))$ $R=(((\sim A)\&B)$^$(A\&C))$;
BHB gate	A,B,C	$P=A$^B;$Q=A$^C; $R=(((A$^$B)\&(\sim C))$^$((\sim A)\&B))$;
BHC gate	A,B,C,D	$P=A$; $Q=(((\sim A)\&B)$^$(A\&C))$; $R=((\sim A)\&B)|((\sim A)\&C))$ $S=(((\sim A)\&B)$^$(A\&C)$^$D)$
BHD gate	A,B,C,D	$P=A$;$Q=A$^B^C; $R=((\sim A)\&B)|((\sim A)\&C)$ $S=(((\sim A)\&B)$^$(A\&C)$^$D)$
HNG gate	A,B,C,D	$P=A$;$Q=A$^C; $R=B$;$S=B$^D;

Performance parameters of Reversible Logic

The following are the most common metrics used in literature for evaluating the performance of reversible logic circuits.

Table 2: Gates with QC and Delays:

Gates	Quantum Cost	Delay(Δ)
Feynman gate	1	1Δ
Double Feynman	2	2Δ
NOT gate	1	1Δ
Tofolli gate	5	5Δ
TR gate	4	4Δ
Peres gate	4	4Δ
Fredkin gate	5	5Δ
Islam gate	7	7Δ
BJN gate	5	5Δ
BHA gate	4	5Δ
BHB gate	5	5Δ
BHC gate	6	6Δ
BHD gate	6	6Δ
HNG gate	6	6Δ

Constant input is measured by counting the number of input lines that are kept fixed at either 0 or 1 in order to synthesise the given logical function. Garbage is the number of outputs added to make an n-input k-output function reversible. The relation between the number of garbage outputs and constant inputs is given by, *Input + constant input = output + garbage.*

Quantum cost refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit. Hardware complexity refers to the total number of logical calculation (TC) in a circuit. The hardware complexity (HC) is determined by counting the number of EX-OR operations, number of AND operations and number of OR operations.

III. METHODOLOGY OF RGB TO HMMD CONVERTER

A new colour model HMMD is disclosed based upon hue, the shade, the tone, the tint and the brightness of a colour, and a colour quantizing method using the HMMD colour space is shown in Fig 1.
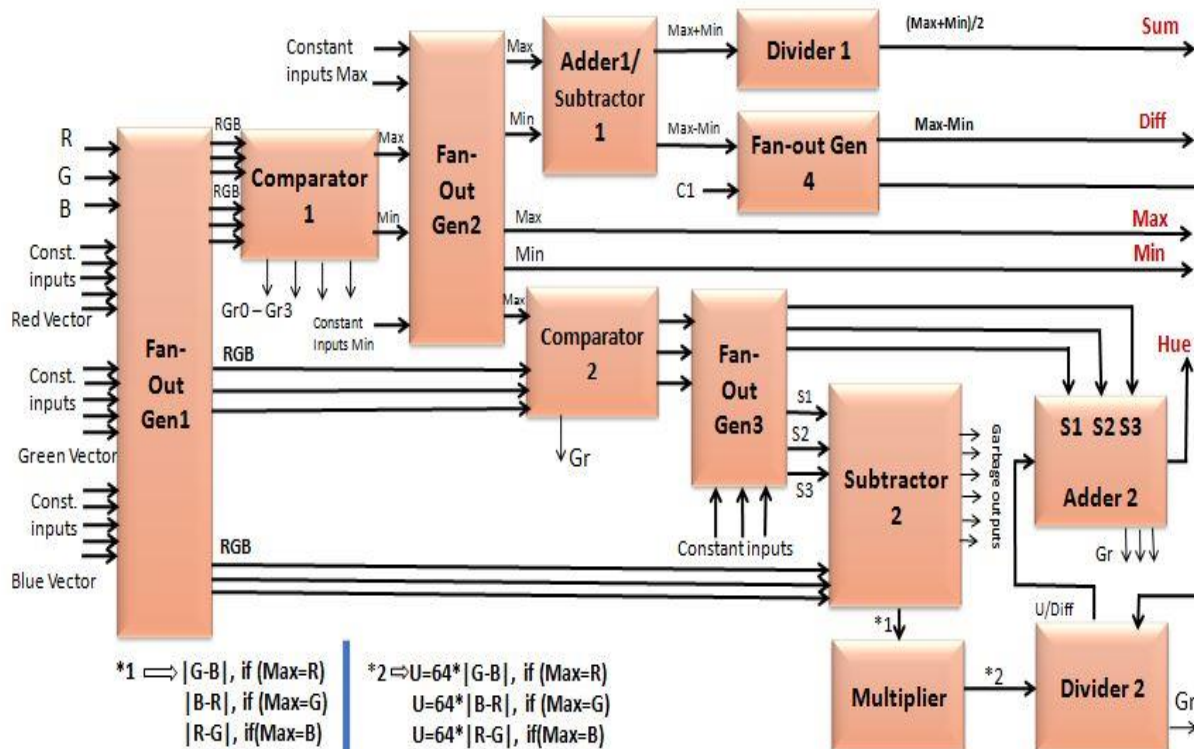

Fig 1: Block diagram of RGB to HMMD converter

The process of RGB to HMMD converter is a non-linear transformation. The HMMD refers to Hue,Max,Min,Diff and Sum.

- Max: max of R,G,B

   This indicates how much black colour an image has giving the flavour of blackness.

   Max= Max{RGB}

- Min: min of R,G,B

   This indicates how much white colour an image has giving the flavour of tint or whiteness.

   Min= Min{RGB}

- Diff: Max-Min

   This indicates how much grey colour an image has giving the flavour of tone or colourfullness.

   Diff= (Max-Min)

- Sum:(Max+Min)/2

   This simulates the brightness of the colour.

   Sum={(Max+Min)/2}

- Hue: When (Max=Min), then Hue=0

IV.BLOCKS OF RGB-HMMD CONVERTER

The blocks used for reversible HMMD converter are fan-out generators, comparators, adder/subtractor, multiplier, and dividers.

Fan-out generators:

The role of fan gen is to create replications of RGB signals. In reversible logic, fan-out is not considered. So, here we have to use reversible gates to create replications of the RGB signals. Fan-gen is composed of two DFG and one FG. The quantum cost of single fangen is 5 (DFG=2 & FG=1).Totally the quantum cost of 8 bit FG is 120. The Min and Diff duplication vectors are composed, respectively, by eight DFG and eight FG gates. The Max vector is composed by eight DFG and eight FG gates.

Comparator:

In present day industrial automation, comparators play a major role. Digital comparator are used in computer processors, and moreover it can be used in some industrial automation devices that contrast visual images with digital images, as in the case of mechanical engineering industry that relies on computer-aided drafting (CAD) programs to check good products from faulty ones. They also can be employed to convert analog signals into digital patterns.

A comparator is a device that compares two signals and outputs a digital signal indicating which is larger. The comparators are used to find the maximum and minimum among the RGB signals. The Max comparator circuit is composed of two multiplexers, two comparators and one fanout generator block. The function for comparing vectors is given by,

R&G: $X_i= R_i .G_i +R_i'. G_i'$

R&B: $X_i= R_i .B_i +R_i'. B_i'$

B&G: $X_i= B_i .G_i +B_i'. G_i'$, for i=0,1,2,3,4,5,6,7

Reversible Multiplier

A multiplier is an electronic circuit which is used to produce the product by multiplying two binary numbers. The multiplier block is made of 32 TR gates that is used to perform multiplication operation.

In the proposed design, one multiplier is used. The functionality is given by,

If (Max=**R**), 60 x |G-B|

If (Max=**G**), 60 x |B-R|

If (Max=**B**), 60 x |R-G|

The quantum cost is 160 and a delay is of 4Δ.

Adder/subtractor

Adder–subtractor is a digital circuit that is capable of adding or subtracting numbers (in particular, binary). Depending on a control signal which is given as input, the circuit performs either as adder or subtractor. Hence it is also possible to construct a circuit that performs both addition and subtraction at the same time. In this design we have used two subtractors One is to calculate (Max RGB- Min RGB) and Second is to calculate (G-B), if Max=R or(B-R), if Max=G or (R-G), if Max=B.

Divider circuit

In this divider circuit we have used non-restoring approach to perform division alogorithm. The divider circuit consists of two multiplexers,one adder and two left shift registers.

The inputs are loaded to the Mux and is given to shift register. After performing the addition subtraction operation the data is loaded to the shift registers. The mux block is made of BHA gate. The shift register is nothing but a D flip flop which is made of one feynman and one fredkin gate.

V. PERFORMANCE ANALYSIS

The below are the performance results obtained from implementing the code in 90 nm technology of CADENCE EDA Tool.

	Area (gate count)		Delay (ps)		Power (nW)	
	Prop.	Conv.	Prop.	Conv.	Prop.	Conv.
Fan-out Generator	72	125	321	350	512.178	5421
Adder subtractor	466	782	366	1020	1917.175	2040
Multiplexer	115	125	150	268	3660.332	4002.5
Comparator	125	325	757	1180	4525.476	9112.5
Multiplier	201	402	465	8570	4526.21	5849
Divider	542	785	935	10252	9869.25	18965.48
HMMD CONVERTER	2095	2392	1225	21596	45268.21	99863.9

The parameters like area, power and delay for all the sub-modules and main module based on reversible logic is compared with the conventional logic and the results are tabulated in the above table. From the comparison results it is clearly verified that the parameters like area, power and delay are very much lowered when using reversible logic.

VI. CONCLUSION

This proposed converter consists of several sub-modules in order to increase the efficiency and lower the power loss. The delay, area and power of the individual blocks are given below. The area of comparator is 125 gate count, delay is 1057 ps and power is 4525.476 nW. The area of adder/subtractor block is 466 gate count, delay is 3266 ps and power is 19177.175 nW. The area of multiplier block is 115 gate count, delay is 150 ps   and power is 3660.332 nW. The fan out generator block has delay of 321 ps and power of 512.1 nW. The integration of the all the sub-modules are done and their performance analysis is done. The RGB-HMMD converter has a area of 2095 gate count, delay of 1225 ps and it consumes power of 45268.21 nW.

VII. REFERENCES

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