

# Comparative Analysis of a Seventeen Level Multilevel Inverter Using Equal Area Criterion and Genetic Algorithms

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**Abstract:** Multilevel inverter topologies (MLIs) are progressively being used in medium and high power applications. This is mainly due to their advantages such as low power dissipation on switches, low Total Harmonic Distortion (THD) and low Electro-Magnetic Interference (EMI) at the output. In this paper, a new Multi-Level Inverter (MLI) topology is proposed. This topology consists of two conversion cells such as Level Generating Cell (LGC) and Polarity Generation Cell (PGC). The basic level generation cell consists of a series combination of power switches, power source and a diode in parallel with both switch and a source. This series combination of such cells generates N-1 levels excluding zero levels. This paper focuses on the reduction of the Total Harmonic Distortion (THD) and calculate the effective switching angles to achieve minimum THD using Equal area criterion and Genetic Algorithms and a comparison is also made between the two methodologies. Simulation model (designed in SIMULINK) is developed and the THD in all cases have been identified. The hardware of proposed seventeen level inverter is implemented and the results are compared and analyzed.

**Index Terms - THD, EMI, LGC, PGC, EAC, Genetic Algorithms.**

## I. INTRODUCTION

In recent years, the electrical power demand is increasing significantly and simultaneously there is depletion of conventional energy sources. Hence we are shifting towards non-conventional energy sources (mainly solar) to fulfil the power requirements. The solar energy is taped using PV cells which convert solar energy into electrical energy in the form of DC. So there is essential requirement for an inverter to converter DC to AC for household applications. For medium and high applications, conventional inverters has low efficiency, high THD and considerably high EMI. So, to overcome these difficulties, we are using Multi-level inverters which has low THD, high efficiency and low EMI. The main concept of multilevel inverter is, utilizing power semiconductor switches for power conversion in small steps. These power conversion in small voltage step helps to obtain less harmonic distortion and switching losses. These inverters process a low voltage rating and has higher efficiency. Also, it reduces the  $dv/dt$  stresses on the power semiconductor devices at the load side. Hence there is a reduction in the size of the output filter and has its efficiency improved. There are multilevel inverter topologies proposed [1], among which the cascaded H bridge inverter topology is widely recognized because of its modularized circuit and lack of clamping diodes or capacitors [2]. Also, this topology can be used for higher level generation of voltage steps with minimal circuit components. Thus, the harmonic distortion can be reduced as much as possible while keeping low switching frequency and switching losses.

Abundance of literature has been proposed on multilevel inverters. A new hybrid multilevel inverter is proposed in [5] and [7] which is the basis for the inverter topology used. The equal area criterion modulation technique is proposed in [9]. On this basis of modulation technique, the paper is proposed for 17 level multilevel inverter. The proposed inverter is asymmetric cascaded inverter type, which has different internal DC bus voltages, and uses different switching sequence of power semiconductor devices. This inverter topology uses the natural switching period and voltage blocking characteristics of switching devices effectively. As the level of the inverter increases, the quality of the output AC voltage improves thereby reduces the total harmonic distortion (THD) in the system. Also Genetic algorithms [10] is proposed for 17 level multilevel inverter. In this paper a comparison is made between equal area criterion and genetic algorithms for 17 level multilevel inverter topology for better THD values.

## II. PROPOSED 17 LEVEL MLI STRUCTURE

A new hybrid Multi-Level Inverter (MLI) topology is proposed, and it consists of two conversion cells such as Level Generating Cell (LGC) and Polarity Generation Cell (PGC). The basic level generation cell consists of a series combination of power switches, power source and a diode in parallel with both switch and a source. This series combination of such cells generates N-1 levels excluding zero level.

The Polarity Generation Cell (PGC) consists of the H- bridge connection with four switches. One step voltage source is connected in between LGC and PGC in order to obtain two or more levels compared to conventional N-Level MLI (without increasing any number of the device). In general, H-bridge is used for generating positive and negative half cycles. But in this topology, PGC is used for polarity purpose and as well as to control the step voltage which is connected to the H-bridge and it will generate three levels including zero level [5].

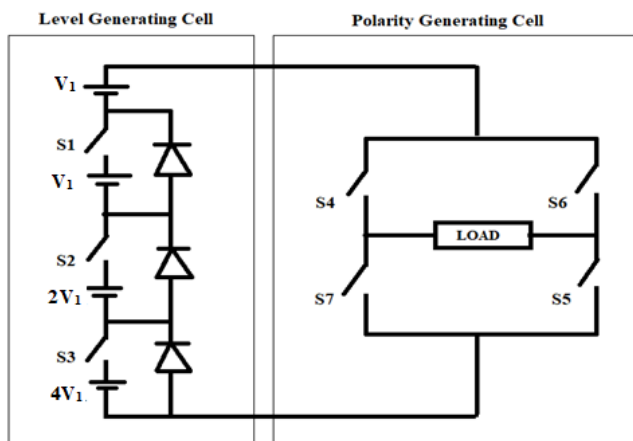


Figure 1: Proposed Hybrid Multilevel Inverter Topology

The general structure of a proposed hybrid multilevel inverter is shown in figure 1. This topology is built with two conversion cells, one is level generating cell and the second one is H-bridge for polarity generation as well as to control turn-on and turn-off of the one step voltage which is connected to the H-bridge [6].

The topology is made of 7 switches and 4 dc sources and is shown in Figure 1. The H-bridge is mainly used for polarity change as well as to control the minimum step voltage i.e.  $V_{dc}$ . Here, the Level Generating Cell (LGC) consists of four separate voltage sources with different voltage sources with different voltage ratio (i.e., 1:1:2:4) each voltage source is connected in series with another source with a power switch and one power diode that can generate the output voltage in +Ve polarity with multiple levels.

In general, H-bridge is used to generate +Ve and -Ve polarities across the load. But in proposed multilevel inverter the H-bridge not only used for polarity purpose but also to generate two more levels in existing conventional hybrid multilevel inverter. This configuration will increase two more levels without increasing number of power switches or diodes in conventional MLI. As results, the output voltage wave form smoothening with increased levels.

With this new topology, utilization of all power switches is increased in an effective manner towards the reduction of both expensive as well as switching losses and hence it increases the efficiency of the inverter. Increased number of levels makes the smoothness of output waveform and it reduces the effect of lower order harmonics on the fundamental component.

### III. METHODOLOGIES

#### Equal Area Criterion

Equal Area Criterion methodology is used in calculating the switching angles for the reduction of harmonic content at the output of a multilevel inverter. It is totally a different approach which does not need for solving the higher-order multi-variable polynomial equations for reducing harmonic content unlike Newton Raphson method [7].

In Equal Area Criterion (EAC) method, the best switching angles can be found by dividing the fundamental sine wave in small horizontal and vertical step voltages with respect to time as shown in the figure below. The steps are in such a way that the area of cross section of the previous step voltage (A1) and the succeeding step voltages (A2) are equal to get the lowest or minimal total harmonic distortion (THD).

For N-levels, the switching angles required =  $[(\text{Number of levels}-1)/2]$ .

From the formula, the number of switching angles required is found out. If  $a_1, a_2, a_3, a_n$ , are the switching angles for N-level inverter topology then total angles should be less than  $90^\circ$  i.e.  $0 < a_1 < a_2 < a_3 < a_4 < a_5 < a_6 < a_7 \dots a_n < 90^\circ$ .

To find the switching angle, i.e. Switching angle in (deg.) =  $[[\text{corresponding time of that switching angle}][2 * \text{fundamental frequency}]] * 180^\circ$ .

The switching angles obtained for 17- level inverter topology using above equations of equal area criteria are [9]:

$$a_1=5^\circ, a_2=11^\circ, a_3=18^\circ, a_4=27^\circ, a_5=34^\circ, a_6=45^\circ, a_7=54^\circ, a_8=71^\circ.$$

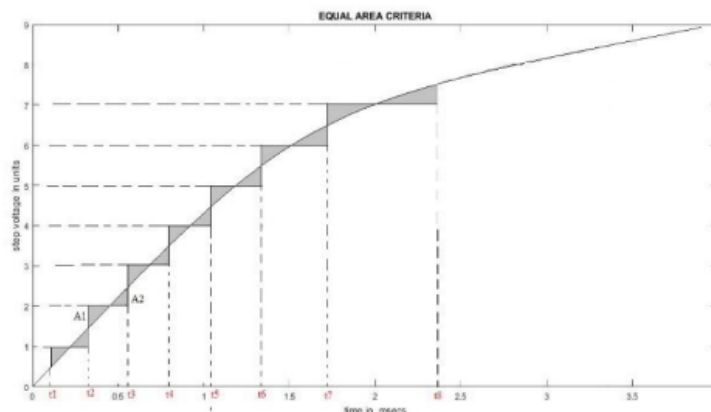


Figure 2: Equal area criterion

**Genetic Algorithms**

Genetic algorithms is a computerized search algorithm and optimization algorithm based on the natural selection process inspired by the Darwin’s theory of survival of the fittest. Genetic algorithms starts a randomized search to get the optimized solution of the problem and it has the ability to process large amount of data and give particular solution for the problem. The biggest advantage in this algorithm is that it does not requires any initial guess for searching [10].

A Genetic algorithms perform a multidimensional search where it starts with an initial random population set of chromosomes provided to it. With the objective function or the fitness function, the chromosomes ability to be the fittest among the population is looked for and it undergoes crossover and mutation process.

$$FV = \frac{\sqrt{\sum_{n=3,5,7,11,13} \left( \frac{1}{n} \sum_{k=1}^5 \cos(n\alpha_k) \right)^2}}{\sum_{k=1}^5 \cos \alpha_k}$$

The two or more chromosomes of the same generation undergoes reproduction operation to form offspring. Changing the gene structure of these chromosomes for obtaining optimal solutions is called as crossover function [11]. Mutation process is modification of the gene structure of the particular chromosomes itself. After undergoing this process, and with the help of fitness function, the best chromosomes are selected and it will be the optimized solution to the problem.

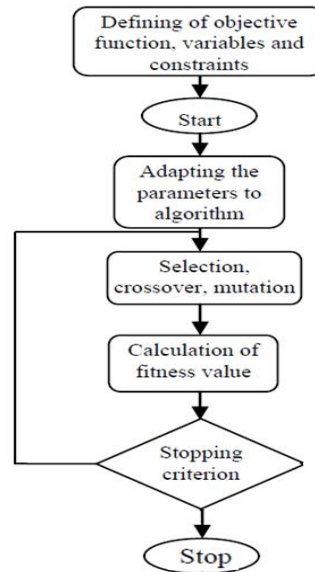


Figure 3: Flow chart to obtain switching angles using genetic algorithms

A new generation is formed by selecting, according to the fitness value. As the population size is constant, the suitable chromosomes having higher survivor capabilities according to fitness are selected. After several iterations, the algorithm converges to the best chromosome giving near optimal solution. Genetic algorithms have quite successfully been applied to optimization problem such as wire routing, scheduling, adaptive control, game playing, cognitive modelling, transportation problem, travelling sales men problem, optimal control problems, and database query optimization and so on.

**IV. SIMULATION RESULTS**

In this proposed 17 level multilevel inverter, the circuit consists of 7 MOSFET switches and 3 diodes. The output load is resistive and has a value of 10 ohms. The 100 volts asymmetric dc input voltages are used in the ratio of 1:1:2:4. Figure 4 represents the simulation circuit of the proposed 17 level inverter using equal area criterion. Figure 5 represents the generation of pulses for switching of MOSFETs and figure 6 represents the output voltage and current waveforms of the simulation respectively.

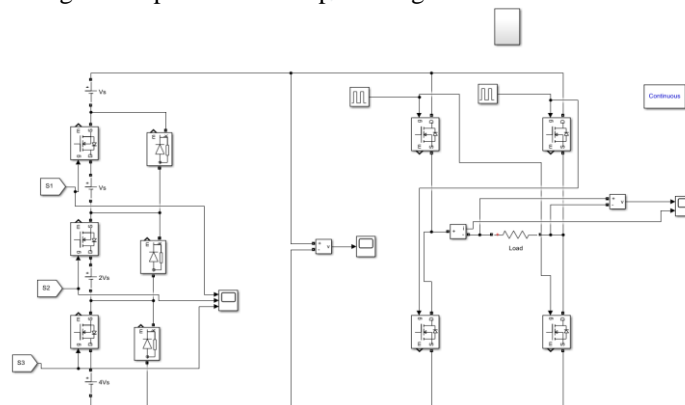


Figure 4: Simulation of seventeen levels multilevel inverter using equal area criterion technique

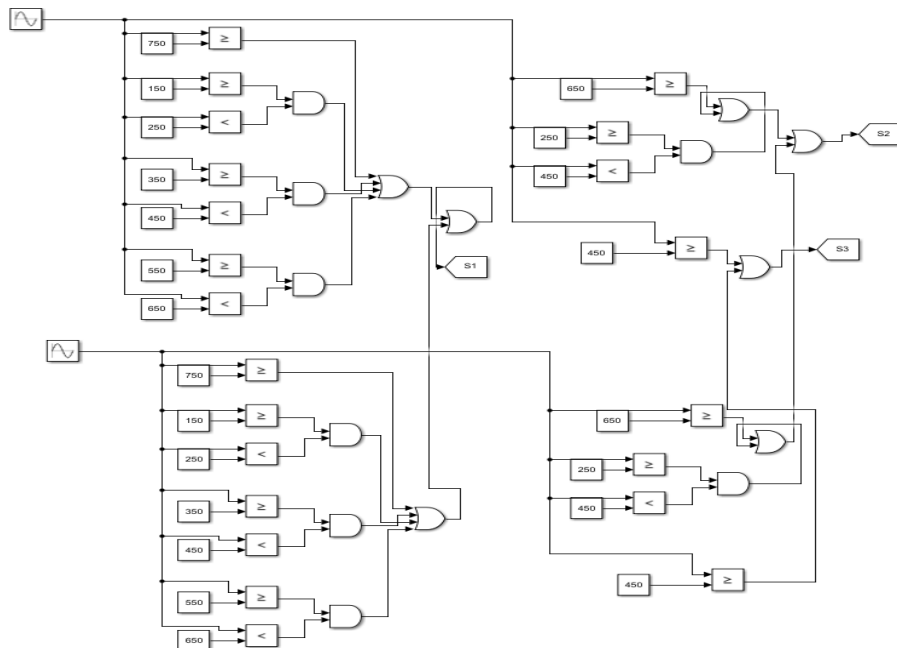


Figure 5: Generation of pulses for the switches of level generating cell

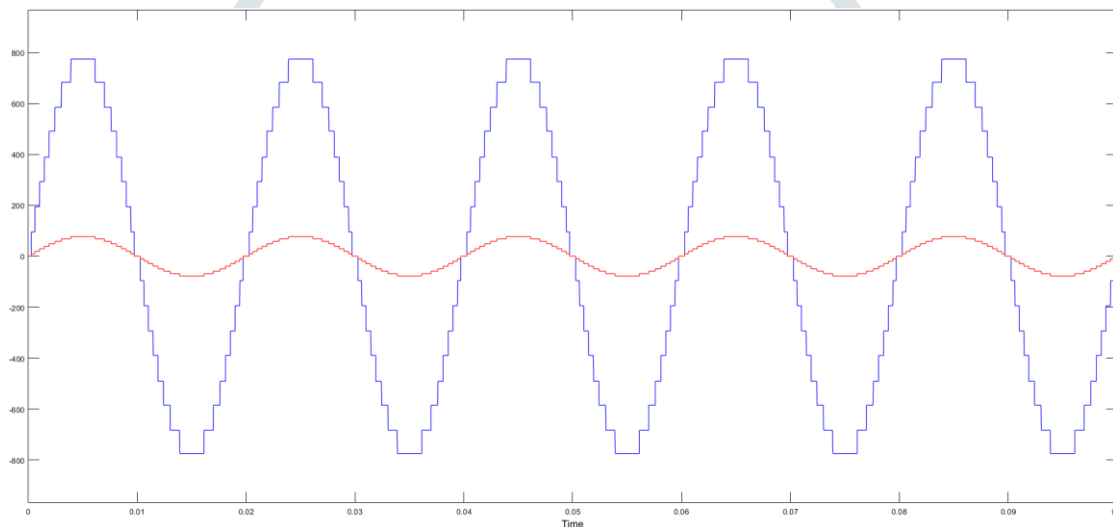


Figure 6: The output voltage and current waveforms of the simulated circuit using equal area criterion

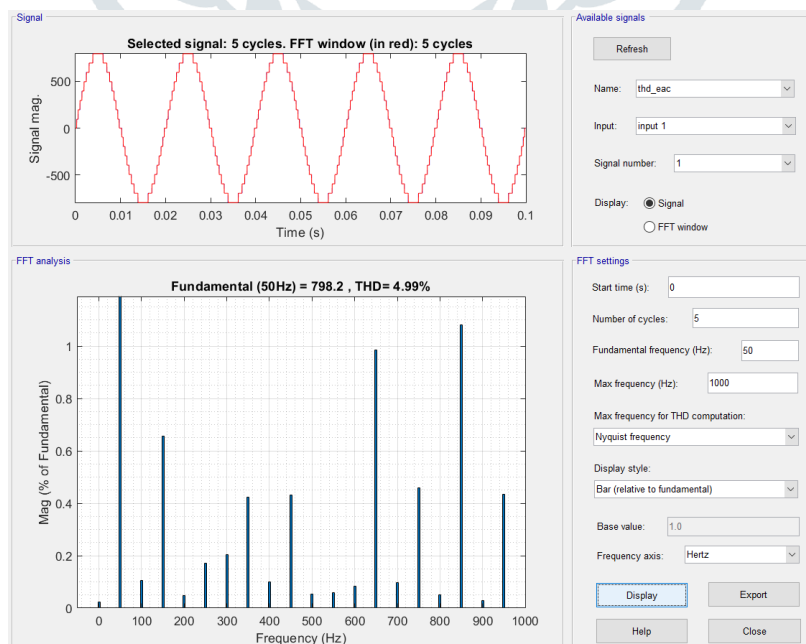


Figure 7: The FFT analysis of 17 levels MLI using Equal area criterion

Figure 7 shows the FFT analysis of the MLI using Equal area criterion. The total harmonic Distortion for 17 level MLI using Equal area criterion is 4.99% and it's well within IEEE standards.

Figure 8 shows the simulation of 17 level MLI using Genetic Algorithm technique. The circuit consists of seven switches and four asymmetrical DC voltage sources in the ratio 1:1:2:4.

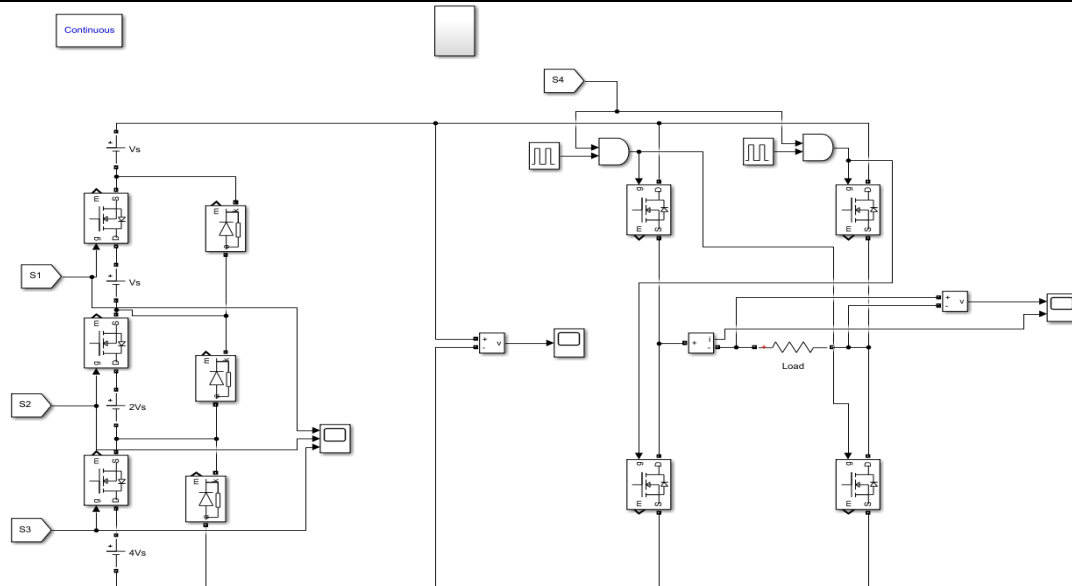


Figure 8: Simulation circuit of Seventeen levels multilevel inverter using genetic algorithm technique

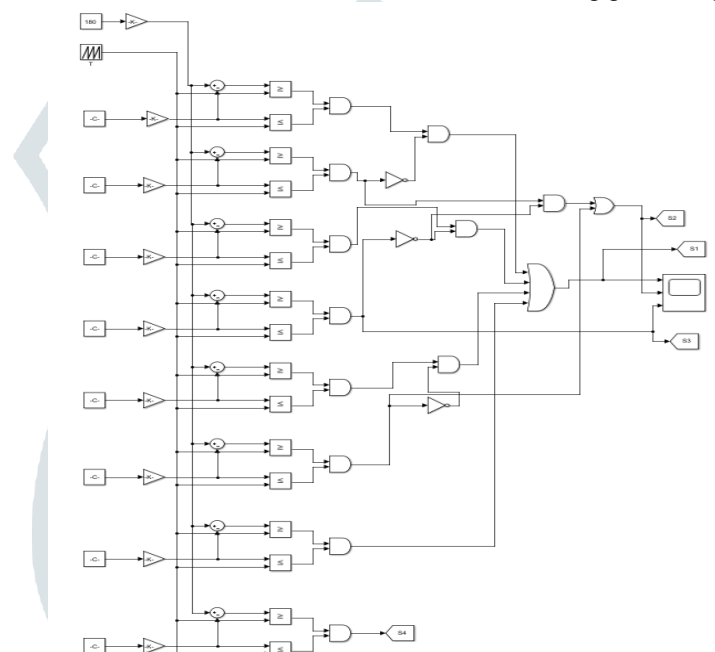


Figure 9: Pulse generation circuit for the power semiconductor switches in LGC

Figure 9 shows the pulse generation circuit for the power semiconductor switches used in LGC using genetic algorithm technique. Genetic algorithm technique is implemented in MATLAB for the generation of switching angles. These angles are called in the simulation circuit for the generation of pulses.

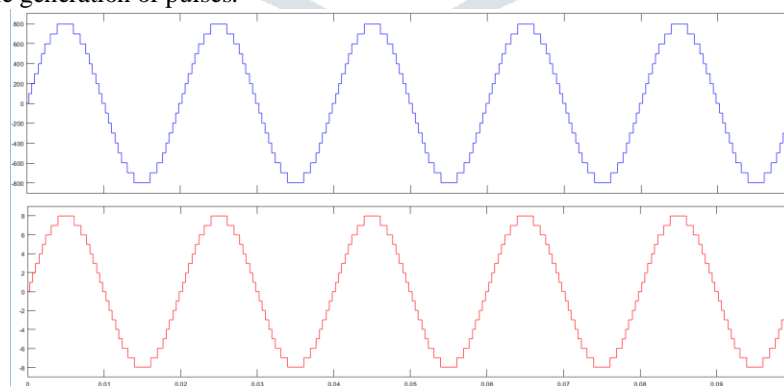


Figure 10: Output voltage and current waveforms of 17 levels MLI using Genetic Algorithms

Figure 10 shows the output voltage and current waveforms of 17 level MLI using Genetic Algorithm and Figure 11 shows the FFT analysis of 17 level MLI using Genetic Algorithm.

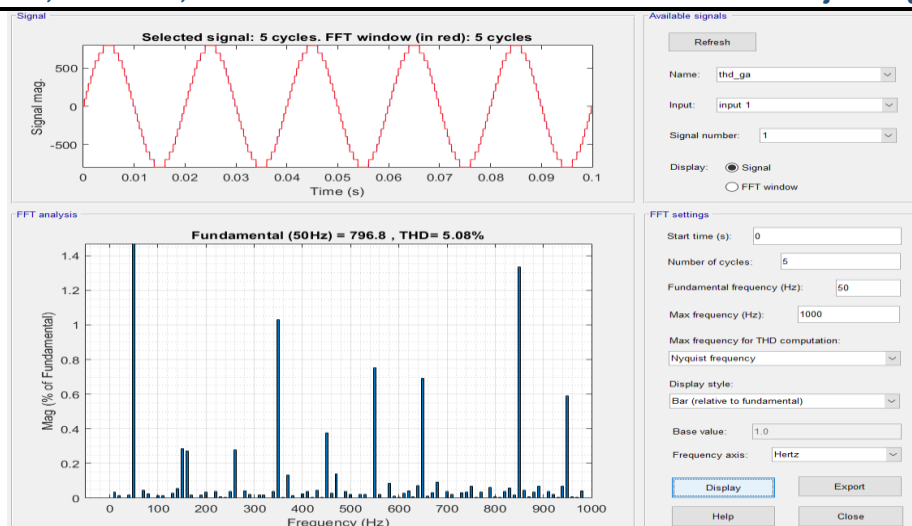


Figure 11: FFT analysis of the 17 levels MLI using Genetic Algorithms

### Comparison between Equal Area Criterion and Genetic Algorithm

Table 6.1 shows a comparison between equal area criterion and genetic algorithms for different parameters. From the above table, it can be inferred that equal area criterion has lower THD values compared to genetic algorithms and also the fundamental voltage component of the equal area criterion is higher than that of genetic algorithms. In the above table, a comparison of various harmonic order percentages are made between equal area criterion and genetic algorithms and are tabulated.

Table 4.1 Comparison between EAC and GA for different parameters

SL.NO	PARAMETERS	EQUAL AREA CRITERION	GENETIC ALGORITHMS
1	THD %	4.99	5.08
2	Fundamental voltage component	798.2	796.8
3	3 <sup>rd</sup> order harmonics %	0.66	0.28
4	5 <sup>th</sup> order harmonics %	0.17	0.04
5	7 <sup>th</sup> order harmonics %	0.42	1.03
6	9 <sup>th</sup> order harmonics %	0.43	0.38
7	11 <sup>th</sup> order harmonics %	0.06	0.75
8	13 <sup>th</sup> order harmonics %	0.98	0.69
9	15 <sup>th</sup> order harmonics %	0.46	0.07
10	17 <sup>th</sup> order harmonics %	1.08	1.33

### V. HARDWARE RESULTS

The experimental setup is shown in the Figure 12. The output waveforms displayed on the oscilloscope is shown in the Figure 13. The multilevel output voltage is obtained in hardware and it almost resembles that of the simulation. But when implemented in hardware, the output voltage is a little distorted. This may be due to noise signals generated in PIC controller while generating switching signals, inter capacitance between terminals in MOSFETs, inherent inductance and capacitance in other components etc. Implementation of high power multilevel inverter in hardware is difficult as large DC voltage requirements are essential. And this makes the system bulky and costly.

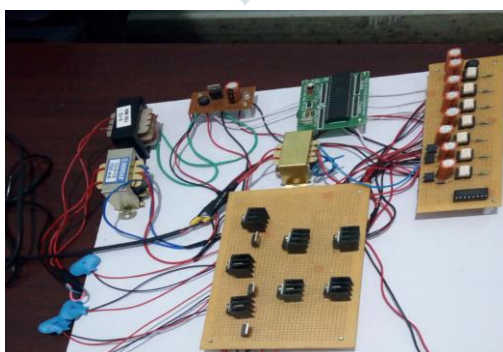


Figure 12: Experimental setup of proposed multilevel inverter

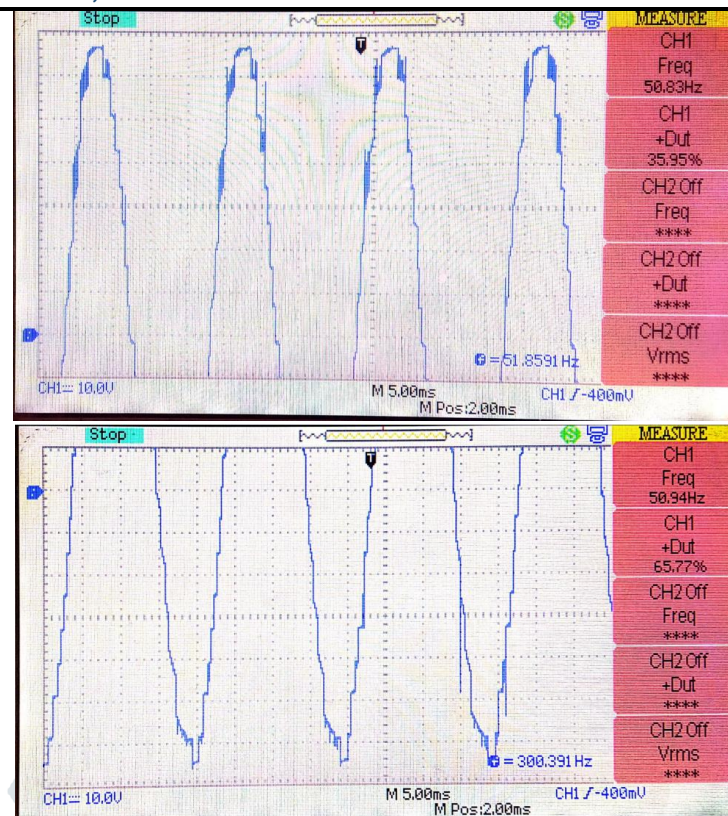


Figure 13: Output voltage waveform obtained from hardware setup

## VI. CONCLUSION

A comparative analysis of 17 level multilevel inverter using equal area criterion and genetic algorithms is presented in this project work. The 17 level MLI topology using equal area criterion technique gives a total harmonic distortion of 4.99% which is well within the IEEE standards and the AC output voltage waveform almost resembles the sine waveform. The 17 level MLI topology using Genetic Algorithms gives a total harmonic distortion of 5.08% which is also well within IEEE standards. From this we can conclude that equal area criterion technique shows a better THD results compared to GA.

Also the asymmetric hybrid inverter topology is the best topology among the inverter classification and it uses very less number of components when compared to other topology. The number of levels can be increased by connecting step voltage (minimum voltage) to the conventional topology without increasing any number of devices.

## REFERENCES

- [1]. José Rodríguez, Jih-Sheng Lai, and Fang Zheng Peng, "Multilevel Inverters: A Survey of Topologies, Controls, and Applications" in IEEE Transactions on Industrial Electronics, Vol. 49, No. 4, August 2002.
- [2]. Jih-Sheng Lai, and Fang Zheng Peng, "Multilevel Converters-A New Breed of Power Converters" in IEEE Transactions On Industry Applications, Vol. 32, No. 3, May/June 1996.
- [3]. Damoun Ahmadi, Ke Zou, Cong Li, Yi Huan, and Jin Wang, " A Universal Selective Harmonic Elimination Method for High-Power Inverters", in IEEE Transactions On Power Electronics, Vol. 26, No. 10, October 2011.
- [4]. Yun Zhang, Yun-ping Zou, Cheng-zhi Wang', Jie Zhang' and Zhen-xing Wu', "A Novel Modulation Technology for Multilevel Inverter Based on Equivalent Area", in The 33rd Annual Conference of The IEEE Industrial Electronics Society (IECON) Nov. 5-8, 2007, Taipei, Taiwan.
- [5]. H R Ramesh, Palemkota Mahesh and Dr. E.G. Shivakumar "Comparison of Hybrid Multi Level Inverter Topologies using Equal Area Criteria", in International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering Vol. 5, Issue 6, June 2016.
- [6]. Remyasree.R and Dona Sebastian "Fifteen Level Hybrid Cascaded Inverter", in International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering Vol. 4, Issue 9, September 2015.
- [7]. Palemkota Mahesh and H R Ramesh, "A New Topology Of Hybrid Multi Level Inverter With Equal Area Criteria Switching Technique" in Ijret: International Journal Of Research In Engineering And Technology, Eissn: 2319-1163 | Pissn: 2321-7308.
- [8]. J. Venkataramanaiah , Y. Suresh and Anup Kumar Panda, "Design And Development Of A Novel 19-Level Inverter Using An Effective Fundamental Switching Strategy", in IEEE Journal Of Emerging And Selected Topics In Power Electronics, Vol. 6, No. 4, December 2018.
- [9]. H R Ramesh and Dr. E.G. Shivakumar, "A Simplified Multi level Inverter Topology for Grid Interconnection of PV Systems International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering Vol. 5, Issue 6, June 2016.
- [10]. Madhusudhana J, P S Puttaswamy and SunilKumar, "Genetic Algorithm Based 15 Level Modified Multilevel Inverter For Stand Alone Photovoltaic Applications", in international journal of modern trends in engineering and research, Issn (online): 2349-9745, Issn (print): 2393-8161.

- [11]. Darshan Kumar, Dr. Swapnajit Pattnaik and Mrs. Varsha Singh, “Genetic Algorithm Based Approach for Optimization of Conducting Angles in Cascaded Multilevel Inverter”, in International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622, Vol. 2, Issue 3, May-Jun 2012, pp.2389-2395.
- [12]. Chiranjit Sarkar, Soumyasanta Saha, Pradip Kumar Saha and Goutam Kumar Panda, “Selective Harmonics Elimination Of Cascaded Multilevel Inverter Using Genetic Algorithm”, in International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE) Volume 2, Issue 12, December- 2013.
- [13]. Ranjhitha.G and Padmanaban.K, “Harmonic Minimization for Cascade Multilevel Inverter based on Genetic Algorithm” in International Journal of Innovative Research in Science, Engineering and Technology, Volume 3, Special Issue 1, Issn (Online) : 2319 – 8753,Issn (Print) : 2347 - 6710 February 2014.
- [14]. Burak Ozpineci, Leon M. Tolbert and John N. Chiasson, “Harmonic Optimization Of Multilevel Converters Using Genetic Algorithms”, in IEEE Power Electronics Letters, Vol. 3, No. 3, September 2005.

