Designing of D-Flip Flop under timing considerations for sequential circuit applications

SonalDahiya[a], Krishan Kumar[a]
[a]*Amity School of Engineering and Technology,*
Amity University Haryana,
Gurgaon, India

Abstract—***Digital design techniques contribute a very important role in VLSI designing. Growth in the complexity of circuits and performance requirements are driving force to use computer aided design tools. In this paper, our goal is to analyze the designing of sequential circuits and come out with solutions for the problems encountered during the designing of these circuits. Sequential circuits use complex clocking schedules and circuit structures to capture and store data signals. Design of a D-Dlip Flop under timing considerations is done in this paper so that it can be used as a component in sequential circuits.***

Keywords—D-Flip Flop, Sequential, Timing Metrices

I. Introduction

Digital circuits can be classified into combinational or sequential. Combinational logic output is entirely dependent on the current inputs levels. Although every digital system is likely to have combinational circuits, most systems also include storage elements,which result into another category of circuits,commonly known as sequential circuits. Unlike the combinational circuits, sequential logic output depends not only on present inputs but also on storage levels.
A basic block diagram of a sequential circuit is as shown below:

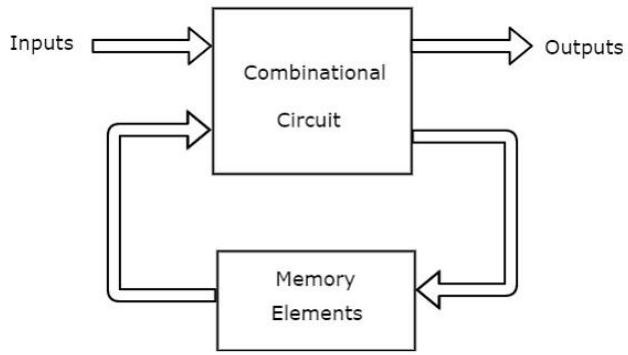

Fig 1. Block diagram of a sequential circuit

The block diagram shown above clearly demonstrates that the outputs in a sequential circuit are not only a function of the inputs, but also of the present stage of the storage elements. The next stage of the storage elements is also a function of external inputs and the present state. Thus, a sequential circuit is specified by a time sequence of inputs, outputs and internal states.
There are basically two main types of sequential circuits. Their classification depends on the timing of their signals. These are :-

1. Synchronous Sequential Circuits
2. Asynchronous Sequential Circuits

STORAGE ELEMENTS

In synchronous sequential circuits, the change of internal state occurs in response to synchronized clock pulses. On the other hand, asynchronous circuits do not use clock pulses.
The memory elements used in sequential circuits are basically of following two types. These are:

1. Clocked Flip Flops
2. Unclocked Flip Flops or Time-delay elements

These memory elements are used as memory elements in synchronous sequential circuits. Flip-flops are binary cells capable of storing one bit of information. It has two outputs, one for normal and one for the complement value of the bit stored in it. A flip-flop circuit can maintain a binary state indefinitely(as long as power supply is there) until directed by an input signal to switch states.
The various types of flip-flops are as summarized below:

1. **S-R Flip Flop**: The most fundamental latch is the simple SR latch (or simple **SR flip-flop**), where S and R stand for set and reset. It can be constructed from a pair of cross-coupled NOR (negative OR) logic gates. Normally, in storage mode, the S and R inputs are both low, and feedback maintains the Q and Q outputs in a constant state, with Q the complement of Q'. If S (Set) is pulsed high while R is held low, then the Q output is forced high, and stays high when S returns low; similarly, if R (Reset) is pulsed high while S is held low, then the Q output is forced low, and stays low when R returns low.
2. **J-K Flip Flop**: The JK flip-flop augments the behavior of the SR flip-flop by interpreting the S = R = 1 condition as a "flip" or toggle command. Specifically, the combination J = 1, K = 0 is a command to set the flip-flop; the combination J = 0, K = 1 is a command to reset the flip-flop; and the combination J = K = 1 is a command to toggle the flip-flop, i.e., change its output to the logical complement of its current value.
3. **D Flip Flop**: The D flip-flop can be interpreted as a primitive delay line or zero-order hold, since the data is posted at the output one clock cycle after it arrives at the input. It is called delay flip flop since the output takes the value in the Data-in. These flip flops are very useful, as they form the basis for shift registers, which are an essential part of many electronic devices.The advantage of this circuit over the D-type latch is that it "captures" the signal at the moment the clock goes high, and subsequent changes of the data line do not matter, even if the signal line has not yet gone low again.

4. **T Flip Flop** : It is a single-input version of the JK flip-flop.It is obtained from the JK flip flop when both inputs are tried together.The designation T comes from the ability of flip flop to “toggle” ,or complement its state.Regardless of the present state, the flip flop complements its output when the clock pulse occurs while T is 1.When T=0 ,the next state is the same as the present state and no change occurs.

II. TIMING PARAMETERS OF SEQUENTIAL CIRCUITS

Like combinational circuits, when sequential circuits, such as edge-triggered flip-flops, are physically implemented, they exhibit certain timing characteristics. Unlike combinational circuits, these characteristics are specified in relation to the clock input. Since flip-flops only change value in response to a change in the clock value, timing parameters can be specified in relation to the rising (for positive edge-triggered) or falling (for negative-edge triggered) clock edge. The following parameters specify sequential circuit behavior.

Unless otherwise specified, the following descriptions pertain to positive edge-triggered circuits. Similar definitions can be made for negative edge-triggered circuits.

1. **Propagation delay (tClk-Q)** -This value indicates the amount of time needed for change in the flip flop-clock input (e.g. rising edge) to result in a permanent change at the flip-flop output (Q). When the clock edge arrives, the D input value is transfered to output Q..

2. **Contamination delay (tcd)** -This value indicates the amount of time needed for change in the flip-flop clock input to result in the initial change at the flip-flop output (Q)..

3. **Setup time (ts)** -This value indicates the amount of time before the clock edge that data input D must be stable.

4. **Hold time (th)** -This value indicates the amount of time after the clock edge that data input D must be held stable. Setup and hold times are restrictions that a flip-flop places on combinational or sequential that drives a flip-flop D input. The circuit must be designed so that the D flip flop input signal arrives at least ts time units before the clock edge and does not change until at least th time units after the clock edge. If either of these restrictions are violated for any of the flip-flops in the circuit, the circuit will not operate correctly. These restrictions limit themaximum clock frequency at which the circuit can operate. If the rising clock edges in Figure 1 are too close together, data will not have enough time to propagate through the circuit to the flip-flop input and arrive ts time units before the rising clock edge.

GATE DELAYS

Transistors within a gate take a finite amount of of time to switch. This means that a change on the input of a gate takes a finite amount of time to Signal rise time Signal fall time cause a change on the output. This time is known as **Propagation Delay.**

Smaller transistors mean faster switching times. A Semiconductor companies are continually finding L new ways to make transistors smaller, which means transistors are faster, and more can fit on a die in H the same area.

1. **Tplh** --time between a change in an input and a low to high change on the output. Measured from 50% point on input signal to 50% point on the output signal. The ‘lh’ part (low to high) refers to H OUTPUT change, NOT input change.

2. **Tphl** --time between a change in an input and a L high to low change on the output. Measured from tplhtphl 50% point on input signal to 50% point on the output signal. The ‘hl’ part (high to low) refers to OUTPUT change, NOT input change.

III. DESIGN AND WAVEFORM

The master slave D flip flop that we designed is shown in the following circuit:

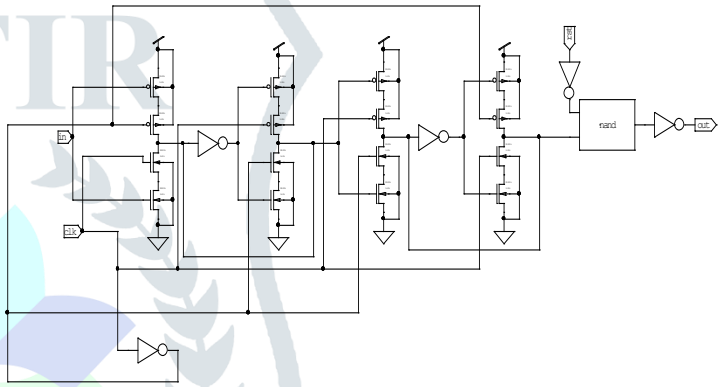

Fig 2: Circuit diagram of a master slave d flip flop

In this flip flop, the first part,i.e. the master is triggered at the positive edge of the clock while the slave is negative edge triggered flip flop.The output of this flop is ANDed with reset signal so as to initialize the output.

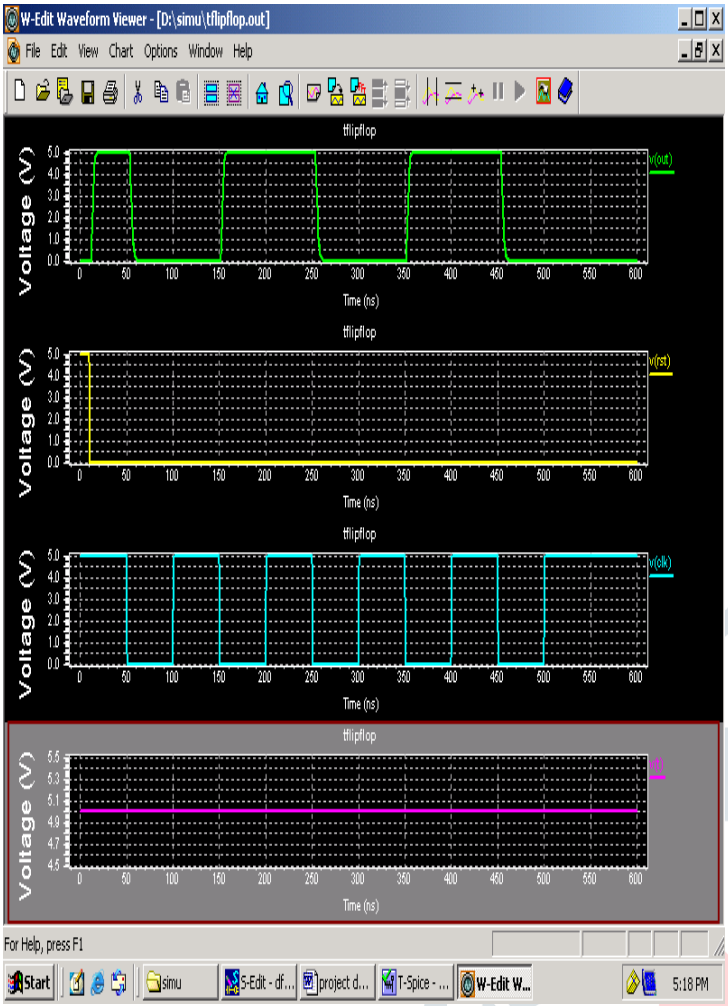

Fig 3: Waveform for design of fig2

IV. TIMING ANALYSIS

Set Up Time : 50% clock – 50% i/p value
= 40.5n – 37.57n
= 2.93 ns.

Hold Time : 50% i/p value – 50% clock
= 40.55n – 40.50n
= 0.05 ns.

PROPAGATION DELAY

High to Low : 50% o/p – 50% clock
= 40.99n - 40.50n
= 0.49ns

Low to High : 50% o/p – 50% clock
= 40.99n - 40.50n
= 0.49ns

V. CONCLUSION

Sequential circuits is a very broad topic and analysis done for these circuits is always insufficient. In this paper, we studied and analyzed the synchronous circuits along with their timing considerations. However; we could only calculate the set up, hold time and propagation delays for these circuits. The set up time for the designed D-Flip – Flop is 2.93 ns while the hold time is 0.05 ns., the propagation delay is 0.49 ns.

VI. REFERENCES

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