SMART ANALOG CIRCUIT SIMULATOR

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Abstract: The traditional teaching learning process with the limitation of visual experience makes it challenging for the teachers to deliver the concepts effectively, this made us to analyze the problem in terms of image processing and computer design automation, which can provide better solution. A tool that can automatically generate the waveform out of the captured circuit diagram would be extremely useful for them in their teaching. Unfortunately, such a tool does not exist yet. We present in this paper A prototype for CAD(Computer Aided Design) tool that offers this functionality. The tool, called Smart circuit's simulator is an attempt to address the above discussed challenges while focusing on electronic circuits. Applications of image processing in pattern recognition helps in recognizing the circuit elements of the circuit diagram. The task of image processing for circuit analysis is implemented as a chain of image processing algorithm.

Index Terms **- CAD, recognition, image processing, prototype..**

I. INTRODUCTION

Advances in digital technology have opened up many avenues of learning. Technology has made information accessible to all kinds of learners. To make the learning a better experience, technical institutions needs to adopt and update their teaching learning process with the inclusion of smart integrated technologies. In technical institutions, while handling engineering courses like circuits, machines, and hydraulics etc, for the sake of understanding the concepts teacher has to write the circuits on the board to analyze its outputs and related parameters with waveforms. Here, for every change in parameter the output/waveform also changes and it needs to be redrawn, which leads to difficulty for the teacher in terms of rewriting the waveform for every parameter changes. This ultimately results in tedious time consuming task of analysis. To make learning of engineering or science courses effective with emphasis on analysis and visualization, a sophisticated and smart technology needs to be developed. The proposed work, smart circuit's simulator is an attempt to address the above discussed challenges while focusing on electronic circuits in particular. Applications of image processing in pattern recognition helps in recognizing the circuit elements of the captured circuit diagram.

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1.1. CAD TOOLS AND TEACHING AID IN ENGINEERING

Use of advanced CAD analysis programs will help to overcome the barrier of fragmented learning in the development and reinforcement of skills among engineering students Computer-aided design (CAD**)** is the use of computers to aid in the creation, modification, analysis of a design **.** OrCAD, Ngspice , kTechLab KiCad ,freePCB , Electric, a proprietary software tool suite used primarily for electronic design automation(EDA)[1]. The software is used mainly by electronic design engineers and electronic technicians to create electronic schematics.This technology will then be used throughout the curriculum to teach the basic technical principles that they need in their professional career.

II. PROBLEM STATEMENT

Develop a prototype that can process circuit diagram, recognise the elements of the circuit, generate a netlist and facilitate to find output response.

The current problem can be defined in the mathematical model.

$$\{Nc, parameters, n\} = f(I) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

$$\{netlist, values\} = NLG\{Nc, p_1, p_2 \ldots\ldots p_n, n, I\} \ldots\ldots (2)$$

$$Response = netlist\}_{Pn} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3)$$

where, I = captured image, Nc= Number of components.

p1,p2.....pn = parameters of the captured circuit diagram. n=nodes of interest.

The input image I is processed to extract the connectivity information like, Number of components, parameters of the circuits and nodes of interest is as shown in the eqn1.using the connectivity information Netlist is generated is as shown in eqn 2. Netlist is processed with the given values to find the output response is as shown in eqn 3. The above mathematical model is illustrated in the Figure 1.

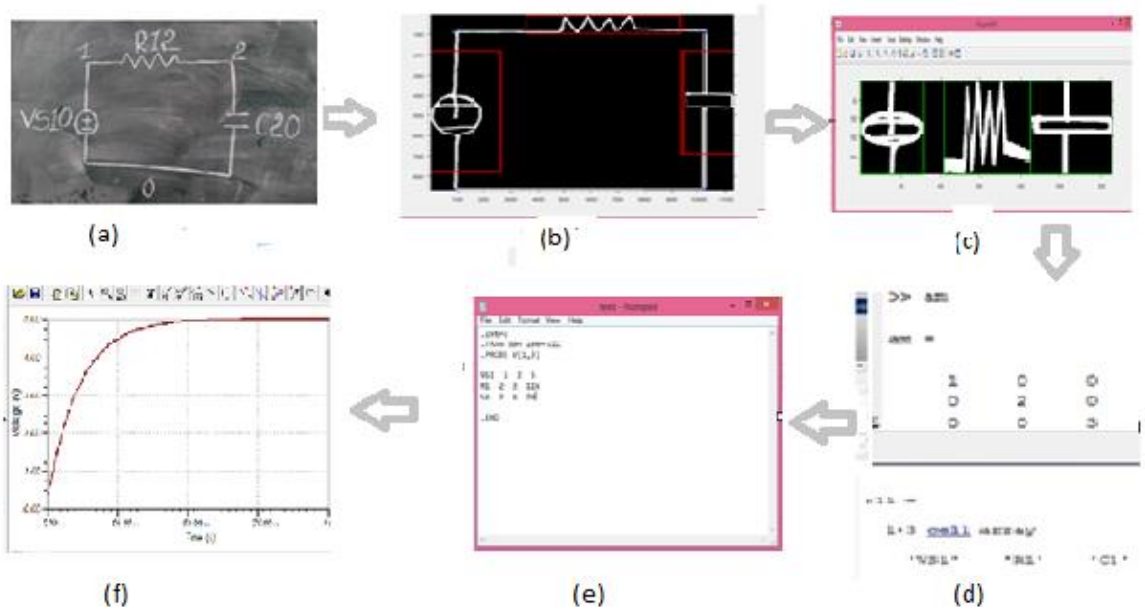

Figure 1: Illustration of the proposed work for Analog circuits.
(a) captured circuit image. (b)&(c) Extraction of circuit elements (d) Identification of the circuit elements and its connectivity. (e) Netlist generation. (f) Output response.

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. III. Framework for the Simulation of circuit Image.

Preprocessing, corner identification, circuit element identification, Image Segmentation, Template Matching, Netlist Generation, Simulation algorithms have been developed in this work. in this section, we shall see them in detail .

A. Preprocessing

Pre-processing operations include image processing, Gray conversion,, binarisation and removal of small objects [2],in pre-processing phase rgb image is converted into Gray image by forming a weighted sum of the R, G,and B components. That is given in equation (4).

$$g(x,y) = 0.299 * R + 0.587 * G + 0.114 * B \quad \text{…….. (4)}$$

Where, the coefficients that is used to calculate Gray scale values are identical to those values used to calculate luminance (E'y)in Rec ITU-R BT.601-7.

The resultant Gray scale image is converted into binary image because it specifically needs processing of shapes and links rather than colours. binarisation is the process which applies thresholding on to the Gray image with that pixels having the value less than the thresholding value is marked as zero and values greater than the thresholding value is marked as one is shown in equation (6).One of the algorithm underlying binarisation is the Otsu's method for the selection of threshold. To choose a threshold automatically by examining the histogram of image pixel values .The basic idea is to look for two peeks, representing foreground and background pixel values and pick a point in between the two peeks as the threshold value is shown in equation (5).

$$T = otsuthreshold(h(m)(g(x,y), -0.5{:}255.5)) \text{…… (5)}$$

Where, h(m) is the histogram, it is given by,

$$h(m) = \{(r,c)/I(r,c) = m\} \text{..... (6)}$$

Where, m spans the Gray level values.

$$ib(x,y) = \begin{Bmatrix} 0 & if\ g(x,y) \geq T \\ 1 & otherwise \end{Bmatrix} \text{…….. (7)}$$

Where, g(x, y) = gray image , ib =Binarised image, T=Threshold Value,

After the binarisation of the image, we are interested in processing the single loop circuit ,so it is necessary to remove small objects around the circuit image so that proposed algorithms can give more accurate results.The preprocessing steps are illustrated in the Figure 2.

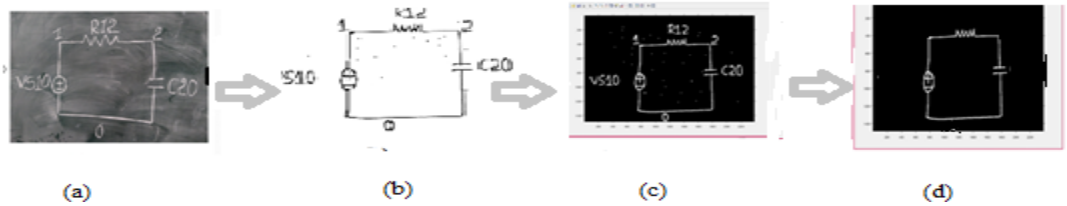


Figure 2: Preprocessing steps.
(a) Input image. (b)Gray Image (c) Binarised Image (d)Removal of small objects.

B. Identifications of Corners and connectivity

The circuit image contains information about the elements and their connectivity. The circuit image matrix can be processed to find out a set of linear equation by relating the nodes and elements of the circuit**.** To extract the connectivity information from the pre-processed image, it is necessary to Identify the corners. Each Corner consists of two coordinates (x(column pixel),y(row pixel)). To find the corner point divide the circuit horizontally two parts and find the maximum number of ones in each column. In which column it as maximum ones that is taken as x coordinate. To find the y coordinate, circuit image is divided into vertically two part find the maximum number of ones in each row.. In which row it as maximum ones that is taken as y coordinates. Remaining tentative nodes can be found by the same procedure with respect to the rows and columns. The four tentative nodes are plotted on the circuit image is shown in the Figure 3(b).

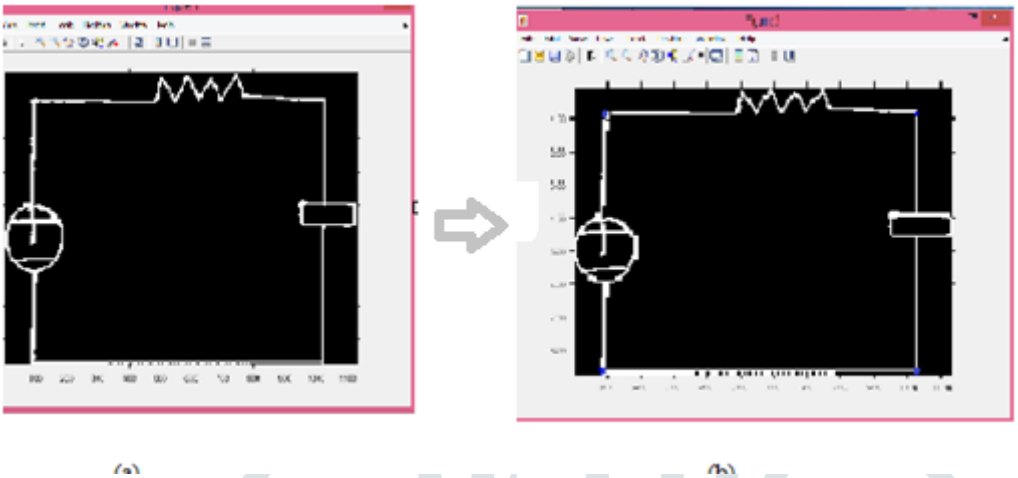


Figure 3: Corners Identification. (a) Pre-processed image. (b) Corner identification.

Connectivity Matrix: connectivity matrix can be designed to check is their any elements in between the two tentative nodes. Binary masking helps to mask the circuit elements and other connection retains as the same. Using the pixel value of the centroid(xc,yc) for every two nodes, connectivity is checked out and written in matrix. In the given circuit there are four tentative nodes. Between last two nodes there is no element in between the nodes and they are same nodes , so we have considered only three nodes, and it is shown in the Figure 4(b), the nonzero elements represents the nodes, zero represents there is no connectivity between tentative nodes.

Centroid can be represented as,

$$xc = (x1 + x2)/2 \dots\dots\dots\dots\dots\dots (8)$$

$$Yc = \frac{y1 + y2}{2} \dots\dots\dots\dots\dots\dots\dots (9)$$

$$Centroid = [xc, yc] \dots\dots\dots\dots\dots\dots (10)$$

Where, $x1$ is x coordinate of the first node. $x2$ is x coordinate of the second node.
$Y1$ is y coordinate of the first node. $Y2$ is y coordinate of the second node.

A basic concepts in image processing is that applying a mask to an image. The concept comes from the image processing operations of convolution. A mask is a set of pixels position and corresponding value called weights. The application of a mask to an input image yields an output image of the same size as the input for each pixel in the input image. For each pixel in the input image, the mask is conceptually placed on the top of the image with its origin lying on that pixel.

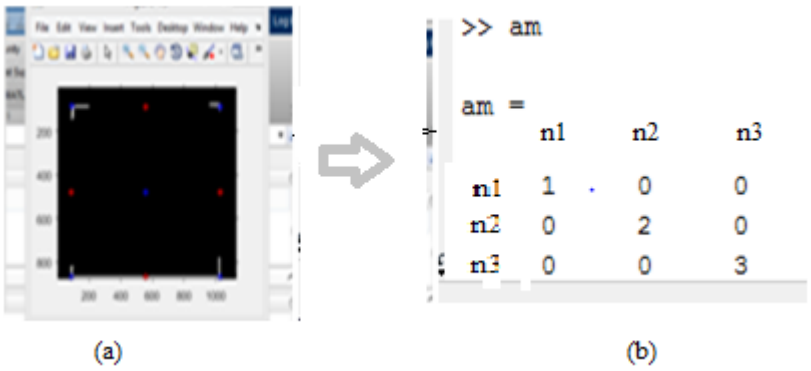


Figure 4: Circuit connectivity matrix.

C. Circuit Elements Segmentation

For the recognition of the circuit elements segmentation can be done as prior step for the template matching, segmentation is the process of simplifying and changing the representation of an image into sub images [4]. The main aim of circuit element segmentation is to determine the utility of conventional element recognition systems. using the extracted corner points bounding boxes are plotted around the elements to be extracted. Each bounding box represented in equation (11) is cropped to get the isolated circuit elements and they are stored in a matrix is shown in the Figure 5(b).

The plotted bounding box is represented as,

$$BoundingBox = [x0, y0, w, h] \ldots\ldots\ldots\ldots\ldots\ldots \quad (11)$$

Where, x0 and y0 are the coordinate of the upper left point. w,h are the width and height.

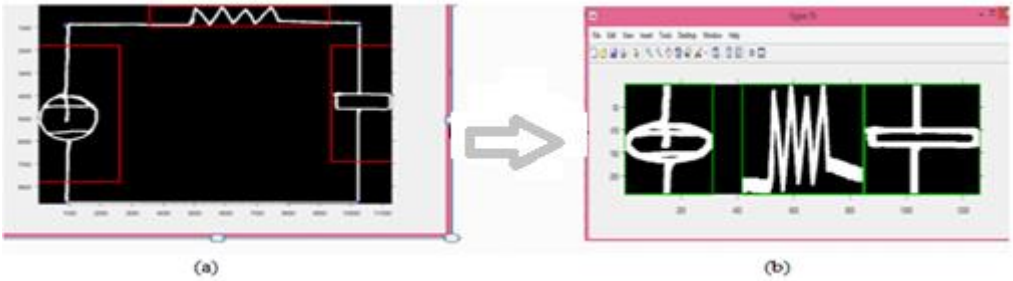


Figure 5: Circuit Element Segmentation. (a) Extraction of the elements using corners (b) Segmentation of the circuit elements

D. Identification of Circuit Elements

After the identification of tentative nodes and extraction circuit elements, it is necessary to identify the circuit elements between the tentative nodes. Identification of circuit elements is done by template matching criteria. Template matching is the process of finding the maximum possible correlation values of a symbol that best fits to the input image[3]. Processing steps of template matching is shown in Figure 6.

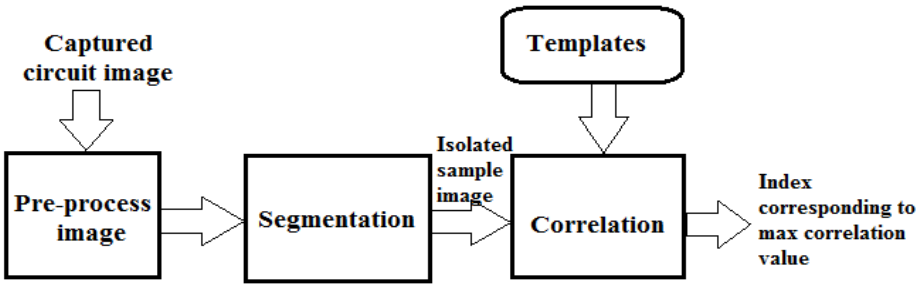


Figure 6: Template Matching

$$r = \frac{\sum_m \sum_n (A_{mn} - \bar{A})(B_{mn} - \bar{B})}{\sqrt{\left(\sum_m \sum_n (A_{mn} - \bar{A})^2\right)\left(\sum_m \sum_n (B_{mn} - \bar{B})^2\right)}} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (12)$$

Where,

$\bar{A}$ = mean2 (A), $\bar{B}$ = mean2 (B), A=input image ,B=template image,. m & n=pixel location.

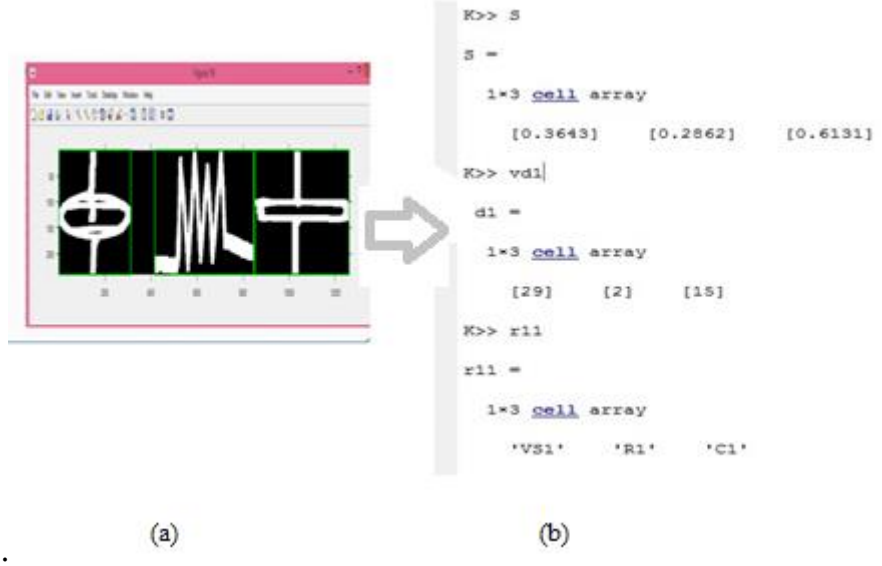


Figure 7: Circuit element identification (a)circuit element segmentation, (b) circuit element identification.

In the Figure 7(a) the circuits consists of voltage source resistor and capacitor as elements, using template matching criteria it is recognized as VS1,R1,C1 is as shown in the Figure 7(b). The recognition algorithm have been tested for test cases with different images is tabulated in the Table 1.

Table 1 : Result Accuracy

CIRCUIT	NUMBER OF ELEMENTS IN EACH CIRCUIT	ELEMENTS IN THE CIRCUIT	RECOGNISED ELEMENTS	NUMBER OF ELEMENTS ARE RECOGNIZED	% RECOGNIZATION	%FAILURE
CKT1	3	VS1,R1,C1	VS1,R1,C1	3	100	0
CKT2	3	VS1,R1,C1	VS1,R1,VS1	2	80	20
CKT3	4	VS1,R1,L1,C1	VS1,R1,L1,C1	4	100	0
CKT4	4	VS1,R1,L1,C1	VS1,R1,L1,R1	3	80	20

E. Netlist Generation

Electrical circuit analysis needs identification of circuit elements, nodes and relation between the parameters, the relation interms of netlist relating nodes and elements from the extracted connected informationand it is converted into PSpice netlist. PSpice Netlist is a description of the connectivity of an electronic circuit. It consists of a list of the electronic components in a circuit and a list of the nodes they are connected[5]. Generated PSpice Netlist is shown in the Figure 8(b).

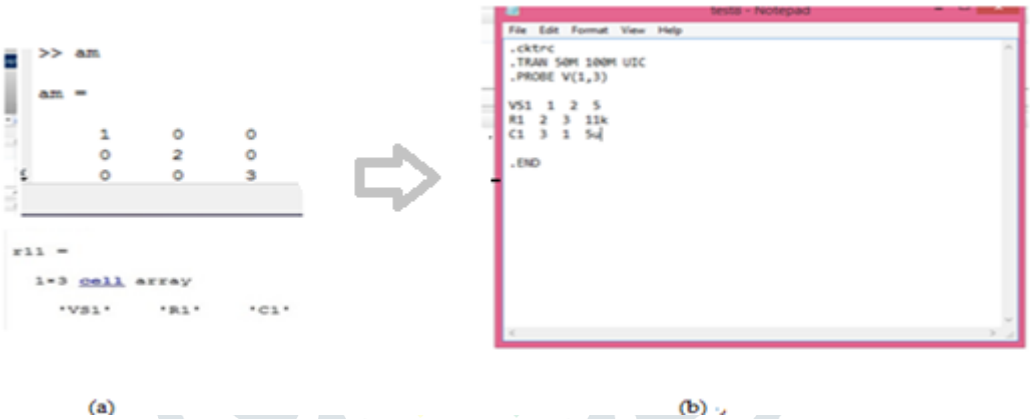


Figure 8: PSpice Netlist generation, (a) connectivity information, (b) PSpice Netlist

IV Flow Chart

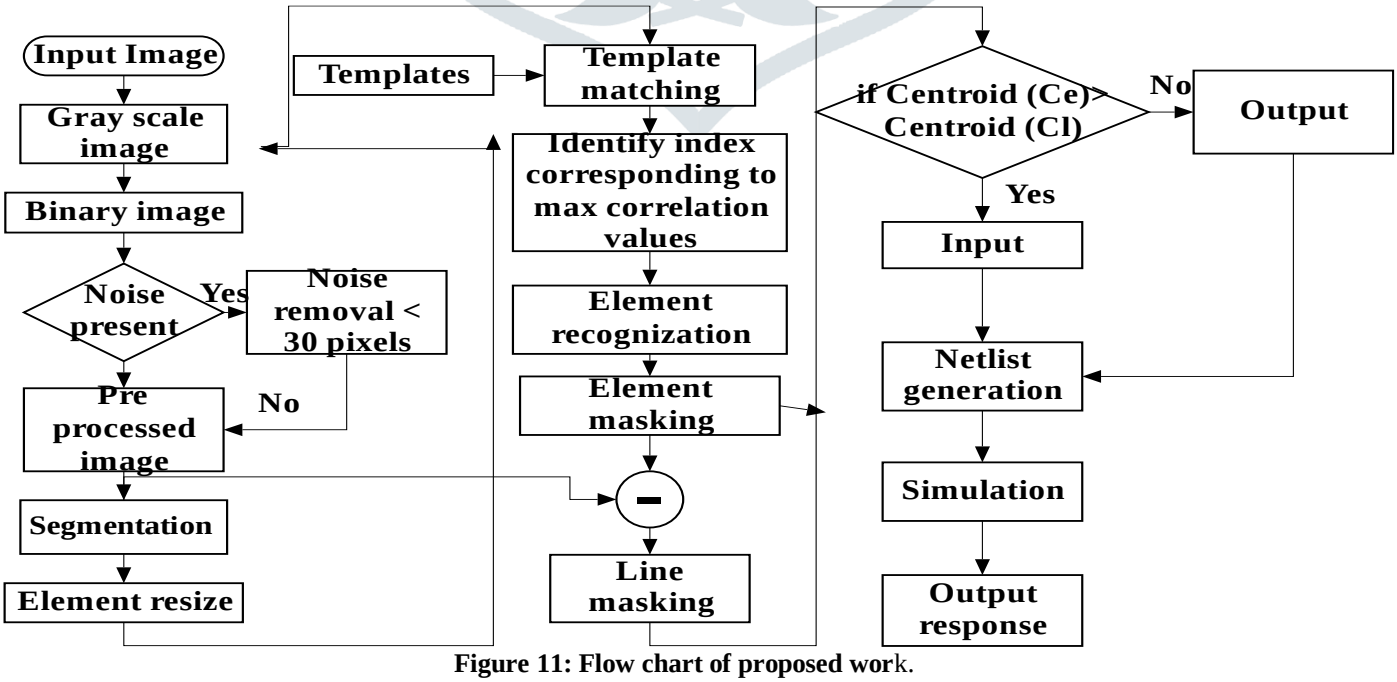
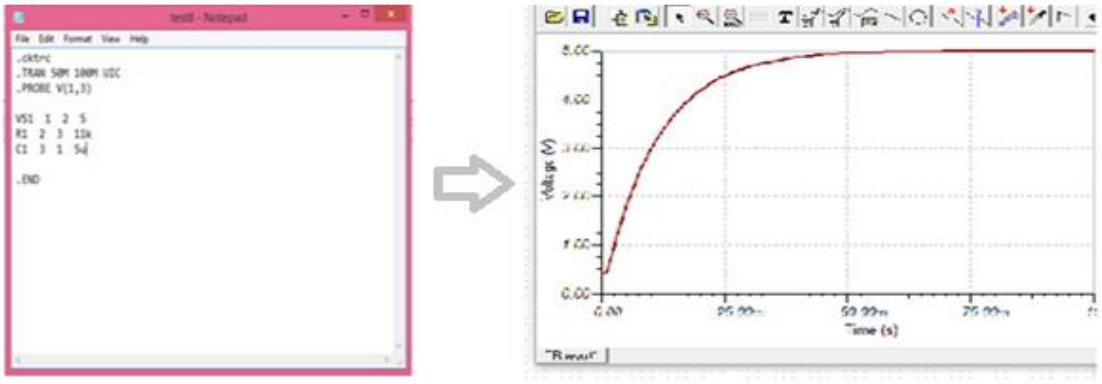


Figure 11: Flow chart of proposed work.

V Simulation Results

For the given input image we have extract and identified the circuit elements and their connectivity between the tentative nodes, using that information a PSpice Netlist is generated. For further processing the generated Netlist with the given values is fed to a PSpice model to find the output response is as shown in the Figure 10.



(a) (b)

Figure 10: Output Response (a) Generated Netlist, (b) Transient Analysis Of RC Circuit.

VI. Conclusion and Future work

A series of algorithms for element recognition, connectivity extraction have been developed.the algorithm have been validated with regressive simulation, the result of tests have shown better accuracy. Our work was basically focused on Template matching technique with good qualitative results, if basic circuit elements are considered. Some of the circuit elements deviated due to similarity between the elements. And we have taken the closed capacitor in the circuit image to avoid breakage in capacitor that will affects in segmentation, corner detection for generating a Netlist for multi loop circuits is still a challenging problem. Therefore, further work could be done to improve the system prototype into a better system by taking multi loop circuits.

Vii. Acknowledgments

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