PERFORMANCE ANALYSIS OF LOW-POWER HIGHSPEED HYBRID MODIFIED CONVENTIONAL TOWARDS 1-BIT FULL ADDERS

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ABSTRACT

The usage of digital devices is increasing rapidly and they became essential part of everyone's life. Digital devices can be designed according to their application and most of them are realized using arithmetic processor which consists of several operations like addition, subtraction, multiplication, etc., all of them can be implemented using full adder as the basic building block. As full adder plays a major role in digital devices we need to design a low-power full adder such that the devices can operate at lower power consumption and has longer battery life. In this research work, a hybrid low-power 1-bit full adder was designed using CMOS logic, pass transistor, and transmission gate logic with 14 transistor. The design was simulated using HSPICE tools in 90 nm technology with supply voltage of 1.2 V. Performance parameters, such as power, delay, and power delay product were compared with the existing designs, such as C-CMOS Full Adder, Mirror adder, hybrid pass-logic with static CMOS output drive full adder and found that the proposed adder has the low-power consumption and power delay product than the aforementioned adders.

KEYWORDS: Adder · CMOS · Pass transistor · XNOR · Low power.

INTRODUCTION

Full adder is the fundamental building block of all battery operated devices like mobile phones, personal digital assistants, laptops, and many useful electronic gadgets. This becomes a key factor for researches to propose or modify the existing adders such that the power and delay are reduced. Several designs of full adders were proposed [1, 2] regarding to power and efficiency. Full adder can be designed with different logic styles, each having its own advantages and disadvantages, these were studied to implement 1-bit full adder. The designs studied were classified into two categories static and dynamic. Static consumes less power and high area with reliability. But dynamic adder has lesser area compared to static adder [3, 4]. As mentioned above

full adder is basic block for complex circuits. As full adder reduces circuit complexity and hence used to construct higher bit adders and multipliers. Everyone is relying in battery and performance. Addition is the basic function used in arithmetic operations and used in biomedical applications. Processor chip which consists of ALU (Arithmetic Block unit) consists of full adder. This Block is used to make operations like addition, subtraction, multiplication, and many other operations. Basic operation of 1-bit full adder is to add three 1-bit numbers A, B, and Cin. A and B are the inputs, and Cin is a bit carried in from the previous stage. Different logic styles will have their own performance parameters at the cost of other parameter. Design which use combination of different traditional logic styles comes under hybrid design. Hybrid designs explore the merits of different logic styles to improve the performance parameters of the full adder.

CONVENTIONAL FULL ADDERS

Complementary CMOS Adder

The C-CMOS adder [3] shown in Fig. 1 is a regular pull-up and pull-down network. It consists of 28 transistors but it consumes more power and area due to more number of transistors.

Mirror Adder

Mirror adder [9] is based on the symmetrical arrangement of the NMOS and PMOS transistors. Carry in signal is connected to the transistors which are nearer to the output node such that the transistor can be optimized for the lesser delay of the adder. Transistors generating sum can be designed of small size. The arrangement of transistors is different and it also has 28 transistors as shown in Fig. 2.

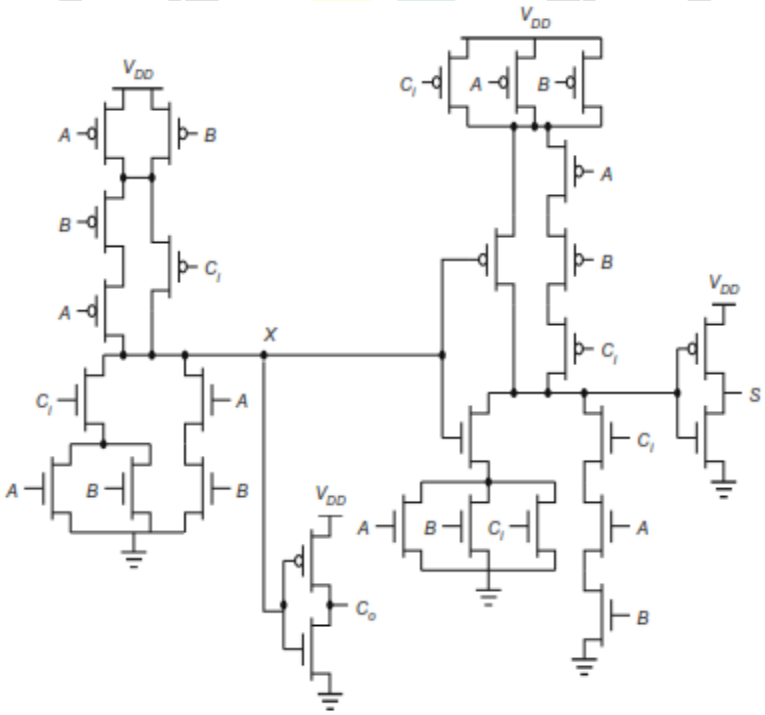

Fig. 1 Complementary CMOS adder circuit

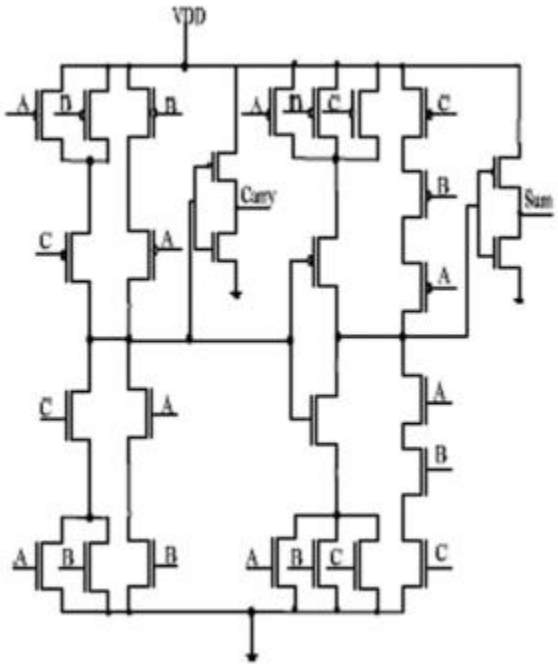

Fig. 2 Mirror adder

HPSC ADDER

The hybrid pass-logic (HPSC) full adder [9] shown in Fig. 3 uses 22 transistors and the equations used to design this adder are given in Eqs. 1 and 2.

$$\text{Sum} = \text{H xor Cin} \quad (1)$$

Where

$$\text{H} = \text{A xor B}$$

$$\text{Cout} = \text{A.H}' + \text{Cin.H} \quad (2)$$

Modified Low-Power Hybrid 1-Bit Full Adder

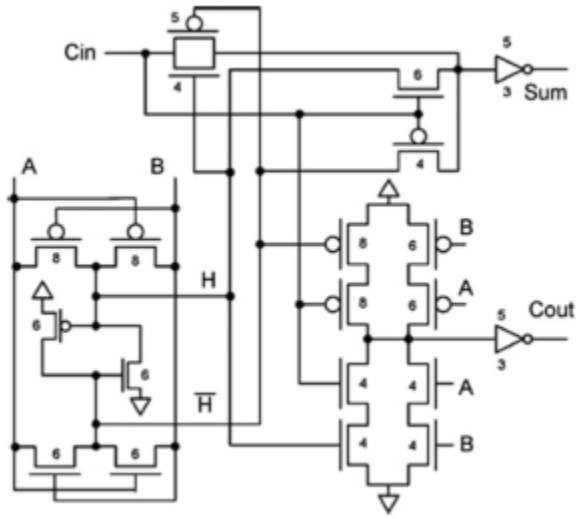

Fig. 3 HPSC adder

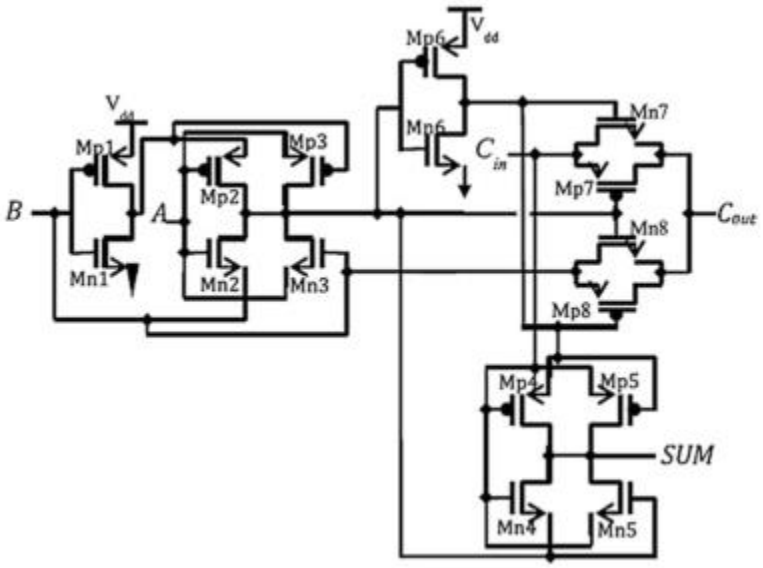

Fig. 4 Hybrid 1-bit full adder

HYBRID 1-BIT FULL ADDER

The hybrid 1-bit full adder [8] consists of 16 transistors is shown in Fig. 4 and is designed by XNOR and carry generation modules.

Proposed XNOR Circuit

The proposed XNOR circuit shown in Fig. 5 is designed with two NMOS and two PMOS circuits, where the nmos transistors are arranged as the pass transistor logic and it gives output as AND gate for inputs 00-0, 01-0, 10-0, 11-1, and when the input is 00 for XNOR we should obtain 1 as output so we use two PMOS transistors arranged in circuit such that it gives output as 1. Hence, we obtain 00-1, 01-0, 10-0, 11-1.

Proposed Adder

The 1-bit full adder designed by considering the above circuits and proposed XNOR circuit such that the optimal value of power and delay were obtained without degrading the output and the swing of output is obtained successfully.

Implementation. The proposed full adder circuit block diagram is shown in Fig. 6. Sum signal is generated by the first two modules, i.e., 1 and 2 which are XNOR modules and the output carry signal is generated by carry generation module, i.e., 3. Now the basic element is XNOR in full adder so we use proposed XNOR module to reduce power. The proposed 1-bit full adder is shown in Fig. 7 and it consists of proposed XNOR circuit as module1 and the other XNOR module is taken from the design of hybrid 1-bit full adder such that the output swing is restored and the carry generation module is designed with transmission gate. The proposed 1-bit full adder consists of 14 transistors which are less than hybrid 1-bit full adder.

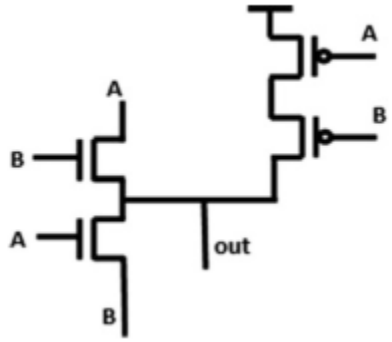

Fig. 5 Proposed XNOR gate

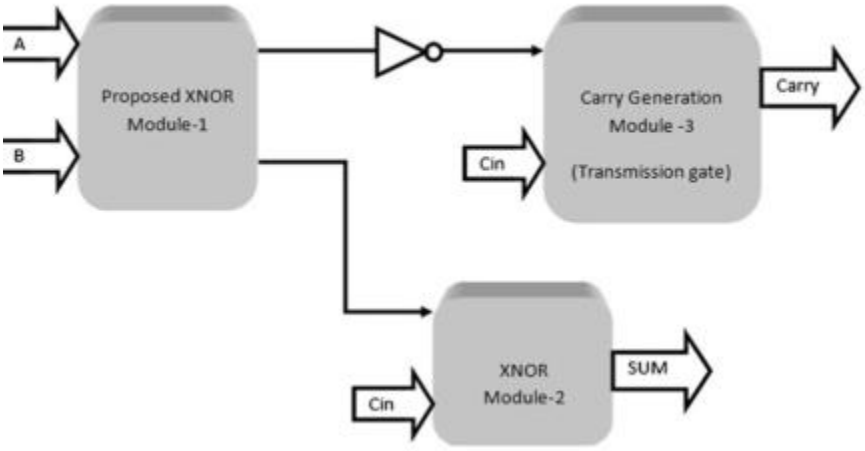

Fig. 6 Block representation of proposed full adder

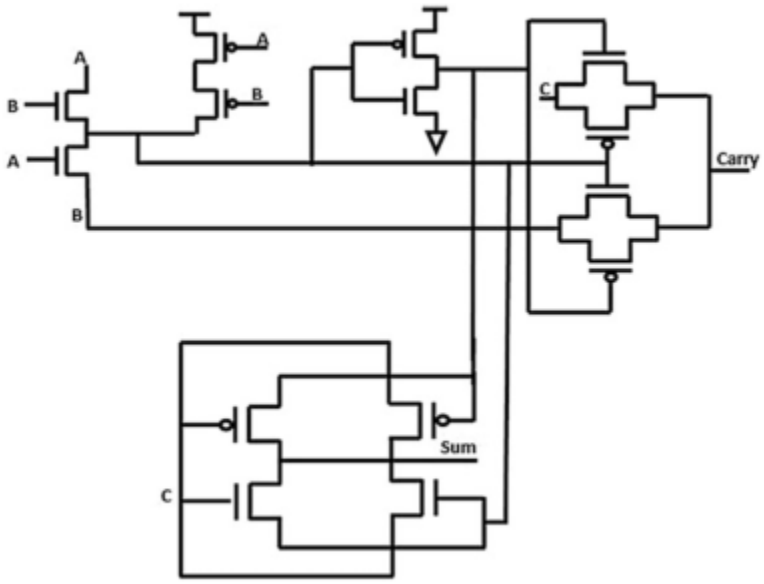

Fig. 7 Proposed full adder

CONCLUSION

In this research work, the simulation and analysis of C-CMOS adder, Mirror adder, HPSC adder, and hybrid 1-bit full adder are carried out using HSPICE with 90 nm technology. As the Hybrid adder is divided into modules and XNOR being the basic module for power consumption different XNOR circuits were considered and simulated in HSPICE 90 nm technology with supply voltage of 1.2 V and found proposed XNOR has the lowest power consumption of 0.34 µw. A full adder was designed by using proposed XNOR with 14 transistors and simulated using HSPICE 90 nm technology and found that power consumption of proposed adder, i.e., 0.59 µw is low compared to the benchmark circuits, i.e., C-CMOS adder, Mirror adder, HPSC adder and hybrid 1-bit full adder which has power consumption 1.46, 1.1451, 1.034, and 0.954 µw, respectively. When delay is compared there is a slight increase compared to the hybrid 1-bit Full adder but has the low-power delay product than benchmark circuits.

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