A 12-BIT SAR ADC WITH NON-LINEAR CAPACITANCE DAC SWITCHING SCHEME IN 32-nm CMOS

Dr.M.Deepa, Associate professor, ECE department, Usha Rama College of engineering and technology, Telaprolu
K.Savikhya (17NG5A0402), K.Radhika (16NG1A0427), G.V.Samyuktha (16NG1A0421),G.Naveen Kumar (16NG1A0418)
final year students, ECE department, Usha Rama College of engineering and technology, Telaprolu.

Abstract: In this work presented an ultra-low power 12 bit asynchronous analog to digital converter with successive approximation technique. The major design consists of five blocks those are non- binary array of capacitors, retiming clock generation unit, comparator, self-timed loop and SAR logic. These all blocks are utilized to decline the power consumption and delivers the accurate results. In this non-linear capacitance correction method and latch output glitch removal correlation method has been employed, SAR logic gives the improved speed of operations and reduces the power consumption by 1.2mW in a 32-nm CMOS technology.

Index terms **–** successive approximation register (SAR), capacitor array ADC, 32-nm CMOS technology.

Introduction:

Analog-to-digital converters (ADCs) with high sampling rate and medium resolution are important building blocks in instrumentation (oscilloscopes, spectrum analyzers, medical imaging), video applications and wireless communication. Successive approximation register (SAR) ADC architectures offer a compact and power efficient alternative but are generally designed for lower frequencies. High performance VLSI designs are very much useful for current technologies, but conventional designs do not reach the operational rate compared to present industry. In this work proposes a 32-nm analog to digital converter design with 12 bit outcomes. In addition, considering its structural characteristic, it's far appropriate for designing a small and narrow size time- interleaved ADC (TI- ADC) channel. There are many techniques that have been said for implementing moderate- overall performance SAR ADCs. The SAR ADC uses a couple of comparators to acquire excessively. This approach is at the price of hardware complexity in change for tempo. So, the small unit capacitor is used inside the digital-to-analog converter (DAC) capacitor array for excessive-pace and low power consumption underneath the hindrance of kT/C noise.

However, with small DAC capacitors, a spread of things will restrict the ADC performance, which includes capacitor mismatches, the top plate parasitic capacitors, the comparator input nonlinear parasitic capacitors and the leakage and clock feed through of the plate switches. Non-binary capacitor array and asynchronous timing are used to rush up the complete ADC. Due to non-binary redundancy and the proper capacitor switching scheme, incomplete settling of DAC reference voltage is authorized. And asynchronous timing lets in for efficient use of spare time compared to synchronous timing. As the comparator is one of the block which limits the speed of the converter, its optimization is of utmost importance. The preamplifier stage amplifies the input signal to improve the comparator sensitivity and isolate the input of the comparator from switching noise coming from positive feedback stage.

The latch stage is used to determine which of the input signals is larger and extremely amplifies their difference. The output buffer amplifies the information from latch and outputs a digital signal. The latched comparator is used for the clock signal and indicate digital output level, whether its differential input signal is positive or negative. A positive feedback mechanism to regenerate the analog input signal into a full scale digital signal is much faster and power efficient than performing multi-stage linear applications. The preamplifier latch comparator, which combines an amplifier and a latch comparator can be obtained high speed and low power dissipation. The amplifier which is added before the latch can reduce offset voltage to obtain a high resolution. This type of latched comparator was also used for high speed and low power performance cannot be tolerated.

This paper proposes a 12-bit low-electricity SAR ADC with a 0.9V supply. The architecture and the calibration allow the downsizing of DAC unit capacitor Cu to that of the kT/C noise restriction. To beautify the accuracy and pace of the comparator at a low-power supply, the proposed nonlinear capacitance correction method and latch output glitch removal method are used.

Furthermore, The SAR ADC changed into fabricated the use of a 32-nm CMOS technology. The ADC is achieved and consumes 1.2mW at a sampling rate of 100 MS/s.

SAR ADC:

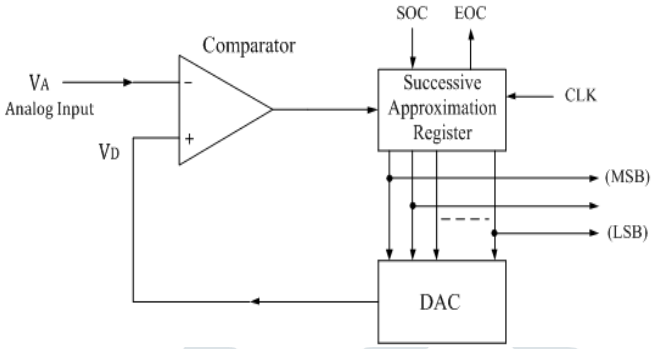

Fig1: General SAR ADC block diagram

The successive approximation analog-to-digital converter circuit typically consists of four chief sub circuits (a) A sample and hold circuit to acquire the input voltage (V_{in}). (b) An analog voltage comparator that compares V_{in} to the output of the internal DAC and outputs the result of the comparison to the successive approximation register (SAR). (c) A successive approximation register sub circuit designed to supply an approximate digital code of V_{in} to the internal DAC. (d) An internal reference DAC that, for comparison with V_{REF}, supplies the comparator with an analog voltage equal to the digital code output of the SAR_{in}.

Proposed system:

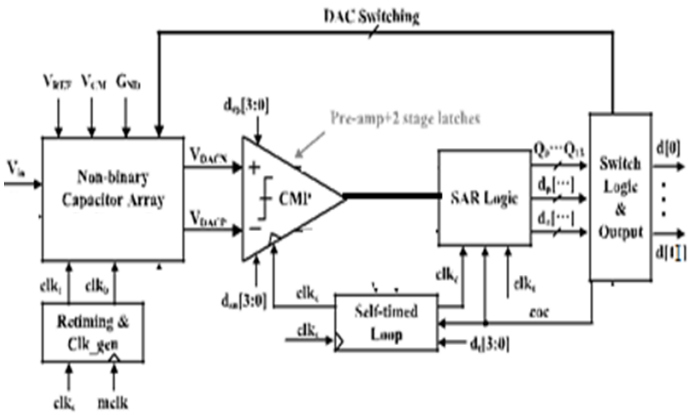

Fig2:Proposed system block diagram

The absolutely differential configuration benefits from advanced not unusual-mode noise rejection, a doubling of the signal voltage range, and a discount of even harmonic distortion. Moreover, all key modules on this SAR ADC are designed for low-voltage operation, in particular the DAC (nonbinary and small unit capacitor) and the comparator (preamplifier and -level latches). Like maximum asynchronous SAR ADCs, there are key loops: Loop I and Loop 2. The slowest loop determines the most speed of the SAR ADC, the put off of Loop 2 is the number one issue that limits the ADC pace. The proposed excessive-velocity SAR desirable judgment is aimed at decreasing the elimination of Loop 2 by enhancing the ADC velocity. To avoid using an excessive-frequency clock generator and make full use of quantization time, asynchronous timing is used inside the ADC.

Non-binary capacitor array:

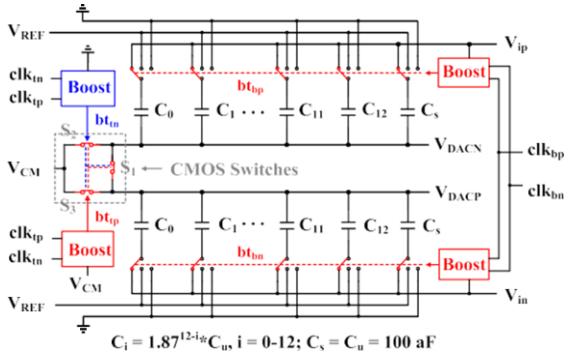

Fig3: Non-binary capacitor array

Non-binary capacitor array consists of top plate structure and bottom plate structure. Although the small unit capacitor gives the blessings as defined earlier, it ends in the rate injection and leakage issues of the top plate. CMOS switches are used as the top plate switches with a purpose to lessen the rate injection and clock feed through where the ratio of the dimensions of the pMOS to that of nMOS (Wp/L p:Wn/Ln) is equal to 3:2. And long channel length gadgets are accompanied to lessen leakage. The pinnacle plate switches also are managed by means of a bootstrapped clock signal to reduce ON-resistance of the switches. In addition, the n-type three-transfer is brought to similarly reduce the ON-resistance and to decorate the settling speed and accuracy of VCM.

Effect of capacitor mismatch:

When electronic components are fabricated some variation in their properties, such as device dimensions and layer thickness, is inevitable. Systematic errors such as a slightly higher or lower unit capacitance, typically related to "global" variations during chip production, are usually not a problem. Relative errors,e.g. mismatch between unit capacitors due to differences within a chip, can on the other hand cause deviation from the ideal transfer curve of the DAC resulting in a distorted output. This makes matching of unit capacitors critical for the accuracy and resolution of the entire ADC. The output voltage of a capacitive DAC is determined by the fraction of the total capacitance C_{tot} connected to the reference voltage. With x unit capacitors connected to V_{ref} the top plate voltage becomes:

$$V_X = \frac{C\,ref}{C\,tot} Vref$$

Comparator:

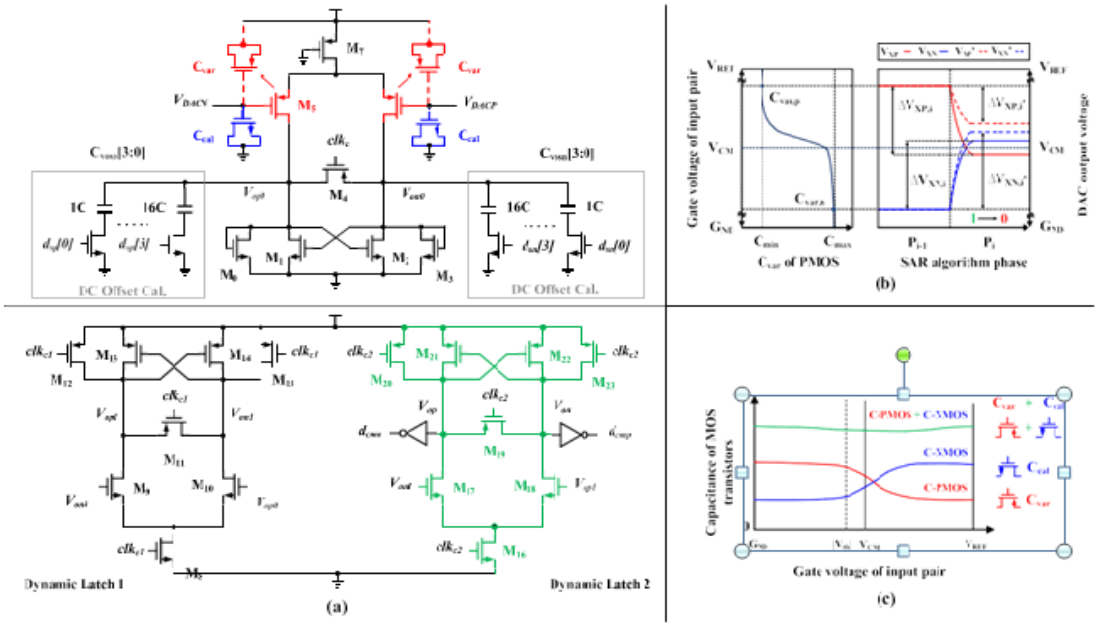

Fig4: Proposed low-voltage and high-speed comparator. (a) Schematic of comparator including a preamplifier and two latches. (b) Effects of nonlinear parasitic capacitors. (c) Correction principle of the nonlinear capacitor.

For excessive decision and excessive- pace at a low energy supply, the comparator consists of a preamplifier and -level dynamic latches. Fig. 4(a) suggests the schematic of the comparator with the nonlinear parasitic calibration capacitors. The dc offset is calibrated by way of manner of sixty capacitors which might be managed During the reset section, the outputs of the preamplifier are equalized through M4. This is useful to the subsequent settling whilst the differential voltage modifications from large signal to small sign. Considering the energy consumption, the dynamic latch is used inside the comparator. For lowering the circuit noise, the comparator makes use of a p-kind MOS enter pair. When shrinking the DAC unit capacitor to the volume of dozens to hundreds of aF for excessive-pace and espresso strength intake, the enter parasitic capacitor of the comparator ought to be considered.

Parasitic capacitors C_{var} of input pair are MOS transistor capacitor , which might be nonlinear capacitors. This paper proposes a completely unique solution. Another simplified latch is used which follows the previous latch, and the design makes use of a not on time control clock clkc2. Both the 2 methods grow the delay of comparator moreover. However, the latter is more reliable and has the capability of running at a low deliver voltage than the previous whilst thinking about the approach sorts. Fig.4 indicates the effect of the trade of the reversal threshold at the put off of an inverter. Under the equal threshold voltage (V_T) variant, the lower the brink voltage is, the more the delay variation. The value of d_t[3:0] is determined by judging whether the EOC signal is generated, that is, whether ADC quantization is completed. Under the premise that ADC can accomplish quantification, increase the value of d_t [3:0] manually and make the remaining time as much as possible allocated to each bit DAC establishment time.

SAR cell:

In the high-speed asynchronous SAR ADC, the delays of two loops are key aspects of the design. The first loop (Loop 1) is the self-timed loop of the comparator, and its delay is t_1; the second loop (Loop 2) is from the SAR to the switching control logic, finally to the DAC, and its delay is t_2. In this design, $t_2 > t_1$, and thus, t_2 determines the maximum achievable speed of the SAR ADC. One way to effectively reduce t_2 is to reduce the SAR cell's delay t_{SAR}. Below fig and the proposed simplified block diagram of single SAR cell with comparator the detailed timing diagram of a single comparison cycle t_{cycle} in traditional SAR and the proposed SAR, where t_{cmp} is the comparison time, t_{cmp_rst} is the comparator reset time, t_{d0-3} are the additional logic delay in order to meet the timing, t_{DAC} is the DAC settling time, t_{eol} is the logic delay of the end of latch (EOL) generation circuit, t_{clk} is the logic delay of the clock generation circuit, and t_{latch} is the logic delay of the data register.

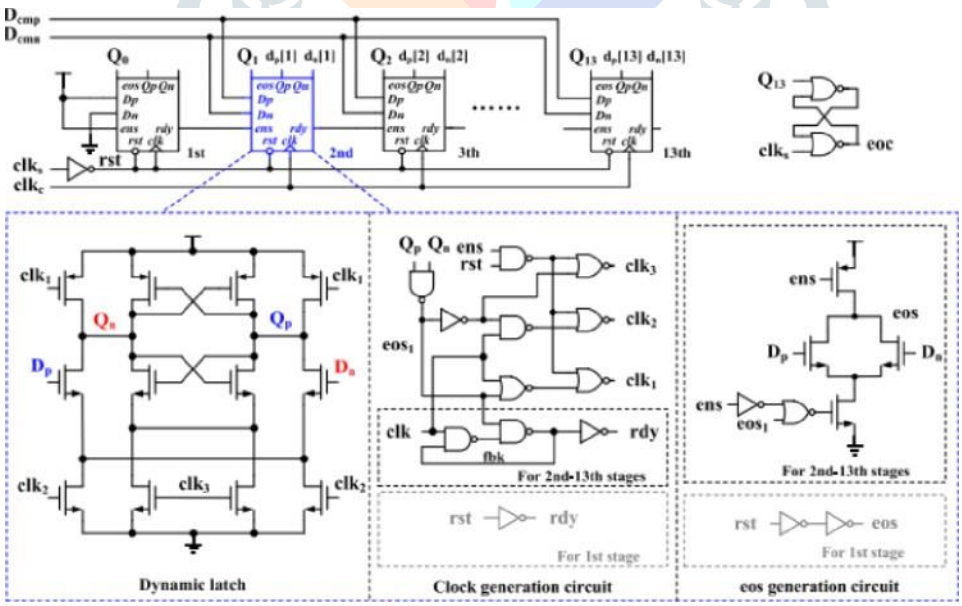

Fig5: SAR cell

Measurement results:

The prototype was fabricated in a 32-nm CMOS technology. The proposed SAR ADC has power consumption of 1.2mw, To reduce the noise in the digital circuitry, the comparator is placed close to DAC and SAR logic is placed away from DAC. In this paper, the logic control circuit has been optimized for power consumption and speed. The measurement results of the prototype are presented in the following.

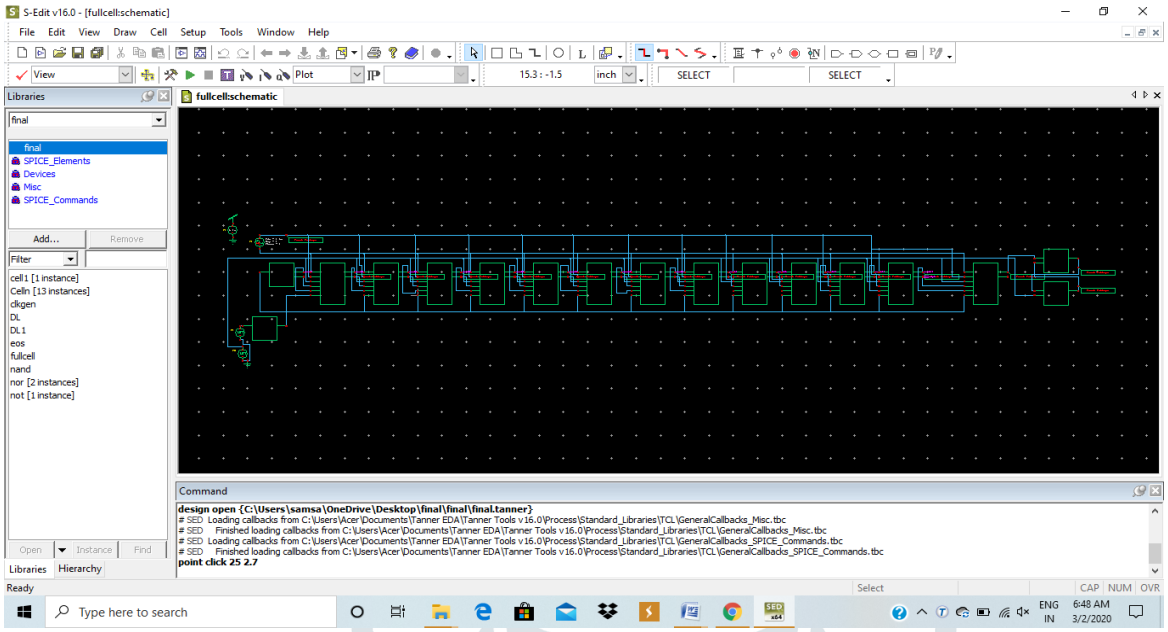

Fig6: Schematic view of proposed system

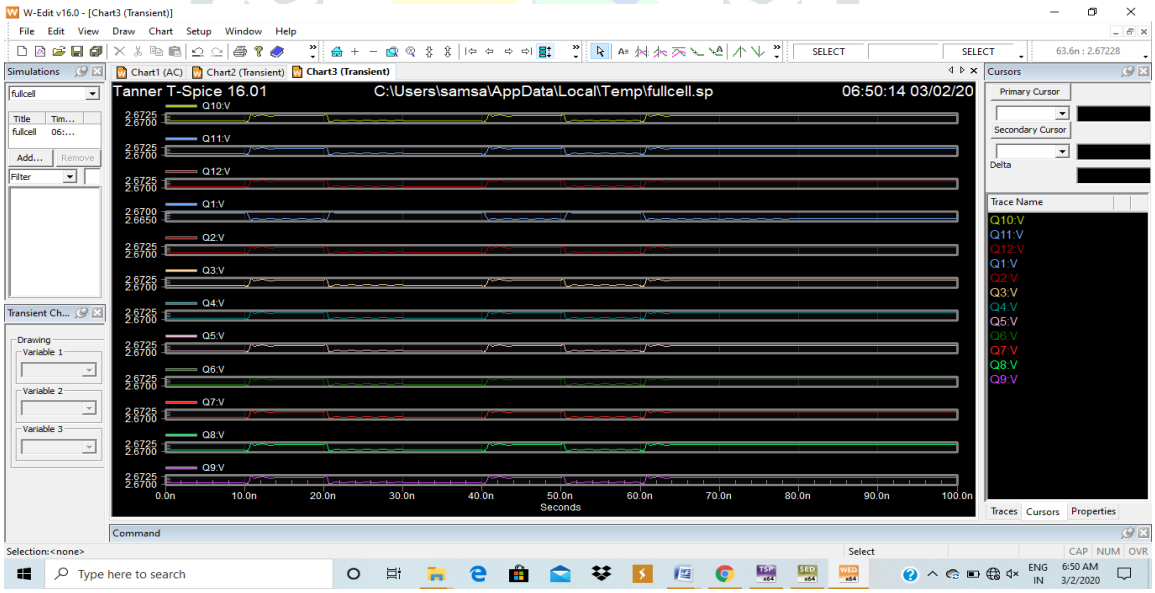

Fig7: Proposed method resultant waveforms

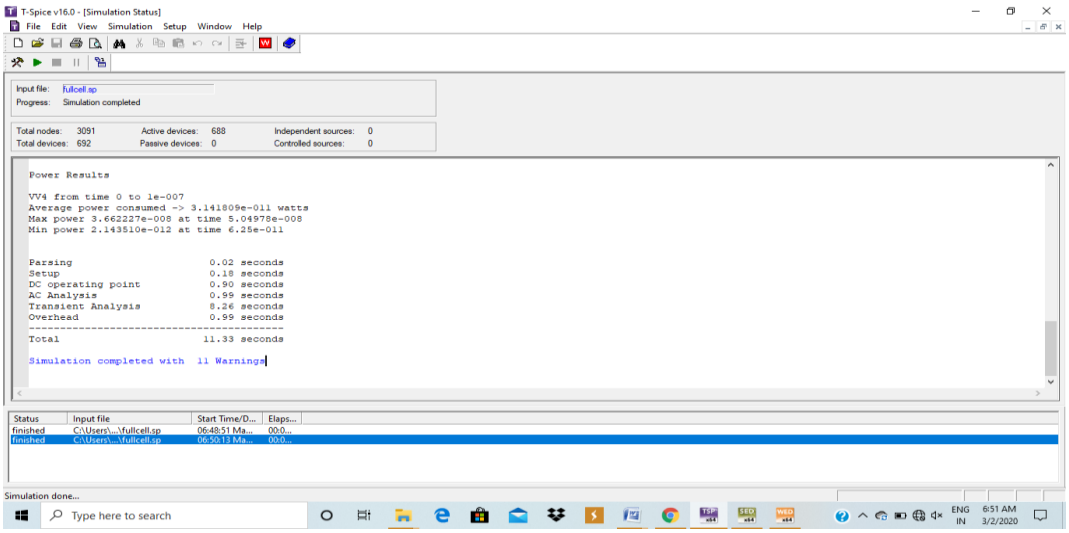

Fig8: Power report

Conclusion:

In this paper, a 12-bit SAR ADC has been presented. The small unit capacitor of DAC allows for extremely high hardware utilization and yielding a wide band input network while reducing DAC settling time and power consumption. In the comparator, the proposed non- linear capacitor correction method and the latch output glitch removal method are used, which help to improve the accuracy and speed of comparator at a low-power supply. In addition, the proposed high-speed SAR logic reduced the SAR ADC's power consumption to 1.2mW.

References:

[I] C.-C. Liu, M.-C. Huang, and Y.-H. Tu, "A 12 bit 100 MS/s SARassistetl digital-slope ADC," IEEE J. Solid- State Circuits, v‹il. 5I , no. 12, pp. 2941—2950, Aug. 20l6.

[2] L. Y‹›ng and M. P. Flynn, "A I iuW 71.5 dB SNDR 50 MS/S 13b fully diiYerential ring-amplifier-based SAR- assisted pipeline ADC," in IEEE Solid-State Circuits Cont. (ISSCC) Dig. Tech. Papers, Feb. 2015, pp. I—3.

[3] Y. Zhu ct a1., "A 10-bit lOO-M8/s reference-free SAR ADC in 9€1 nm CMOS," IEEE J, Solid- Stare Circuits, vol. 45, no. 6, pp. 1111—1121, Jun. 2010.

[41 on, B. Xu, and C. Yun, "A 12 bit 160 MS/8 two-step SAR ADC with background bit-weight calibraaon using a time-domain proximity detector,"' IEEE J. Solid-State Circuits, vol. 50, no. 4, pp. 920—931, Apr. 2015.

f5l H. Huang, H. Xu, B. Elie8, and Y. Chin, "A non-inter1eaved 12-b 330-MS/s pipelined-SAR ADC with PVT- stabilized dynamic amplifier achieving sub-1-dB SNDR variation," mm J. Solid-State Circuits, vol. 52, no. 12, pp. 3235—3247, DTc. 2017.

[61E. Janasen ct a1., "An 11 b 3.6 GS/a time-interleaved SAR ADC in 65 rim CMOS," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Pcb. 2013, pp. 464-4€;d.

[7] X. Tang, L. Chen, J. Song, and N. Sun, "A 10-b 750 qW 200 MS/8 fully dynamic 8ingle-channel SAR ADC in 40 rim CMOS," in Proc. 42nd Eur. Solid-State Circuits Conf. IESSCIRC), Sep. 2Hl6, pp. 413—416.

[8] D. V. Stepanovic, "Calibration techniques for time-interleaved SAR A/D converters," Ph.D. dilution, Dept. Rug. Rtect. Rug., Univ. California, Berkeley, Berkeley, CA, USA, 2Dl2.

I I A. Shikata, R. Sekimoto, T. Kuroda, and H, lahikuro, "A 0,s V 1.1 MS/sec 6.3 O/conver8ion-step SAR-ADC with tri-level comparator in 40 rim CMOS,"' IEEE J. Solid-State Circuits, vol. 47, no. 4, pp. 1022-1030, Apr. 2DI2.

[10] F. Kuttner, "A IN V 10 b 20 MSample/8 non-binany 8ucce88ive approximation ADC in 0.13 pm CMOS,"' in IRRR Solid-State Circuits Conf. (ISSCC) Dig. Tech. Paprrs, Pcb. 2002, pp. 136—137.

[Ill C.-C. Liu, S.-I. Chang, G.-Y. Huang, and Y.-Z. Lin, "A 10-bit 50-MS/s SAR ADC with a monotonie capacitor sitching procedure," IEEE J. Solid-State Circuits, vol. 45, no. 4, pp. 731-740, Apr. 2Hl0.

[12] H. K. Hong et al,, "A deci8ion-error-tolerant 45 rim CMOS 7 b I GS/8 nonbinaiy 2 b/cycle SAR ADC," mEE *1*. Solid-State Circuits, vol. 50, no. 2, pp. 543—555, Peb. 2015.

[l3] E. Yaqubi and S. H. Zahiri, ' timum de8ign of a double-tail latch comparator on power, speed, offmt and 8ize," Analog Integr. Circuit8 Signal Proceee., vol. 90, no. 2, pp. 309—319, Peb. 2016.

[14] W.-Y. Pang, C.-S. Wang, Y.-K. Chang, N.-K. Chou, and C.-K. Wang, "A 10-bit 500-KS/s low power SAR ADC with splitting comparator for bio-medical applicaaon8," in Proc. IEEE A8ian Solid-State Circuits Conf. (A- SSCC), Nov. 2009, 149-15.