DESIGN OF 32 BIT ASYNCHRONOUS RISC-V PROCESSOR USING VERILOG

G.Rajesh Babu, Asst.Proff. ,ECE Department, Usha Rama College Of Engineering and Technology , Telaprolu
M.Bhanu Prakash ,B.Tech, ECE Department, Usha Rama College Of Engineering and Technology , Telaprolu
M.Vijaya Kumari, B.Tech, ECE Department,Usha Rama College Of Engineering and Technology , Telaprolu
Ch.V.D.Ashok Kumar, B.Tech, ECE Department,Usha Rama College Of Engineering and Technology,Telaprolu
G.Sai, B.Tech, ECE Department,Usha Rama College Of Engineering and Technology , Telaprolu.

Abstract – The main Aim of the Project is to design of 5 stage pipeline 32 bit asynchronous RISC-V CPU and its implementation. It performs operations,like division, subtraction, and addition.The ST control signal can be used as a centralized generator of activation signals is based on the micropipeline.The asynchronous processors have a number of benefits, mainly in System on chip it reduces the cross talk between the mixed circuits, ease of integrating multi-rate circuits, component reuse and low power consumption. Implementation of such kind of asynchronous RISC-V processor by using Verilog on Xilinx ISE Design Suite tool where it is the potential of handling R Type, I-Type and Jump instructions Along with it uses separate memory for both data and instruction. The performance parameters were obtained through simulation. The estimated power, and delay were low compared to synchronous CPU were observed by the simulation results of the design.

***Key Words*:** RISC-V(Reduced Instruction Set), Harvard Architecture,ALU(Arithmetic and Logical Unit), Verilog, Xilinx , Asynchronous.

1. Introduction:

Most Current design is based upon a Synchronous approach. However, Nowadays there has been growing interest in asynchronous design due to low power consumption and Faster execution. In Asynchronous Design circuits, there is no clock signal and also the circuit state will changes as input changes. Asynchronous circuit has no need to wait for clock to begin its operation, these are faster than the synchronous circuits. Asynchronous circuits typically communicate and synchronizing using handshake signals. The feature of the RISC-V processor is the speed up the execution.

The 32 bit RISC-V processor comprises of load and store architecture. It means having two instructions for accessing memory LOAD instruction is to load the data from the memory and STORE instruction is used to write the data in to the memory and also uses the Hardwired architecture to increase the performance of the processor.

2. Related Work

In RISC , Harvard architecture is used that means it uses separate memory for both data and program. Asynchronous design increases the performance of the processor by reducing the waiting time at clock edges . The Operations are start its operation after immediate completion of previous operation instead of wait for the positive edge of the clock edge this can be achieved by using micropipeline structure. Asynchronous design reduces the power consumption and also reduce the heat dissipation it leads to lengthen the life of the battery. In previous work VHDL language is used to design 32 bit asynchronous RISC processor and in this work Verilog language is used to implement 32 bit Asynchronous processor due to more compatible to hardware modelling and also compact.

3. Architecture of 32 bit RISC-V Processor

3.1. Microprocessor Architecture

The 32 Bit Asynchronous RISC-V processor Comprises of Arithmetic unit(ALU), Booth's Multiplier, Control Unit, Register Bank, Memory and Data path. The Architecture divided into five stages. The pipeline stages are Instruction fetch(IF), Instruction decode(ID), Instruction Execution(IE), Memory Access(MA), Write back(WB).

The Design consists of three types of memories are Data memory, Instruction memory and register memory.In Instruction fetch stage, the 32 bit Instruction is being loaded into Instruction register by using address in the program counter(PC). After the fetch cycle the PC will increment by four addresses because of each register stores only 8 bit as it requires 4 registers to store 32 bit instruction.

In Instruction Decode stage, the 32 bit Instruction is divided. Depends Upon the 6 bit opcode it decodes from instruction. The Opcode is sent to the decoder then appropriate control signals are generated.

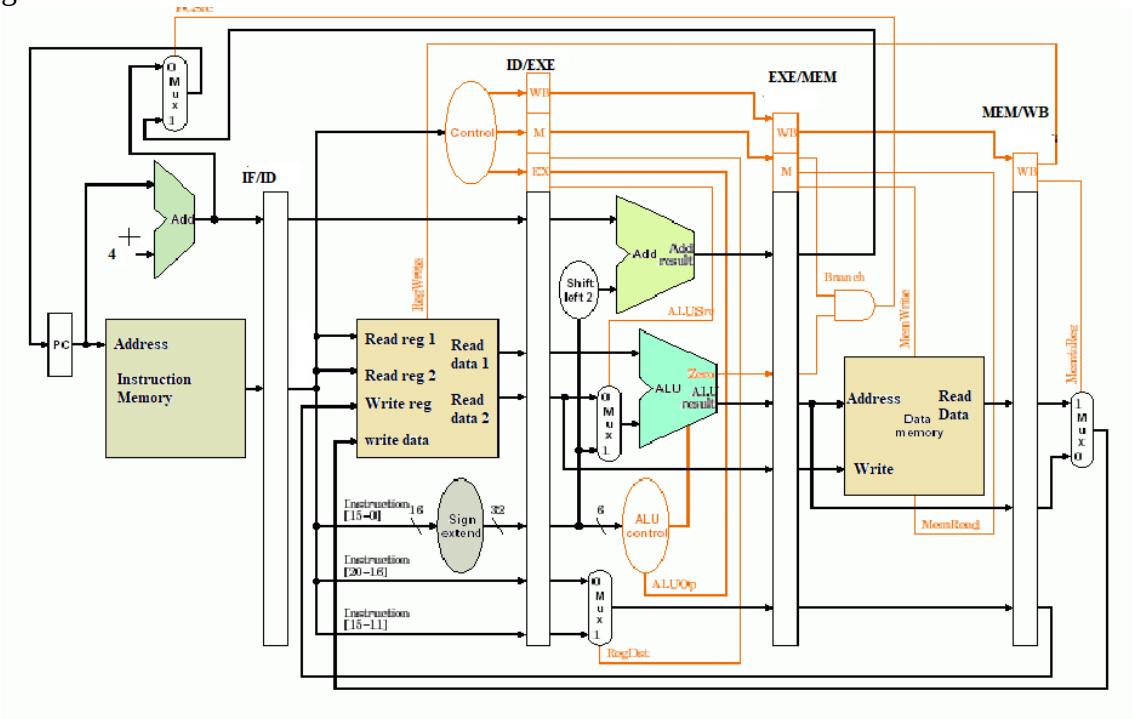

Fig1: 32 bit Asynchronous RISC-V processor

In Execution stage, the ALU unit performs the operations as per the decoded information. In Memory access (MA) the load and store instructions access the memory I.e read and write operations on memory

In Write Back stage, the result from ALU/Memory system write back to register file.

Function	Opcode
Addition	00100
Subtraction	10100
AND	11100
XOR	11101
OR	11110
NOT	11111
Division	01111

Swap	01101

Table1:Opcode Functionality

3.2 Instruction format

The Instructions are categorized into 3 types .They are

1.Register (R) Format: The opcode consists of MSB5 bits,the Rs consists of 6 bits, Rt and Rd consists 5 bits each. These Instructions are mostly used for Arithmetic and logical(ALU) operations.

2.Immediate(I) type: The opcode consists of MSB 6 bits ,Rs and Rt having 5 bits each and 16 bit immediate address value. These instructions are for data transfer, immediate and conditional branch instructions.

3.Jump(J) type: The opcode consists of MSB 6 bits and 26 bit word address. These instructions are used for unconditional branch instructions.

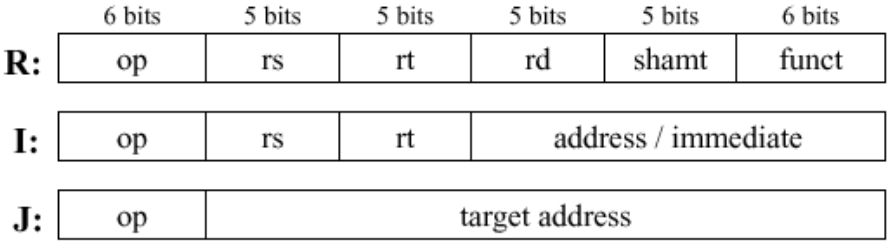

Fig2: Instruction format

OP-Basic operation of the instruction.

rs- First source operand register.

rt-Second source operand register.

rd- Destination register.

Shamt- Shift amount.

Funct- Selects the specific variants of the opcode.

4.Comparison between Synchronous and Asynchronous RISC-V Processor

In Asynchronous design the required stages only operate there by power consumption is reduced and the total delay were reduced due to its micropipeline structure. The Total power is estimated by using the X power Analyzer tool.

S.N	Parameter	synchronous	ASynchronous
1	Total Delay	18.243ns	12.305ns
2	Total Power consumption	0.829 w	0.109 w

Table2:Comparison between synchronous and asynchronous RISC-V Processor

5. PERFORMANCE ANALYSIS:

5.1 RTL Schematic Output of 32 bit Asynchronous RISC-V processor

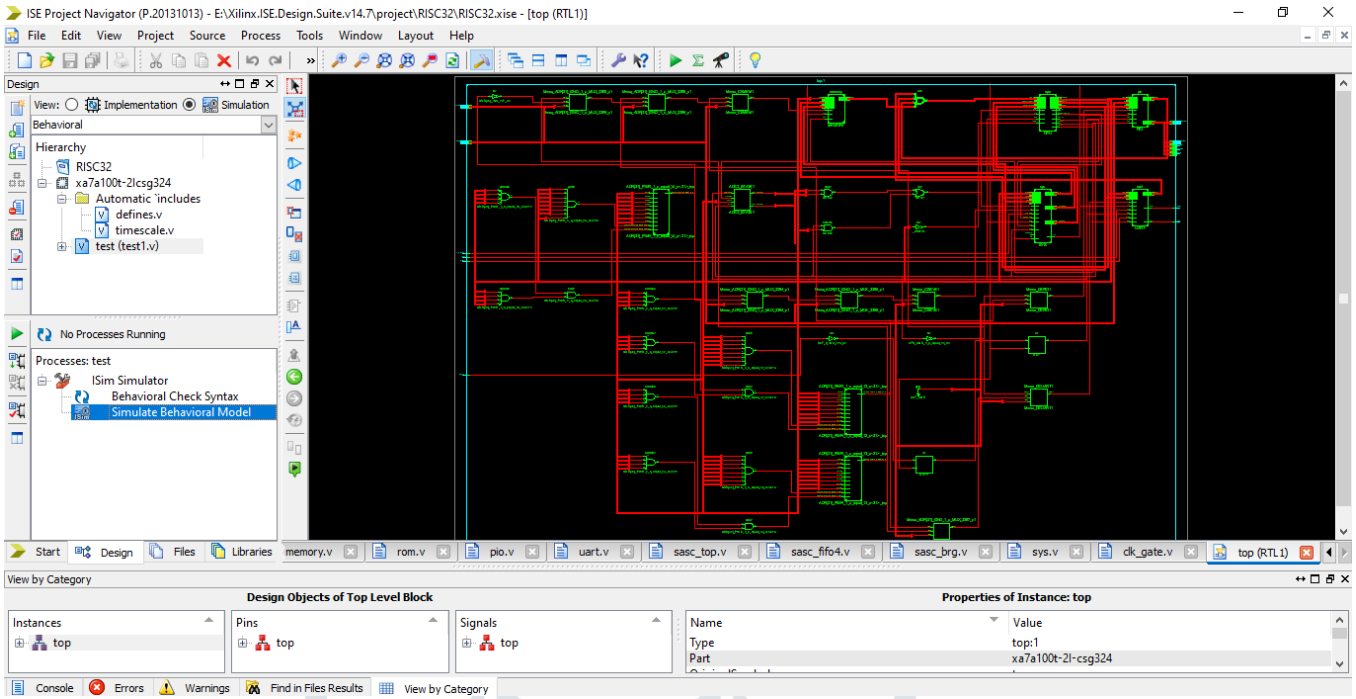

Fig3: RTL Schematic output

5.2 Simulation Result

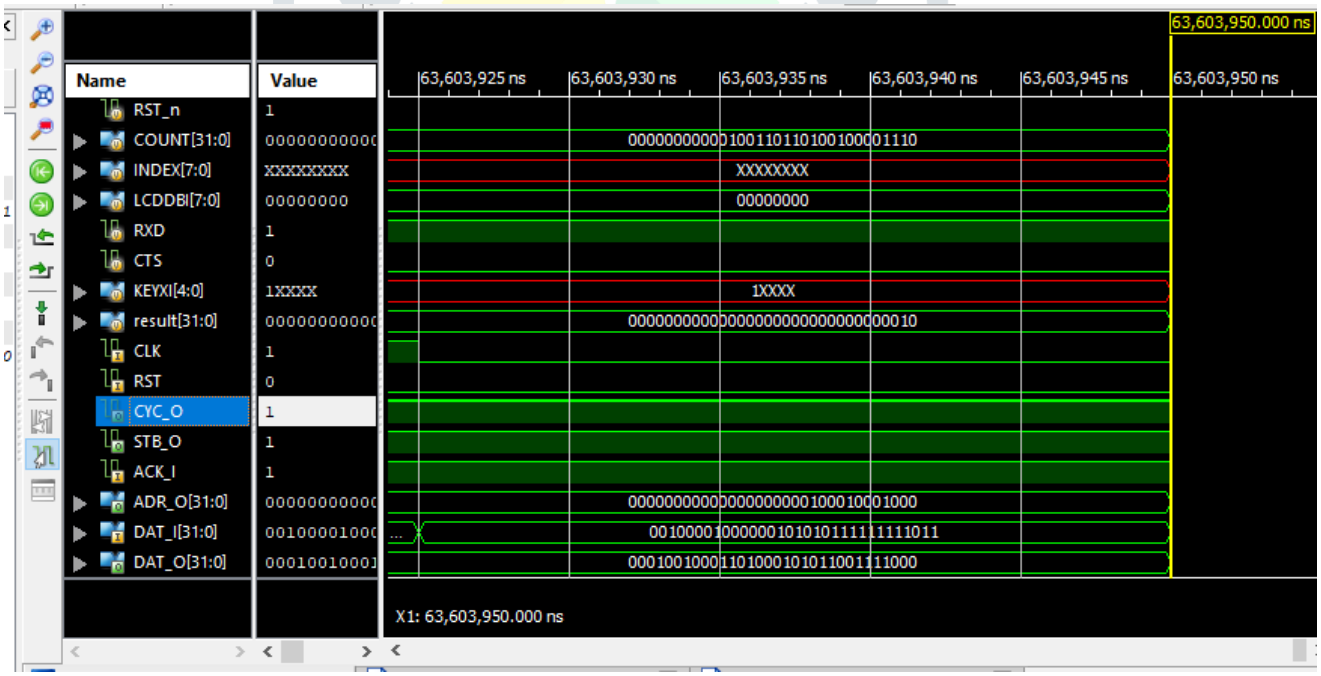

Fig4: Simulation Result of a processor

4.3 Power Analysis

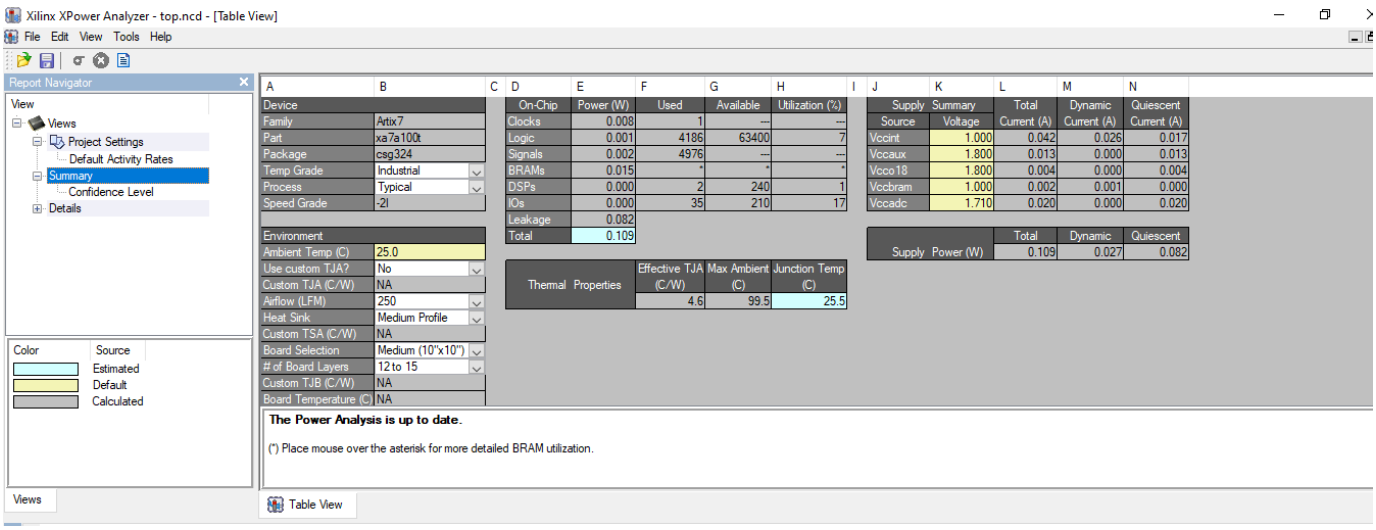

Fig5: Power estimation

7. Future Enhancement:

The above design can be further enhanced to 64 bit wide RISC-V processor, optimization of area and also the logic. In future this can be optimized by upcoming techniques.

6. Conclusion:

The design of 5 stage 32 bit Asynchronous RISC-V processor has been achieved using verilog HDL, generate the RTL Schematic and simulated with ISIM .The result of the power estimation in asynchronous CPU design is analyzed by using X Power Analyzer.

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