DESIGN OF 64 BIT VEDIC MULTIPLIER USING CARRY LOOK AHEAD ADDER

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Abstract: This paper proposed the design of 64 bit vedic multiplier using vedic mathematics based on 16 sutras. The main aim of VLSI is to optimize any type of digital architecture. Multiplication is an important fundamental function in arithmetic logic operation. Computational performance of DSP system is limited by its multiplication performance, multiplication dominates the execution time of most DSP algorithms. our work is to develop the 64-bit vedic multiplier using carry look ahead adder technique.

Index Terms*:* Carry look ahead adder , Vedic multiplier

Introduction:

The speed of a processor, determines its performance. High speed processing is an essential requirement for all the systems. Multiplication is a significant operation in Digital signal processors and ALU, and thus the demand for high speed multiplication is continuously increasing in modern VLSI design.

Multipliers like booth multiplier, Modified Booth Multiplier, and array multipliers were considered for high speed multiplication, but these multipliers involve large number of intermediate steps, which reduces their speed with increase in the number of bits. For high speed multiplication as well as to increase the performance of multiplier vedic multiplier is proposed.

				A3	A2	A1	A0	Inputs
			x	B3	B2	B1	B0	
			C	B0 x A3	B0 x A2	B0 x A1	B0 x A0	
		+	B1 x A3	B1 x A2	B1 x A1	B1 x A0		
		C	sum	sum	sum	sum		
	+	B2 x A3	B2 x A2	B2 x A1	B2 x A0			Internal Signals
	C	sum	sum	sum	sum			
+	B3 x A3	B3 x A2	B3 x A1	B3 x A0				
C	sum	sum	sum	sum				
Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Outputs

Fig1: Array multiplication

In the existing system of array multiplier using carry select adder, the partial products are generated simultaneously but power consumption is more .It is a fast multiplier but complexity level is high.Carry propagation time is more compared to vedic multiplier.

Proposed system:

The proposed system is used to reduce the carry propagation time and to optimize the hardware complexity level for 64 bit Vedic multiplier operation. The proposed system is to implement vertical and cross-wise equation based logical 64 bit multiplier operation.

Vedic Mathematics Swami Bharati Krishna Tirtha, called a set of 16 Sutras (aphorisms) and 13 Sub-Sutras (Corollaries) from the Atharva Veda. He developed method and techniques for amplifying the principles contained in the aphorisms and their corollaries, and called it Vedic Mathematics. In Vedic Mathematics partial products are generated in parallel, which increases the speed of operation. In this paper we are proposing a design for accumulation of these intermediate products, with minimal delay Multiplication if an operation much needed in Digital Signal Processing for various applications. This paper puts forward a high speed Vedic multiplier which is efficient in terms of speed, making use of Urdhva Tiryakbhyam, a sutra from Vedic Math for multiplication.

Vedic Multiplier:

The high speed processor requires high speed multipliers and the Vedic Multiplication technique is very much suitable for this purpose Multipliers are extensively used in Microprocessors, DSP and communication applications. For higher order multiplications, a huge number of adders are to be used to perform the partial product addition. The need of high speed multiplier is increasing as the need of high speed processors are increasing. Higher throughput arithmetic operation.

Multiplication algorithm:

The proposed system is to modify the PPG unit addition process and to optimize the carry selection processing time. The carry selection time is to be reduced. A high speed processor depends greatly on the multiplier as it is one of the key hardware blocks in most digital signal processing systems as well as in general processors. This paper presents a high speed 8x8 bit Vedic multiplier architecture which is quite different from the Conventional method of multiplication like add and shift.

Vedic mathematics, which simplifies arithmetic and algebraic operations, has increasingly found acceptance the world over. Experts suggest that it could be a handy tool for those who need to solve mathematical problems faster by the day. It is an ancient technique, which simplifies multiplication, divisibility, complex numbers, squaring, cubing, square roots and cube roots. Even recurring decimals and auxiliary fractions can be handled by Vedic mathematics. The multiplier will require the same amount of time to calculate the product and hence is independent of the clock frequency. By adapting the Vedic multiplier, structure.

Due to its regular structure, it can be easily layout in microprocessors and designers can easily circumvent this power of multiplier. It can easily be increased by increasing the input and output data bus width since it has a quite a regular problems to avoid catastrophic device failures. The net advantage is that it reduces the need of microprocessors to operate at increasingly high clock frequency.

Multiplication Algorithm for Urdhva Tiryakbhyam Sutra:

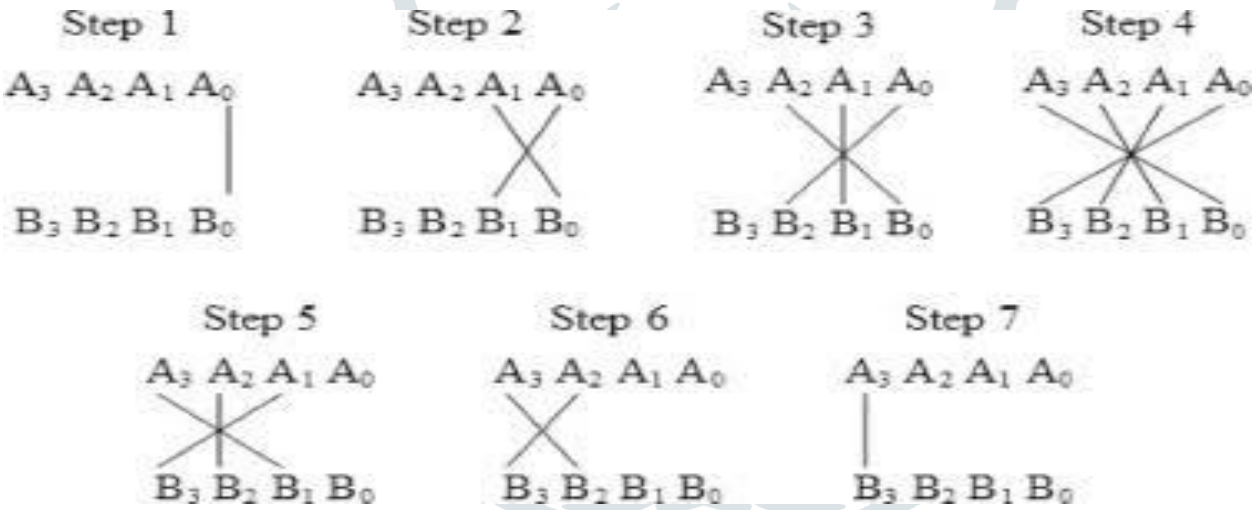


Fig2: Algorithm of UT sutra

Carry look ahead adder:

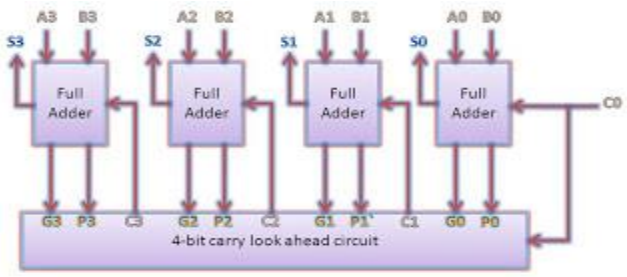


Fig3: 4bit carry look ahead adder

A Carry Look Ahead Adder or Fast adder is a type of adder used in digital logic.A carry look ahead adder improves speed by reducing the amount of time required to determine carry bits. The carry Look Ahead Adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits of the adder.\

64 Bit Multiplier Architecture:

Our work is to modify the 64-bit multiplier architecture using Vedic mathematics technique. This technique is to implement the vertical and cross-wise equation based process. First we design a 4-bit multiplication operation and to develop the 8-bit multiplication process using 4bit multiplication result. Finally we design a 64 bit multiplier architecture using a 4-bit, 8-bit ,16bit and 32bit multiplication process. This structure is to reduce the complexity and time level.

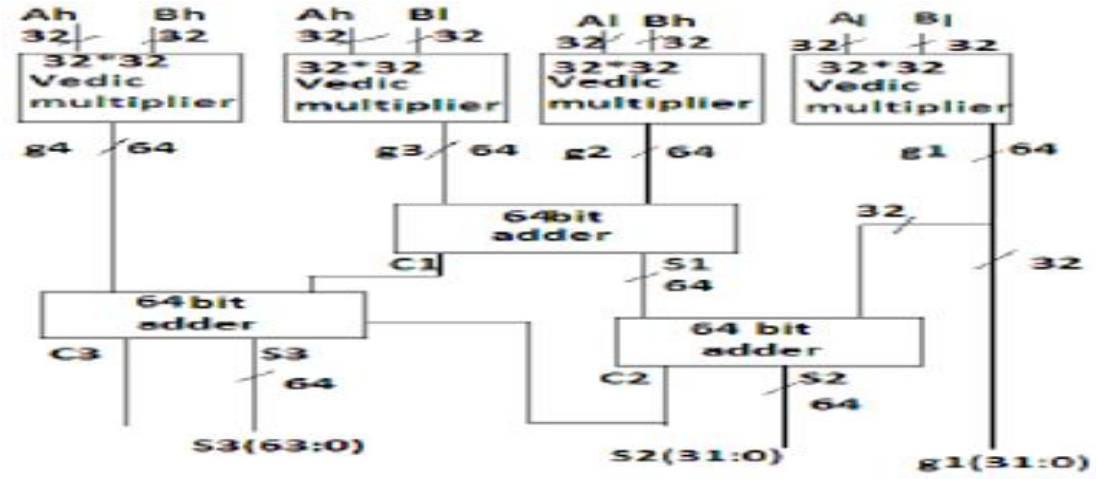


Fig4: Vedic Multiplier Block Diagram

Performance Analysis:

The multiplier architecture is mainly used to the ALU UNIT. Because the architecture optimization process is only possible in the VLSI domain. The Verilog HDL language is mainly used to improve the accuracy compare to another type of process. The XILINX 14.5 software is used in our project. Our process was developed in Verilog HDL language using XILINX software. It is an ancient technique, which simplifies multiplication, divisibility, complex numbers, squaring, cubing, square roots and cube roots. Even recurring decimals and auxiliary fractions can be handled by Vedic mathematics.

Result Analysis:

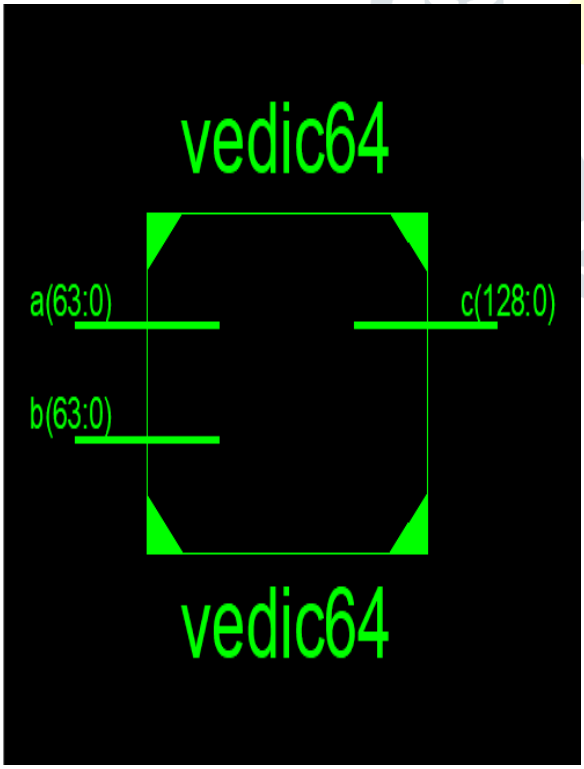


Fig5: Proposed method pin diagram

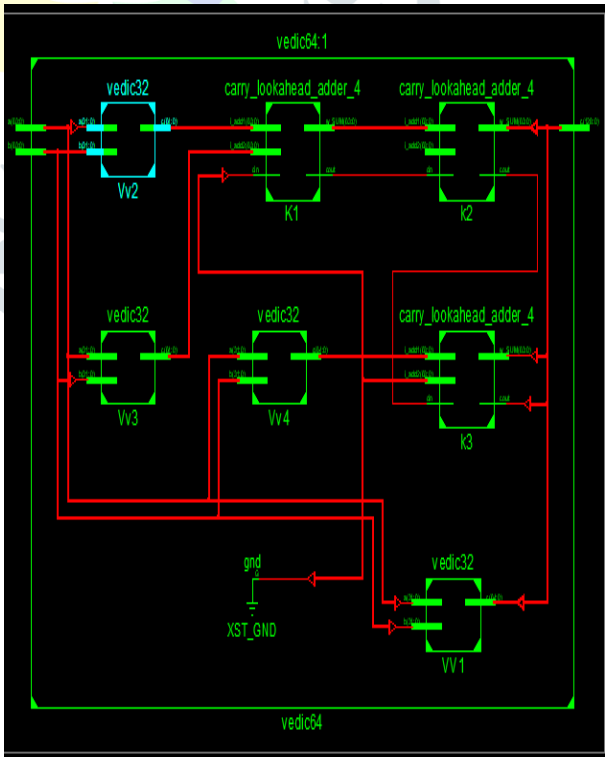


Fig6: Schematic view of proposed system

Resultant Waveforms:

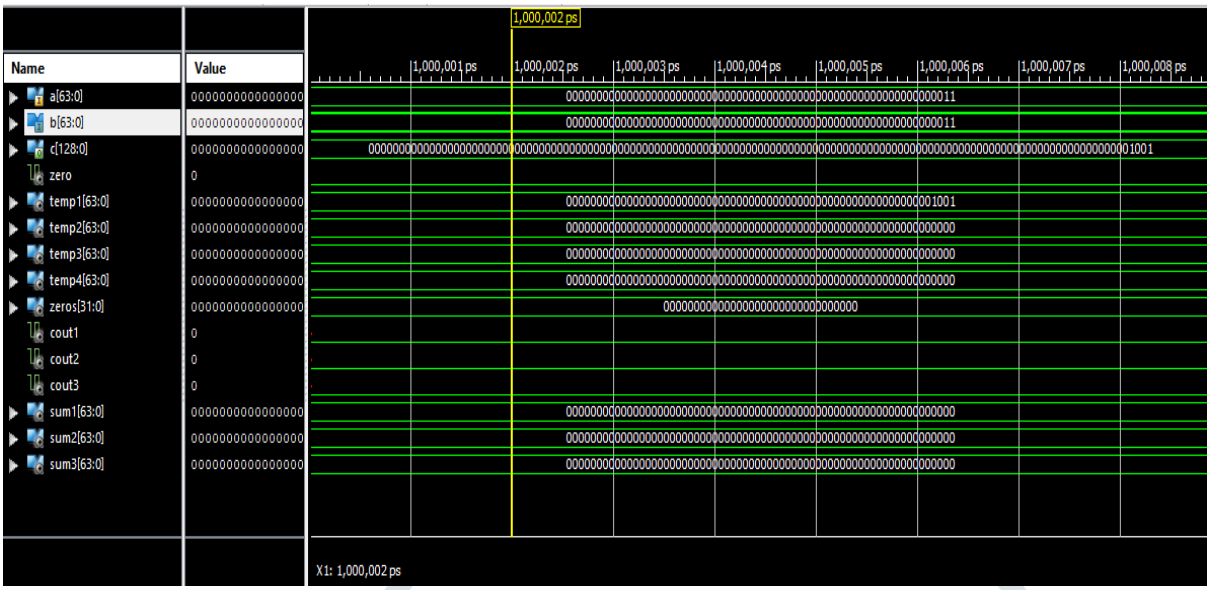
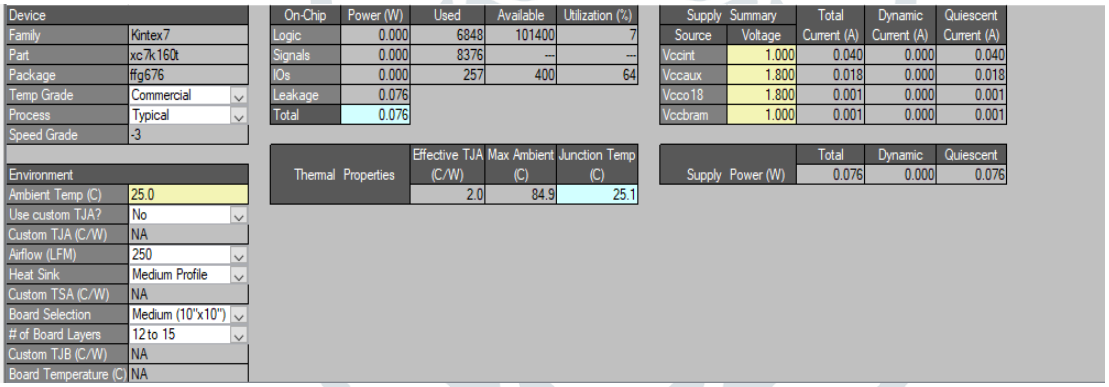


Fig7:Proposed method resultant waveforms

Power Analysis:



Device	
Family	Kintex7
Part	xc7k160t
Package	ffg676
Temp Grade	Commercial
Process	Typical
Speed Grade	-3

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile
Custom TSA (C/W)	NA
Board Selection	Medium (10"x10")
# of Board Layers	12 to 15
Custom TJB (C/W)	NA
Board Temperature (C)	NA

On-Chip	Power (W)	Used	Available	Utilization (%)
Logic	0.000	6848	101400	7
Signals	0.000	8376	---	---
IOs	0.000	257	400	64
Leakage	0.076			
Total	0.076			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	2.0	84.9	25.1

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.000	0.040	0.000	0.040
Vccaux	1.800	0.018	0.000	0.018
Vcco18	1.800	0.001	0.000	0.001
Vccbram	1.000	0.001	0.000	0.001

Supply Power (W)	Total	Dynamic	Quiescent
	0.076	0.000	0.076

Fig8:Power Report

Delay Report:

```
    ----------------------------------------
    Total                          58.841ns (5.203ns logic, 53.638ns route)
                                            (8.8% logic, 91.2% route)

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Cross Clock Domains Report:
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Total REAL time to Xst completion: 24.00 secs
Total CPU time to Xst completion: 24.79 secs

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Total memory usage is 4636708 kilobytes
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Fig9:Delay Report

Conclusion:

This paper presents a highly efficient method of multiplication– "Urdhva Tiryakbhyam Sutra" based on Vedic mathematics. It gives us method for modular multiplier design and clearly indicates the computational advantages offered by Vedic methods. The computational path delay for proposed new Vedic multiplier is found to be less as compared to other multiplier. Hence our motivation to reduce delay is finely fulfilled. Therefore, we observed that the new Vedic multiplier is much more efficient than Array and conventional multiplier in terms of execution time (speed). It is used for Digital Signal Processing application. The Proposed Multiplier design can be used in applications with minimal loss in output quality while saving significant power and area.

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