Optimised Division Circuit Using Reversible Logic Gates For Quantum Computers

M.Bhanusri,Dr.Ch.Santhi Rani,A.Sneha Latha,P.Ramyasri ,

Department of ECE,Usharama College of Engineering and Technology.

Abstract:

Reversible logic is introduced to overcome the problem of heat dissipation in conventional systems i.e using AND and OR gates.Quantum computing is one of the major and emerging applications of reversible logic.In conventional computers there are two states either '1' or '0' but quantum computing which is devolping based on the quantum theory where '0' and '1'are used simultaneously . Reversible logic gates are designed using reversible logic.Reversible logic gates are the gates that have same number of inputs and outputs and have one-to-one mapping between input and output lines.Based on this reversible logic we have designed a reversible division circuit since division is one of the main building block in ALU and has crucial role in digital signal processing.The proposed design have reduced the hardware complexity of 24ß+48δ when compared to the existing designs in reversible logic.

Keywords:Reversible logic,Quantum computing,one-to-one mapping,ALU,reversible division, hardware complexity.

Introduction

Energy dissipation is one of the essential factor considered in designing circuits in VLSI.In irreversible circuits for every bit of information lost dissipates KT*ln2 of energy.So inorder to avoid this Bennett in 1973 proposed that computation should be done in reversible manner.Reversible logic circuits are also called lossless circuits since they have no information loss or energy loss.A gate is said to be reversible logic gate if it has equal number of input and output lines and if it has unique mapping between input and output vectors.Because of this unique mapping between input and output lines the inputs are recovered from output.Since reversible logic circuits do not lose data they have theoretically zero heat dissipation.Division process is one of the important module in ALU and has wide applications in digital signal processing.This paper focuses in designing a division circuit using reversible logic gates which gives less hardware complexity compared to the previous designs.The parameters that are considered while designing the circuits using reversible logic gates are hardware complexity,garbage outputs,constant inputs,quantum cost.

Hardware complexity:

Hardware complexity refers to the number of logical calculations[6] i.e AND,EX-OR,NOT gates used in circuit.

α = Number of EX-OR gates

ß = Number of AND gates

δ = Number of NOT gates

Garbage outputs:

The unutilized outputs[2] of the gate are considered as garbage outputs.

Constant inputs:

Inputs that are connected to logical '0' or '1' inorder to get the logical function[14] are termed as constant inputs.

Quantum cost:

Quantum cost is defined as number of elementary gates[1] used to realize the circuit .

Related Work:

In the process of designing the circuits one should select the gates that have less hardware complexity,garbage outputs,constant inputs,quantum cost.A.Bolhassani and in 2016[6] proposed a division cicuit based on reversible logic has 89 constant inputs,quantum cost[1] of 454,103 garbage outputs and has the hardware complexity of 65α+74 β+52δ.And this circuit follows the restoring division process.In 2009,Nayeem[15] proposed a division circuit which follows the non restoring algorithm for division process has the total constant inputs of 91,quantum cost of 538,106 garbage outputs[2] and hardware complexity of 59α+67 β+33δ.Faraz Dasatan proposed a division circuit using reversible logic gates in 2012 [7]which follows non restoring algorithm has 161 constant inputs,846 quantum cost,181 garbage outputs and hardware complexity of 91α+98 β+43δ.

In this paper we have choosen non restoring algorithm for division process since test of subtraction is required in restoring algorithm[12].In non restoring algorithm signed bit chooses whether to perform addition or subtraction and test for subtraction is not required.This work mainly focused in optimization the circuit by choosing the gates that have less hardware complexity.

Division process flow chart:

The division circuit proposed in this work follows the algorithm of non restoring division.The flow chart of this division process is shown in the fig1 below.
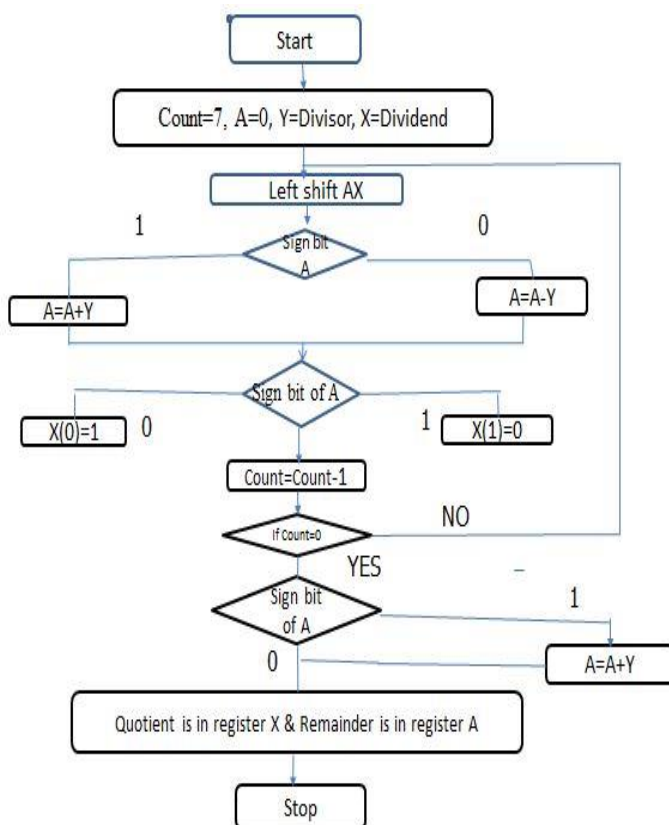

Fig1:Division process flowchart

Step1:Intialize the registers count=7,A=0,Y=divisor,X=dividend.
Step2:Shift the AX registers to the left by one count.
Step3:Check the sign bit of A.If it is 1 performs addition else if it is 0 performs subtraction.
Step4:Again check the sign bit of A if it is 1 X(0)=0 else X(0)=1.
Step5:Decrement the count value.
Step6:If is not equal to 0 repeat the process from Step2 else check the sign bit if it is 1 perform subtraction else go to Step7.
Step7:X register contains quotient and A register contains remainder.
Step8:Stop.

Division Circuit Building Blocks

The following are the reversible components required to implement the division circuit:

- Multiplexer using reversible logic gates
- Adder/Subtractor using reversible logic gates
- PIPO left shift register using reversible logic gates
- Control circuit using reversible logic gates

Multiplexer designed with RI reversible logic gate:

The Fig2 shows the design of 8-bit reversible multiplexer.This multiplexer is designed using R-I gate.Where sel is the selection line,A and B are the two input lines of the multiplexer.The second output line is the output of multiplexer i.e op.If sel=0 the op=A else if sel=1 then op=B.
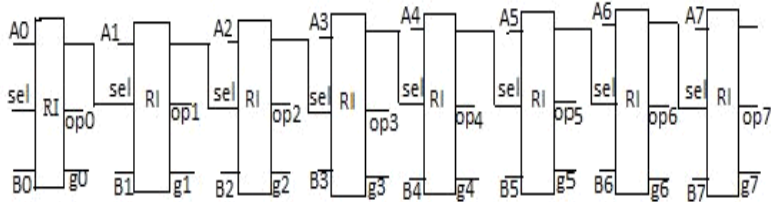
Fig2:8-bit multiplexer using RI gate

Adder/Subtractor using reversible logic gates:

This adder/subtractor block is designed using reversible logic gates HNG and TS-3.Reversible adder/subtractor block is shown in the Fig3.If control input is '1' then it performs addition else it performs subtraction.
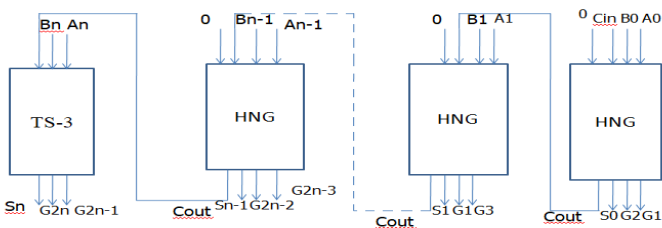

Fig3:n-bit adder/subtractor using reversible logic gates

PIPO left shift register using reversible logic gates:

The reversible register which is designed using BHC gates which acts as D-Latch is shown in Fig4.And using this register a left shift register using D-Latch is designed.
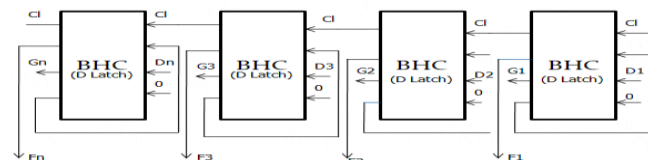

Fig4 :8-bit reversible register

Control circuit:

Control circuit includes comporator and counter circuits.Comparator is used to compare two inputs for greater than,less than and equal to conditions.And counter is used to count the clock pulses.Here mod8 counter is used which counts from 0 to 7 if the stored value is 0 or counts from 7 to 0 if the stored value is 7

Reversible division circuit:

By using these reversible components like multiplexer adder/subtractor,shift register,control circuit a reversible circuit that performs division operation is designed and shown below.To perform division operations dividend and divisor are given as inputs,quotient and remainder are obtained as outputs for the given inputs.
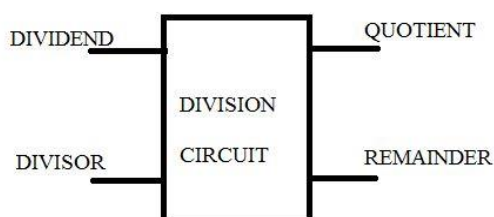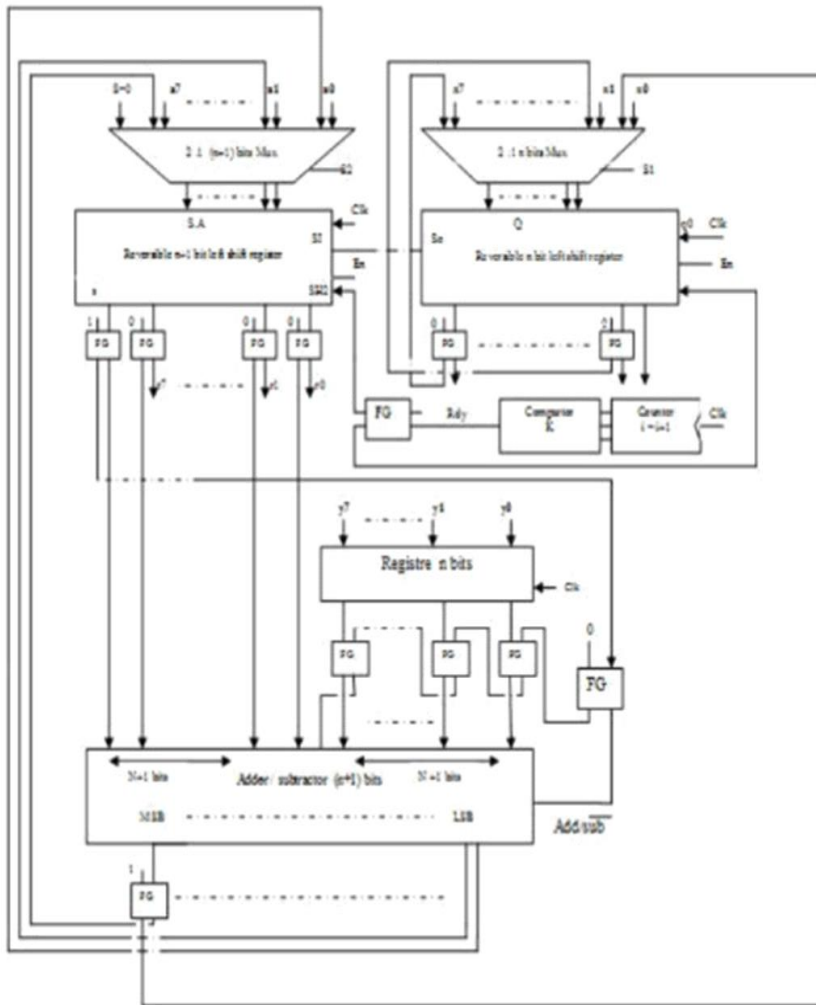

Fig5:Division process

Fig6:proposed division circuit using reversible logic gates

In the Fig6 X and Y represents dividend and divisor and 'A' stores 0 initially.The A and X registers are concantated and shifted to left by one count.After shifting the MSB bit of A is compared.If the MSB bit is '1' then it performs addition else performs subtraction of A and Y and its result is stored in A.Again the MSB bit of A is compared.If it is '1' then the LSB bit of X is stored as '0' else stored as '1'.And this process is continued until the count value in the counter equals to '0'.Finally the contents of A register is remainder and the contents of X register is quotient.

Comparison:
     The following Table1 compares the proposed design with the existing designs of division circuits using reversible logic.
Table1:Comparsion

Existing division circuits	Constant inputs	Quantum cost	Garbage outputs	Hardware complexity (n=1)	Hardware Complexity (n=8)
Our work	88	440	99	$53\alpha+59\beta+37\delta$	$424\alpha+472\beta+296\delta$
Gassoumi, 2018	88	440	99	$53\alpha+62\beta+43\delta$	$424\alpha+496\beta+344\delta$
Bolhassani, 2016	89	454	103	$65\alpha+74\beta+52\delta$	$520\alpha+592\beta+416\delta$
Faraz Dastan1, 2012	161	846	181	$91\alpha+98\beta+50\delta$	$728\alpha+784\beta+400\delta$

The proposed design reduces the hardware complexity when compared to the existing designs using reversible logic.This work reduced the hardare complexity of 24ß+48δ for a 8-bit division circuit.

Simulation Results:

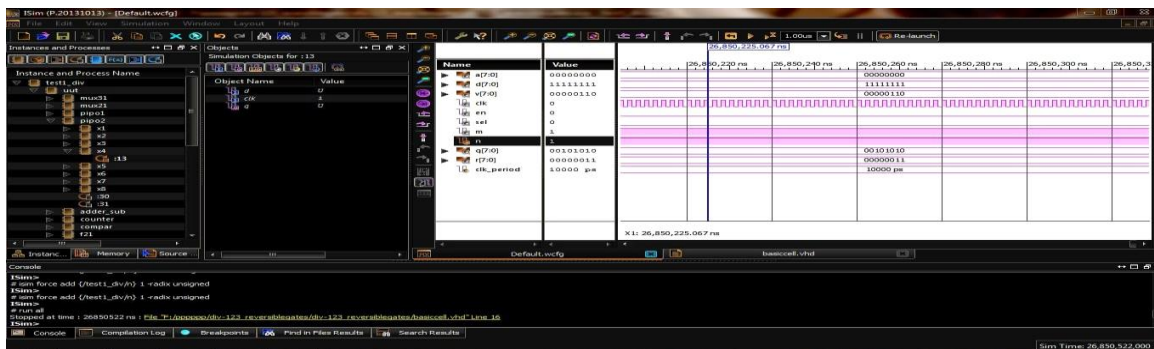The simulation results for 8-bit division circuit using reversible logic gates is shown in Fig7.

Fig7:Simulations of 8-bit division circuit

For division dividend and divisor are given as inputs and remainder and quotient are obtained as outputs.Here A register is loaded with 0 and 'd' and 'v' are dividend and divisor i.e inputs and 'q' and 'r' are outputs i.e outputs.In the above example we have taken the inputs dividend as 255 and divisor as 6 in decimal equivalents.And we obtain the outputs quotient and remainder as 42 and 3(decimal equivalent).

Conclusion:

This work proposed an optimized reversible division circuit using reversible logic gates.This optimized design have better performance in terms of hardware complexity compared to the previous reversible designs. Our proposed design have reduced the hardware complexity of 24ß+48δ when compared with the existing design with reversible logic.In future,research in the field of quantum computing is going to be increasing rapidly. As a result of it we can access quantum computers in real time where a set of calculations is performed at a time instaed of doing one after another.

References:

[1] Ismail Gassoumi,Lamjed Touil,Bouraoui Ouni, "Division Circuit Using Reversible Logic   Gates",IEEE,pp.60-65,June 2018.

[2] G.Srikanth,C.Venkata sudhakar,"Design and synthesis of combinational circuits using reversible logic",International Journal of Electronics,Electrical and Computational System,Volume 7,Issue 4,pp.527-533,April 2017.

[3] Lenin Gopal,Nikhil Raj,Alpha Agape Gopalai,Ashoutsh Kumar Singh,"Design Reversible multiplexer/Demultiplexer",IEEE,pp.416-420,November 2014.

[4] C.H.Bernet,"Logical reversibility of Computation",IBM Journal Of Research and Development,pp.525-532,1973.

[5] Md.Ashraful Haque,sadia rahman,"Sequential circuit using reversible logic gates", International Journal of Scientific & Engineering Research, Volume 6, Issue 4,pp.901-908 ,April-2015 .

[6] A.Bolhassani, M. Haghparast, "Optimised reversible divider circuit", J. Innovative Computing and Application, pp. 13-33, 2016.

[7] Faraz dastan1 and Majid Haghparast,"A novel nanometric reversible signed divider with overflow checking capability",Research Journal of Applied Sciences,Engineering and Technology,pp.535-543,2012.

[8] G.Srikanth,C.Venkata sudhakar,"Design and synthesis of combinational circuits using reversible logic",International Journal of Electronics,Electrical and Computational System,Volume 7,Issue 4,pp.527-533,April 2017.

[9] R.Landeur,"Irreversibility and heat generation in the computation process",IBM Journal of Research and Development,Vol 5,pp.183-191,1961.

[10] Onkar Nath Sabran,Shrikant Ahirwar,"An Extensive Review on Reversible logic in VLSI",International Journal of Scientific Progress and Research,Vol 01,2014.

[11] Sivaram babu V,P Ravi kumar,"Division circuit using reversible logic gates",IJCEACE,Vol 1,Issue 14,pp.74-84,2018.

[12] D krishnaveni,M.Geethapriya,"Reversible signed division for computing systems",International Journal of Electrical and Computer Engineering,Vol 11,pp.1265-1275,2017.

[13] D.Vinod kumar,Dr.Tata Jaganadha swamy,"VHDL Design and Implementation of CPU by reversible logic gates",IJASTEMS,vol 2,issue 12,pp.108-112,December 2016.

[14] Rohini H,Dr.Rajasekhar S,Dr.Priyatam Kumar,"Design of basic sequential circuits using reversible logic",IEEE,pp.2110-2115,2016.

[15] Noor Muhammed,Md.Adnan Hossain,Md.Mutasimul Haque,Lafifa Jamal,Hafiz M.Hasan"Novel reversible division hardware",IEEE,pp.1134-1138,2009.