DESIGN OF MULTIPLEXER AND JK FLIP FLOP USING ADVANCED REVERSIBLE LOGIC GATES FOR QUANTUM COMPUTERS

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Abstract:

Quantum computers are the present emergent technology which uses reversible logic gates for designing quantum circuits classical logic gates are for conventional digital circuits where as reversible logic gates are building blocks of quantum circuits. power consumption in digital circuits can be drastically reduced by using reversible logic. In conventional digital circuits, during logical operations some bits of information are lost due to significant amount of energy is dissipated. So, this loss of bits of information can be avoided by using reversible logic gates. Reversible logic gates used to maximize the speed and reduce the time delay. Reversible technology plays an important role in nano technology and less energy complementary metal oxide semiconductor (CMOS) technology. This paper presents some of the reversible logic gates, advanced reversible logic gates like PV, SAM, Multiplexer, JK flip flop. JK flip flop with simple reversible logic gates and advanced reversible logic gates is designed. The power, delay in JK flip flop with reversible logic gates is observed as 2.49Mw, 2.18nsec and the power, delay in JK flip flop with advanced reversible logic gates is observed as 2.019Mw, 1.59nsec .From these results it is observed that JK flip flop with advanced reversible logic gates consumes less power and faster than JK flip flop with simple reversible logic gates.

Keywords: Quantum computers, reversible logic, garbage outputs, Multiplexer, JK flip flop.

Introduction

In recent years, power dissipation is the dominant problem. Reversible logic has ability to reduce the power dissipation which is the main requirement in the low power VLSI circuits. It has some applications in low power CMOS , DNA computing, quantum computing, computer graphics, nano technology. Irreversible hardware computation results in information lost due to significant energy dissipation.so, the damage of bits of information lost ,and will deplete KT*ln joules of energy where k is the boltzmann's constant and k=1.38*10
-23 J/K, T is the absolute temperature in Kelvin.According to Moore's law states that number of transistors in a chip doubles every two years but chip size decreases. This cannot be reduced greatly which will lead to more power consumption. Present day computers are formed of digital logic circuits where one bit of information is lost for every computation. This is called irreversible logic . To overcome this problem Bennett proposed number of inputs and outputs makes equal which will dissipate less power as bits are preserved at the output. This is called Reversible logic.

Related work

In[1] author proposed a new 3*3 SAM reversible logic gate and they designed sequential circuits like SR flipflop,Master slave SR flipflop, JK flipflop ,Master JK flipflop and D flipflop with reversible logic gates and compare the parameters like quantum cost ,time delay of the circuit. In[2]Author proposed a PV logic gate and transistor implementation of 2:1 multiplexer along with they designed 4:1 multiplexer and 8:1 multiplexer. In
[3] they proposed R-1 and R-11 gates .R-1 can be used as a 1:2 demultiplexer and R-11 can be used as half adder. They stated that the logical functions such as XOR,AND,MUX,DE-MUX. In[4] author proposed a two universal reversible logic gates ANOX(And-or-xor)gate and NDI(Nand inverter). They also designed the half adder and full adder using proposed gates And they proved it is very useful to design large circuits with low complexity.
Our existing reference paper, authors have carried out the performance comparision of various reversible logic gates and they designed full adder/subtractor in two approaches and compare the two design approaches in terms of garbage outputs, power consumption.

Basic reversible logic gates:

To design reversible logic circuit needs a set of reversible logic gates. An N*N Reversible logic gate can be expressed as

IV=(I1,I2…..IN) OV=(O1,O2….ON)

Where IV and OV are inputs and output vectors. Consider the parameters to perform synthesis of reversible logic gates.

- Garbage outputs: This refers to the number of unused outputs present in a reversible logic circuit. One cannot avoid the

garbage outputs as these are very essential to achieve reversibility.

- Quantum cost (QC): This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates required to realize the circuit.
- Reversible circuit: No of reversible logic gates required to design reversible circuit.
- Transistor count: The transistor count of a reversible gate is the number of transistors used in the gate.

Feynman Gate:

Feynman gate is a 2*2 reversible logic gate. The input vector is (A,B) and the output vector is (P,Q).The outputs are defined by P=A,Q=A xor B .Quantum cost of a feynman gate is one.

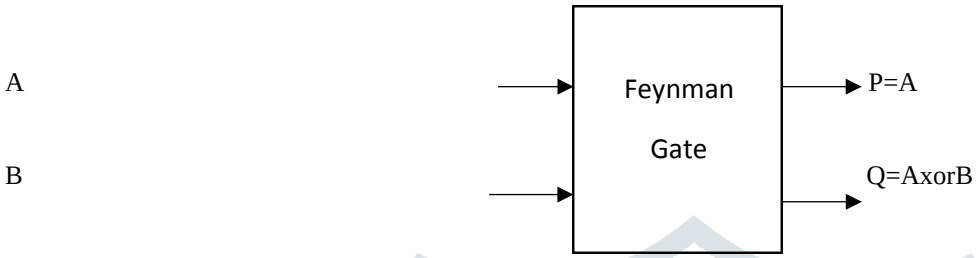

Fig1: Feynman Gate

Fredkin Gate:

Fredkin gate is a 3*3 reversible gate. The input vector is (A,B,C)and the output vector is (P,Q,R).The outputs are defined by P=A,Q=AB xor AC,R=A'C xor AB.

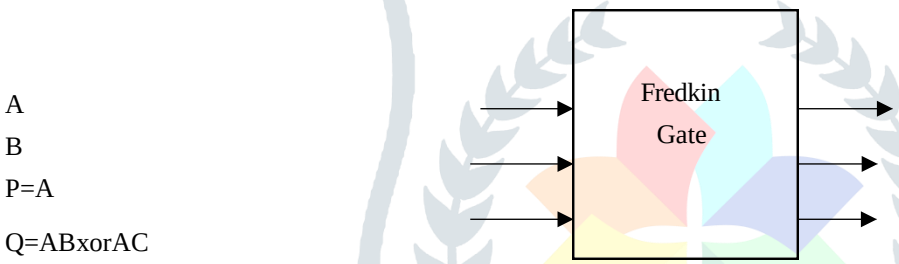

Fig 2:Fredkin Gate

Toffoli gate is a 3*3 reversible gate. The input vector is (A,B,C) and the output vector is (P,Q,R).The outputs are defined by P=A,Q=B,R=AB xor C. Quantum cost of a toffoli gate is 5.

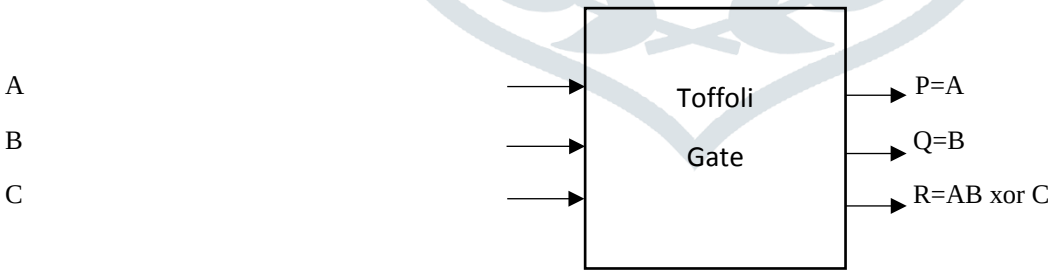

Fig 3:Toffoli gate

2:1 Multiplexer :

A PV gate is a 3*3 reversible gate which can be acts as a 2:1 multiplexer. inputs are S,A,B and the ouare G1,Y,G2.Based on the selection line input S, the corresponding message bits are passed onto the output Y. When selection line S=0, the output Y=A, if selection line S=1 the output Y=B.

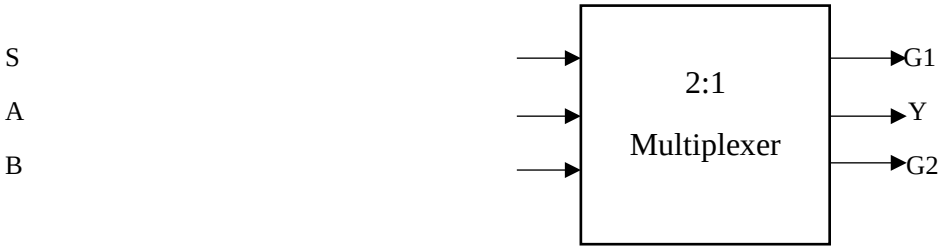

Fig 4:2:1multiplexer

SAM Gate:

A SAM Gate is a 3*3 reversible gate.The inputs is (A,B,C) and the outputs is (P,Q,R).The outputs are defined by P=Not A,Q=A NotB xor NotC. R=A NotC xor AB.

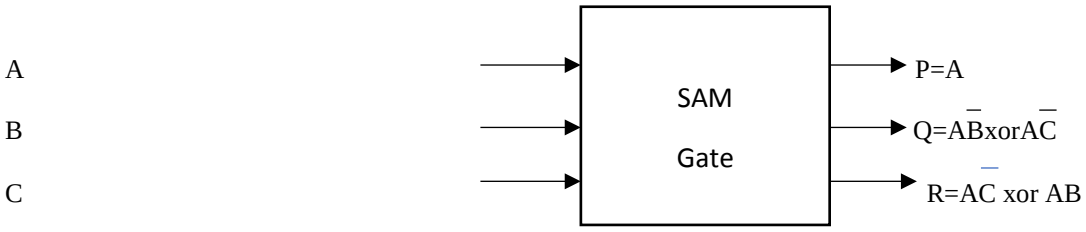

Fig 5:SAM Gate

DESIGN AND SYNTHESIS OF 2:1 MULTIPLEXER

Transistor implementation of 2:1 Multiplexer as shown in fig 6.The inputs is S,A,B and the outputs is G1,Y,G2. G1,G2 are the garbage outputs. S is the selection line. The output waveforms have carried out by tanner tools as shown in fig 7.The PV logic gate can be act as 2:1 multiplexer.

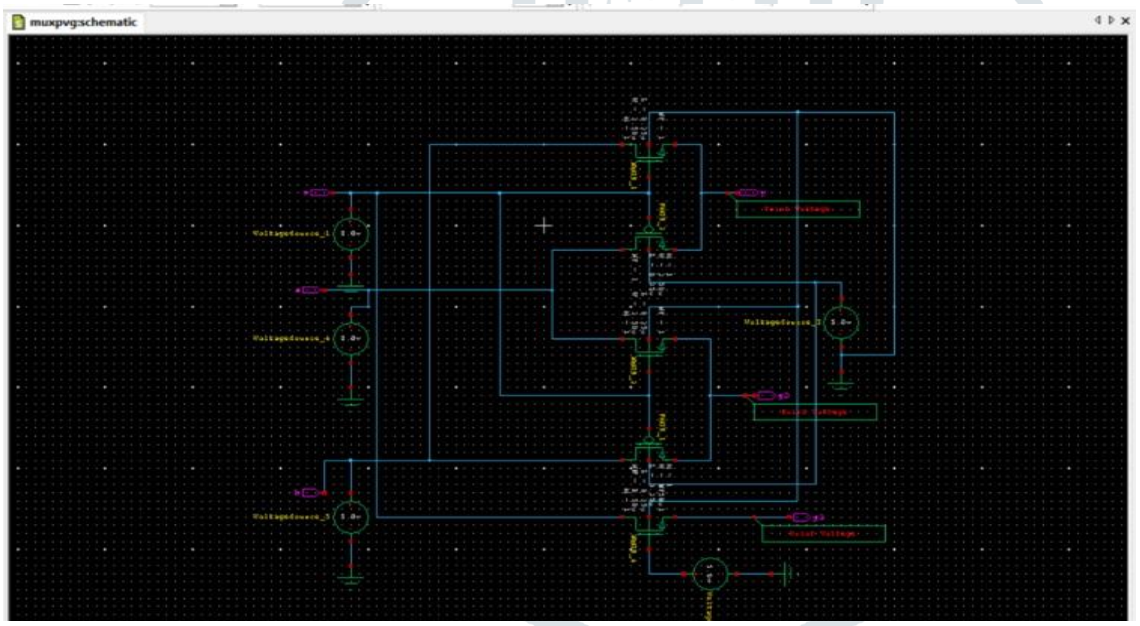

Fig6:Transistor implementation of 2:1multiplexer

In fig 6:When the Selection line is S=0 ,the PMOS transistor is ON state while NMOS is OFF state ,passing A input to the Output Y.If the selection line is S=1,the NMOS transistor is ON state while the PMOS is OFF state, Passing B input to the output.

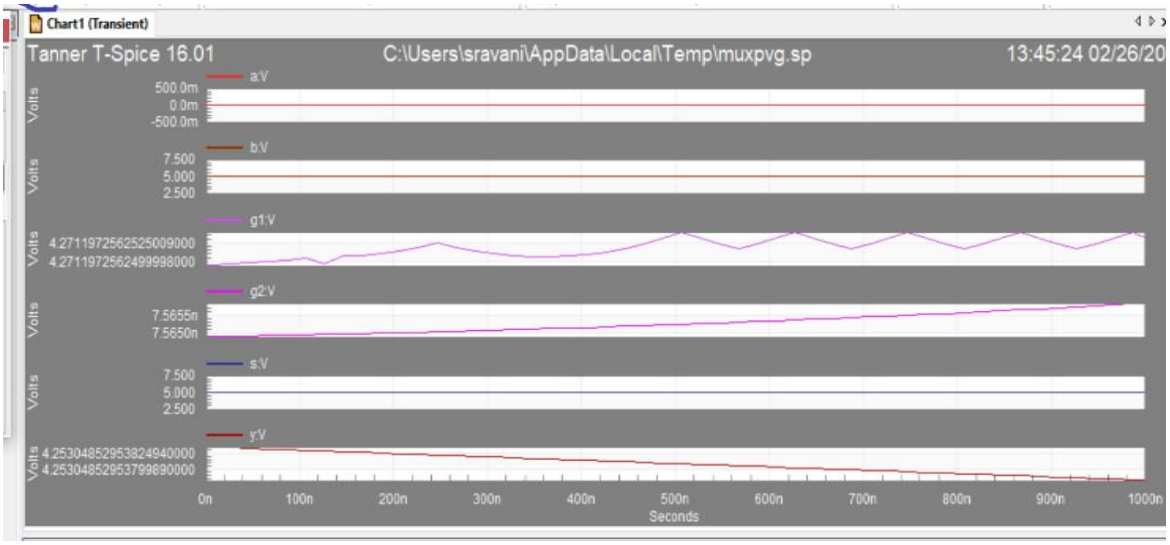

Fig 7:Simulations of 2:1multiplexer

In fig 7, from x-axis represents and time in nano seconds and y-axis represents voltage in volts.

When inputs are A=0,B=S=1 and the output is Y=0.

DESIGN AND SYNTHESIS OF JK FLIPFLOP

Using SAM Gate and Peres gate we have designed JK Flipflop.The inputs is J,K Clk and outputs is Q ,Q bar,G1,G2. The output waveforms have carried out by tanner tools.

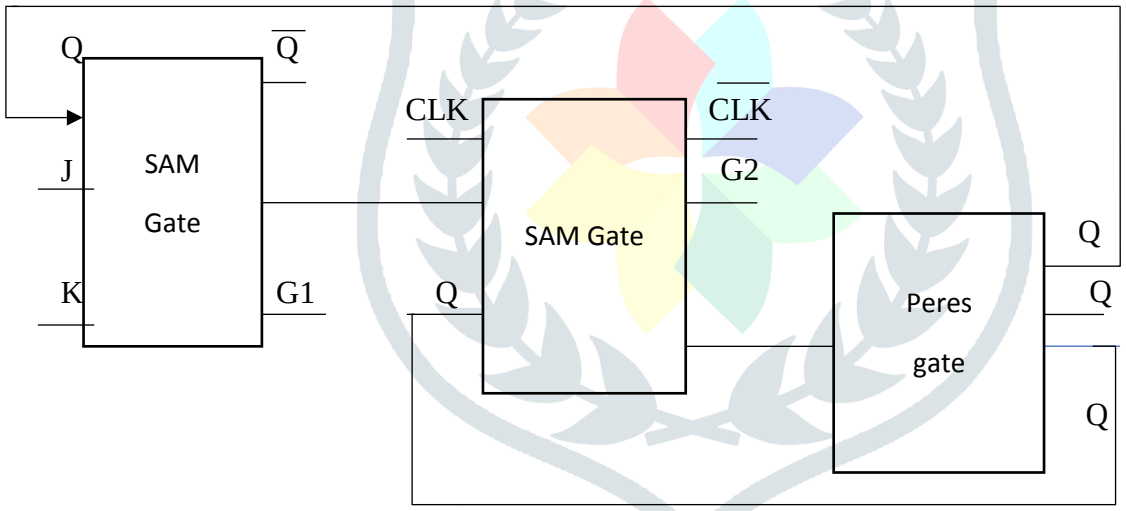

Fig 9: Block diagram of JK flipflop

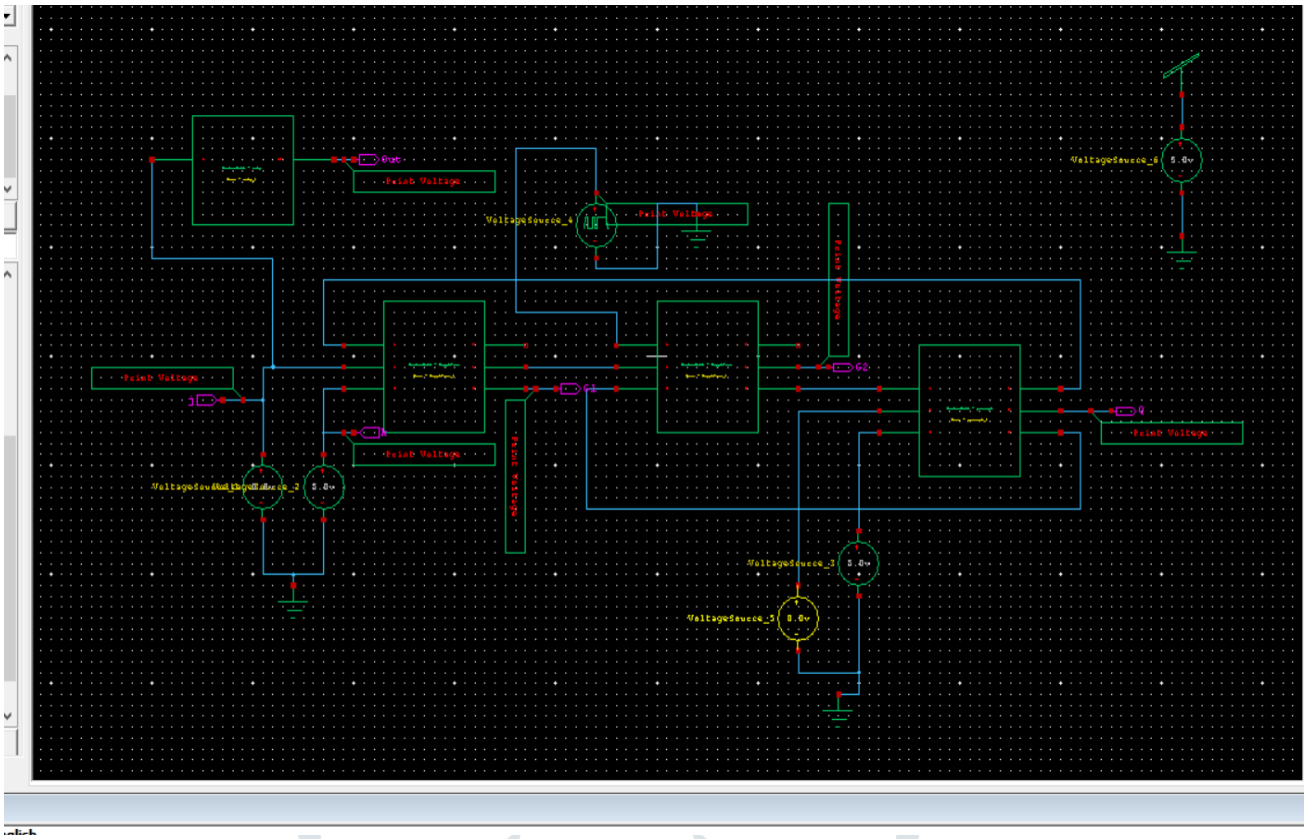

Fig 10:Transistor implementation of JK flipflop

In fig 10,transisitor implementation of JK flipflop using SAM Gate and peres gate.Here the inputs are J,K,CLKand outputs are Q,Q bar,G1,G2.

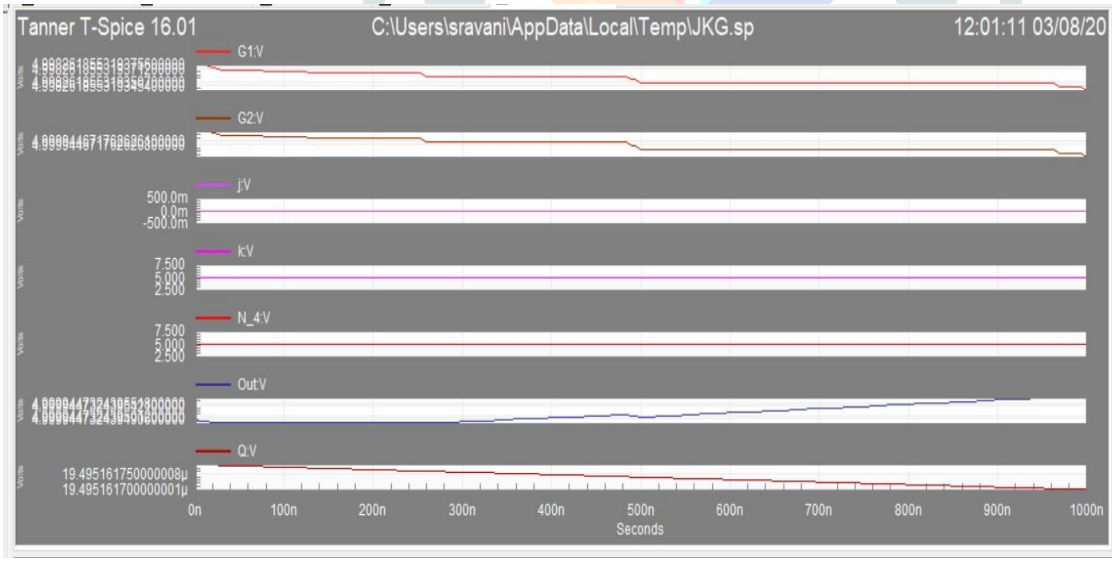

Fig 11:simulations of JK flipflop

In fig 11,from x-axis represents time in nano seconds and y-axis represents voltage in volts.

Here the inputs are J,K,Clk and outputs are Q,Q bar,G1,G2. When the inputs J=0 K=Clk=1 and the outputs are Q=0,Q bar=1 (it means set and reset condition).

PERFORMANCE COMPARISION OF JK FLIPFLOP PARAMETERS USING SIMPLE AND ADVANCED REVERSIBLE LOGIC GATES

JK FLIPFLOP	POWER CONSUMPTION	DELAY
Using Simple reversible logic gates	2.49Mw	2.18ns
Using Advanced reversible logic gates	2.01Mw	1.59ns

Fig 12:comparision of JK flipflop parameters with simple and advanced reversible logic gates

In fig12,the performace comparision between JK flipflop with simple and advanced reversible logic gates parameters in terms of power consumption and delay.

conclusion

This paper deals with the reversible logic gates and transistor implementation of 2:1Multiplexer and JK flipflop using advanced reversible logic gates. Performace comparision between JK flipflop parameters with simple reversible logic gates and advanced reversible logic gates in terms of power consumption and delay.

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