Survey Paper on Reversible Arithmetic Unit Based on Programmable Gate Structure

Ravi Ranjan[1*], Dr. Neetesh Raghuwanshi[2], Prof. Dr. Bharti Chourasia[3]
[1]M. Tech. Scholar, Department of Electronics and Communication, RKDF Institute of Science & Technology, SRK University, Bhopal,
[2]Assistant Professor, Department of Electronics and Communication, RKDF Institute of Science & Technology, SRK University, Bhopal,
[3]Associate Professor & HOD, Department of Electronics and Communication, RKDF Institute of Science & Technology, SRK University, Bhopal.

Abstract- Power crisis is a vital problem in today's world. In recent years, the growing market of electronic systems suffers from power dissipation and delay removal problem. Bennett et al. proved that the one-to-one mapping between the inputs and outputs of reversible circuit drastically reduces the power consumption and delay consumed of a circuit. There are four major design parameters of reversible circuits. First is the gate count which is the number of gate are used in the circuit. Second is the quantum delay. Third is the number of ancilla inputs which are constant inputs which are used to maintain the reversibility of the device. Fourth is the number of garbage outputs i.e. output signals which are not used as inputs to other gates and are only there to maintain reversibility. In this paper the survey of design central processing unit based on reversible gate and parameter.

Keywords—Reversible Gates, Arithmetic Logic Unit (ALU), Garbage Output, Quantum Cost.

I. INTRODUCTION

Reversible logic could also help to potentially recover and retain a fraction of the signal energy that can be reused for subsequent operations by doing the computation using the forward path and then undoing the computation using the backward path. These concepts have been implemented in CMOS to save significant amount of energy dissipation even close to 90% using the concepts such as reversible energy recovery logic (RERL) etc [1, 2]. Reversible logic has also promising applications in online and offline testing of faults. For example, it has been proved by researchers that for reversible logic circuits, the test set that detects all single stuck-at faults can also detect multiple stuck-at faults [3]. Further, such a logical structure must possess the same number of inputs and outputs and a one-to-one mapping between the input and output states. Any device designed to these constraints is known as a reversible logic device.

A few critical measurements should be considered in the outline of reversible circuits the significance of which should be talked about. The steady contribution to the reversible quantum circuit is called the ancilla info qubit (ancilla information bit), while the trash yield alludes to the yield which exists in the circuit just to keep up coordinated mapping however is not an essential or a helpful yield. Quantum PCs of numerous qubits are to a great degree hard to acknowledge in this manner the quantity of qubits in the quantum circuits should be minimized.

The importance of minimizing the garbage and ancilla bits could be best illustrated with an example. Suppose there is a need to realize 6 inputs and 4 outputs function in a quantum computer and the design requires 6 additional garbage outputs (that is have the 4 constant inputs). This will result in a reversible function having 10-inputs and 10 outputs. Suppose the best realizable quantum computer due to technology limitations had only 7 qubits, thus we will not able implement the required design. This sets the major objective of optimizing the number of ancilla input qubits and the number of the garbage outputs in the reversible logic based quantum circuits. Additionally, there are number of implementation platforms that are being explored for physical implementations for qubits and quantum gates [4].

Some of these implementation platforms are trapped ions, spintronics, superconducting circuits, linear optics/ photonics, quantum dots, etc. [5]. There is no clear winner and it is not sure which implementation technology will be the future of the quantum computers. Thus there is a need of technology independent design and synthesis of reversible logic circuits that are applicable to quantum computing. The reversible circuit has other important parameters of quantum cost and delay which need to be optimized. The quantum cost of a design is the number of 1x1 and 2x2 reversible gates used in its design thus can be considered equivalent to number of transistors needed in a conventional CMOS design.

II. LITERATURE SURVEY

Vandana Shukla et al. [1], omputerized circuits have been essentially connected to each field of life. Low power proficient frameworks are the need of this time. Reversible rationale approach is the essential result of this need. Reversible innovation is broadly appropriate in the field of nanotechnology, low control CMOS plan, optical figuring and so forth. Reversible methodology essentially expects to overhaul any advanced circuit with reversible structure units. Here, we propose a productive way to deal with structure N-bit Adder/subtractor utilizing reversible approach. In light of proposed N-bit adder/Subtractor plan we have likewise thought about 4-bit, 8-bit and 16-bit circuits with the current structures. Proposed plans are reproduced and incorporated with Xilinx Spartan 3E for Device XC3S500E at 200 MHz recurrence.

Jayashree H V et al. [2], quantum Computation and Quantum information is the major parameter of reversible circuit.. Quantum mechanics is a mathematical framework or set of rules for the development of physical theories. Quantum computation taught us to think physically about computation, and this approach yields many new and exciting capabilities for information processing and communication. In the broadest terms, any physical theory, not just Quantum mechanics, may be used as the basis for a theory of information processing and communication. One of the messages of Quantum computation and information is that new tools are

available for those problems that are relatively more difficult or impossible to solve on Classical computers. Quantum computing believes that what is computable and what is not computable is limited by the Laws of physics.

Hatkar Hatkar et al. [3], reversible rationale is all that much sought after for the future figuring innovations as they are known not low power scattering having its applications in Low Power CMOS, Quantum Computing, Nanotechnology, and Optical Computing. Adders and multipliers are major building obstructs in numerous computational units. In this paper we have introduced and executed reversible Wallace marked multiplier circuit in ASIC through changed Baugh-Wooley approach utilizing standard reversible rationale entryways/cells, in view of corresponding pass transistor rationale and have been accepted with reenactments, a design versus schematic check, and a configuration standard check. It is demonstrated that the proposed multiplier is better and upgraded, contrasted with its current partners as for the quantity of doors, consistent inputs, waste yields, equipment multifaceted nature, and number of transistors required. It has additionally been appeared in Cadence's devices that the reversible multiplier beat the irreversible multiplier as far as force dissemination.

Matthew Morrison et al. [4], proposed the outline of two programmable reversible rationale door structures focused at ALU execution and their utilization in the acknowledgment of a productive reversible ALU is illustrated. The proposed ALU configuration is checked and its points of interest over the main existing ALU outline are quantitatively analyzed. Reversible rationale is generally being considered as the potential rationale configuration style for usage in present day nanotechnology and quantum figuring with negligible effect on physical entropy. Late advances in reversible rationale take into account enhanced quantum PC calculations and plans for comparing PC architectures. Huge commitments have been made in the writing towards the configuration of reversible rationale door structures and number-crunching units, nonetheless, there are very few endeavors coordinated towards the outline of reversible ALUs. In this paper, we propose the outline of two programmable reversible rationale door structures focused at ALU execution and their utilization in the acknowledgment of a proficient reversible ALU is illustrated. The proposed ALU configuration is confirmed and its preferences over the main existing ALU outline are quantitatively investigated.

Mr. Abhishek Gupta et al. [5], presently days the majority of the circuits which are going to be designed to perform any particular or wellbeing discriminating operations are mainly based upon the advanced space, where microchips and microcontrollers assumes an imperative part to outline these computerized circuits. ALU is the heart of these processors. By upgrading this co-processor a highly effective computerized processor can be acquired. So this paper is totally given to outline speed, vitality and force effective Arithmetic Logic Unit. Pace of ALU is significantly relies on the velocity of increase unit. There are such a variety of increases procedures have been conceived at algorithmic and basic level. After an intensive study and profound investigation we have found that Vedic Urdhva Triyambakam duplication calculation is the best calculation as it produces partial products in the parallel way. In this paper we have proposed another tree augmentation structure based construction modeling to plan this Vedic multiplier.

H. Thapliyal et al. [6], to create a programmable reversible arithmetic logic circuit is based on the different reversible gate. For the expansion of halfway created items another expansion tree structure has been proposed. It provides better speed in correlation Array, Booth, Wallace, Modified Booth Wallace, Karatsuba and Vedic Karatsuba Multiplier and additionally it is faster than Vedic multiplier which has been proposed by L. Shriraman and Devika Jaina. To make ALU vitality and force effective, once again reversible rationale entryway has been proposed which is like Fredkin Gate. In the wake of incorporating these modules we have acquired the velocity, vitality and force effective ALU. The proposed Arithmetic Logic Unities coded in Verilog HDL, blended and recreated utilizing Xilinx ISE9.2i programming.
Pace of ALU is significantly relies on the velocity of increase unit. There are such a variety of increases procedures have been conceived at algorithmic and basic level. After an intensive study and profound investigation we have found that Vedic Urdhva Triyambakam duplication calculation is the best calculation as it produces partial products in the parallel way. In this paper we have proposed another tree augmentation structure based construction modeling to plan this Vedic multiplier. To create mostly created items gap and conquer approach has been utilized. For the expansion of halfway created items another expansion tree structure has been proposed.

Table 1: Summary of Literature Review

S. No.	Title	Authors/ Publication	Methodology	Parameter	Demerits /Scope of work
1.	Design and Performance Analysis for the Reversible Realization of Adder/Sub-tractor Circuit	Vandana Shukla, O. P. Singh, G. R. Mishra, R. K. Tiwari	Design Adder and Sub-tractor with the help of WG Gate	No. of Gate = 44, GO = 8, Q.C. = 28	Large QC/ Nano technology
2.	Berger Check and Fault Tolerant Rev. Arithmetic Component Design	Jayashree H V and Ashwin S, IEEE 2015	A reversible fault tolerant Adder/ Sub-tractor Fault tolerant logic,	AI = 12, GO = 8, GC = 24, Delay = 66	Large gate count/ Nano technology
3.	ASIC Design of Reversible Multiplier Circuit	Hatkar A. P. and Hatkar A., IEEE 2014	A reversible Wallace signed multiplier circuit	AI = 46, GO = 46, GC = 45	Large garbage output/ any digital application

4.	Design of a Reversible ALU based on Novel Programmable Reversible Logic Gate Structures	Matthew Morrison and Nagarajan Ranganathan IEEE 2013	Design RALU with the help of HNG Gate	GC =24, Delay = 22	MCPD is large/ used sign and unsigned number
5.	Design of Speed, Energy and Power Efficient Reversible Logic Based Vedic ALU for Digital Processors	Mr. Abhishek Gupta, Mr. Utsav Malviya, IEEE 2012	4x4 reversible multiplier circuit is the help of read only memory (RAM).	GC = 115	MCPD is large/ used sign and unsigned number

III. REVERSIBLE GATES

Reversible rationale is picking up significance in regions of CMOS configuration in light of its low power dissemination. The conventional entryways like AND, OR, XOR are all irreversible doors. Consider the instance of conventional AND entryway. It comprises of two inputs and one yield. Subsequently, one piece is lost every time a calculation is completed. As indicated by reality table appeared in Fig.1, there are three inputs (1, 0), (0, 1) and (0, 0) that compares to a yield zero. Subsequently it is unrealistic to decide interesting information that brought about the yield zero. With a specific end goal to make an entryway reversible extra info and yield lines are added so that a balanced mapping exists between the information and yield. This keeps the loss of data that is fundamental driver of force scattering in irreversible circuits. The info that is added to an m x n capacity to make it reversible is known as steady information (CI). Every one of the yields of a reversible circuit need not be utilized as a part of the circuit [8]. Those yields that are not utilized as a part of the circuit is called as trash yield (GO). The number of garbage output for a particular reversible gate is not fixed. The two main constraints of reversible logic circuit is

- Fan out not allowed
- Feedbacks or loops not allowed.

○ BASIC REVERSIBLE GATES

Several reversible logic gates are used in previous design. In figure 1, show the block diagram of two input (A, B) and two output (P, Q) Feynman gate.

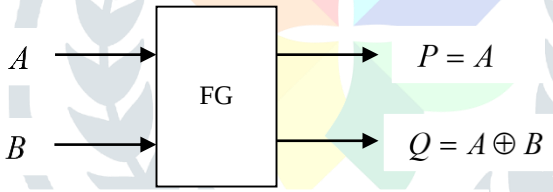

Figure 1: Feynman gate

In figure 2, show the block diagram of the three inputs (A, B, C) and three output (P, Q, R) Fredkin gate.

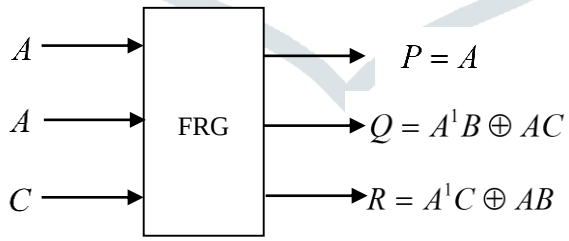

Figure 2: Fredkin gate

Figure 3 shows the Peres gate. A portion of the 4x4 doors are intended for executing some imperative combinational capacities notwithstanding the fundamental capacities. The vast majority of the aforementioned entryways can be utilized as a part of the outline of reversible adders.

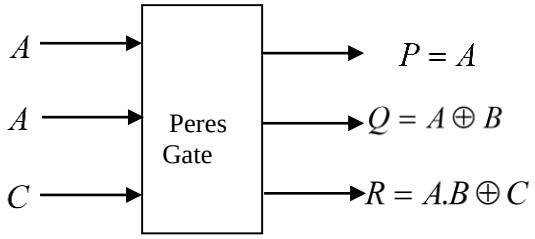

Figure 3: Peres gate

The HNG gate, presented in [10], produces the following logical output calculations:

$$P = A \quad (1)$$

$$Q = B \quad (2)$$

$$R = A \oplus B \oplus C \quad (3)$$

$$S = (A \oplus B).C \oplus (AB \oplus D) \quad (4)$$

The quantum cost and delay of the HNG is 6. At the point when D = 0, the consistent estimations created on the R and S yields are the required total and complete operations for a full snake. The quantum representation of the HNG is exhibited in Fig. 4.

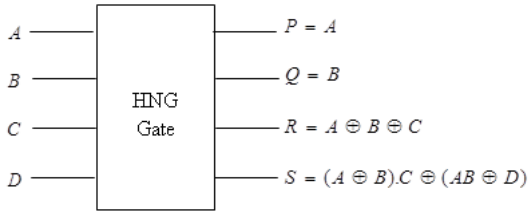

Figure 4: Block Diagram of the HNG Gate

A new programmable 4x4 reversible logic structure Peres And-OR (PAOG) gate is presented which produces outputs

$$P = A \quad (5)$$

$$Q = A \oplus B \quad (6)$$

$$R = AB \oplus C \quad (7)$$

$$S = (AB \oplus C).C \oplus ((A \oplus B) \oplus D) \quad (8)$$

Figure 5 shows the block diagram of the PAOG gate. This gate is an extension of the Peres gate for ALU realization.

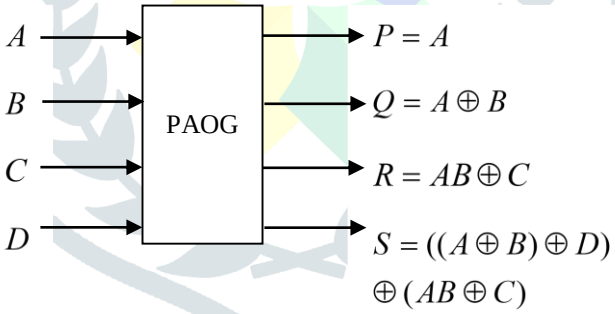

Figure 5: Block Diagram of the PAOG

IV. REVERSIBLE PARAMETER

Some of the reversible gate are NOT Gate, CNOT/ Feynman Gate, Toffoli Gate, Fredkin Gate and Peres Gate. Important parameters of any reversible circuit are as follows:
Gate Count (GC): The number of gates used to realize reversible circuit.
Garbage Outputs (GO): The number of unused outputs in a reversible logic. The inputs regenerated at the outputs are not garbage outputs.
Ancilla Inputs (AI): The number of input kept constant at either 0 or 1.
Quantum Cost (QC): The cost of the circuit in term of cost of a primitive gate.
Delay: It corresponds to number of primitive quantum gates in the critical path of the circuit.

V. PROPOSED METHODOLOGY

The architecture of the proposed reversible processor is shown in Figure 6. In this figure design the overall structure of the reversible CPU has been divided into small components.

- Layout the data bus to handle all of the operations of the reversible ALU.
- Design the reversible realizations of the flip-flops.
- Design the reversible memory circuits (such as buffer registers and counter circuits) using the proposed reversible flip-flops of the previous step.
- Design the arithmetic circuits such as adder, multiplier, divider, comparator etc.
- Design the reversible realization of ALU.

- Design the reversible control unit of the processor by designing an efficient instruction decoder.

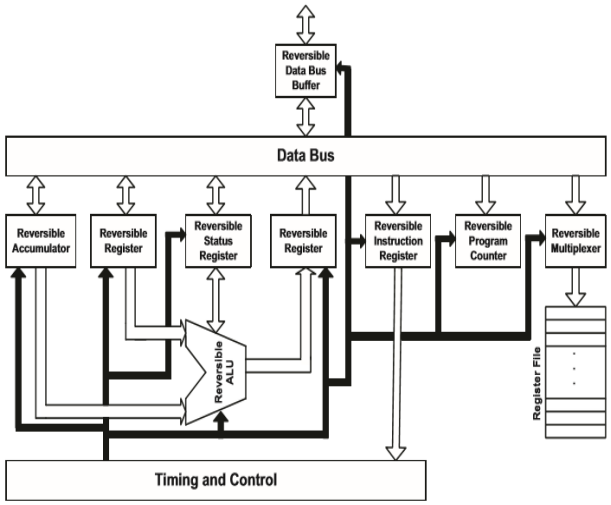

Figure 6: Flow Chart of Proposed Central Processing Unit

VI. CONCLUSION

We have tried the central processing unit is consist of adder, multiplier, divider, memory element, decoder and multiplexer in different reversible gate. The proposed RCPU design will have analyzed on Xilinx 14.1 Spartan-3 and Vertex-7 device family. The proposed design will have compared in terms of maximum combinational path delay (MCPD) and quantum cost with the existing reversible central processing unit (CPU). We can also design 4-bit to 16-bit memory element.

REFERENCE

[1] Vandana Shukla, O. P. Singh, G. R. Mishra and R. K. Tiwari, “Design and Performance Analysis for the Reversible Realization of Adder/Subtractor Circuit”, International Conference on Emerging Trends in Computing and Communication Technologies (ICETCCT), IEEE 2017.

[2] Jayashree H V and Ashwin S, “Berger Check and Fault Tolerant Reversible Arithmetic Component Design”, International Conference on Electron Devices and Solid-State Circuits (EDSSC), IEEE 2015.

[3] Hatkar A. P., Hatkar A. A. and Narkhede N. P., “ASIC Design of Reversible Multiplier Circuit”, International Conference on Electronic Systems, Signal Processing and Computing Technologies, IEEE 2014.

[4] Matthew Morrison and Nagarajan Ranganathan, “Design of a Reversible ALU based on Novel Programmable Reversible Logic Gate Structures”, Computer Society Annual Symposium on VLSI IEEE 2013.

[5] Shefali Mamataj Biswajit Das Anurima Rahaman "An Approach for Realization of 2's Complement Adder Subtractor Using DKG Reversible Gate" International Journal of Emerging Technology and Advanced Engineering vol. 3 no. 12 pp. 205-209 December 2013.

[6] Mr. Abhishek Gupta, Mr. Utsav Malviya and Prof. Vinod Kapse, “Design of Speed, Energy and Power Efficient Reversible Logic Based Vedic ALU for Digital Processors”, Computer Society Annual Symposium on VLSI, IEEE 2012.

[7] LekshmiViswanath and Ponni.M, “Design and Analysis of 16-Bit Reversible ALU”, Internatioal Conference on VLSi Circuit and Digital Signal Processing, Vol. 1, Issue 1, PP 46-53, 2012.

[8] M. Morrison and N. Ranganathan, "Design of a Reversible ALU Based on Novel Programmable Reversible Logic Gate Structures", IEEE International Symposium on VLSI, pp. 126-131, IEEE 2011.

[9] Md. Belayet Ali, Hosna Ara Rahman and Md. Mizanur Rahman, “Design of a High Performance Reversible Multiplier”, IJCSI International Journal of Computer Science Issues, Vol. 8, Issue 6, No 1, November 2011.

[10] Michael Nachtigal, “Design of a Reversible Floating-Point Adder Architecture”, 11th IEEE International Conference on Nanotechnology Portland Marriott, IEEE 2011.

[11] Maher Hawash, MarekPerkowski, Steve Bleiler, John Caughman, and Amjad Hawash, “Reversible function synthesis of large reversible functions with no ancillary bits using covering set partitions”, information Technology: New Generations, Third International Conference, IEEE 2011.

[12] D. Maslov and M. Saeedi. Reversible circuit optimization via leaving the boolean do- main. Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on, 30(6):806 –816, june 2011.