POWER EFFICIENT FREQUENCY DIVIDER CIRCUIT BASED ON ADAPTIVE VOLTAGE LEVEL TECHNIQUE

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Abstract: In the recent trends, power optimisation has become an important factor in integrated circuits. In this paper, a frequency divider circuit has been proposed which consumes less power based on adaptive voltage level at supply (AVLS) technique. In this technique, the supply voltage potential is reduced so as to reduce the power consumption of certain transistors. The aim of this paper is to investigate the power dissipation of the proposed design. The circuit is designed using DSCH and Microwind softwares using 90 nanometer and 45 nanometer technology respectively.

IndexTerms **- Frequency Divider, CMOS, 45 nanometer technology, Adaptive voltage level, AVLS.**

I. INTRODUCTION

The recent trend of compact devices in the field of electronics has led to the requirement of circuits that consume lower power as compared to their conventional counterparts. The main motivation for this low power design is the prolonged battery life and reliability.

This motivation has led to the discovery of technologies in digital systems such as NORA [2] and DOMINO [1] logic based technologies. The advantage with these technologies was that they consumed lesser power as compared to their conventional counterparts but they possessed the problem of charge sharing. This charge sharing problem can be addressed by using a single phase clocking. This led to the development of TSPC [3] logic circuits and AVL [4] design style. All the above mentioned techniques aim at reducing the dynamic power consumption.

In the field of digital circuits, sequential circuit is a circuit whose output at any state depends on the present input as well as the past state outputs. The simplest type of sequential circuit is a memory element cell which has two states. The states can either be 1 or 0. These kind of sequential circuits are called flip flops, since they flip from one state to another and then flip back to the previous state.

One of the simplest flip flops is the set reset flip flop. The disadvantage of this flip flop is that the output cannot be determined if both the inputs S and R are equal to 1 simultaneously. In order to eliminate this problem, another flip flop in which an inverter is used in addition to the input is made. This flip flop is known as a D flip flop and in this flip flop the output follows the input.

One of the key applications of the D flip flop is the frequency divider circuit, which takes the input as a frequency and produces the output whose frequency is divided by a factor of two.

The frequency divider circuits were conventionally made mainly by using either source coupled logic (SCL) [4] or injection locked topology [5]. The problem with these kind of designs was that when the devices were operated at the voltages below 1 volt, the performance of these devices degraded significantly and some of them even failed to function. The improvement over these design style were NORA and DOMINO design logic styles but they suffered from the problem of charge sharing. When the frequency divider circuit is made by using TSPC design style, it consumes lesser power and the problem of charge sharing which was apparent in NORA and DOMINO logic is reduced further.

II. PROPOSED FREQUENCY DIVIDER CIRCUIT

In the proposed frequency divider, we are going to use an AVLS based D flip flop which is inherently based upon TSPC design style. For the designing of this frequency divider circuit we are going to provide the output of the circuit in feedback to the input of the circuit. The AVLS circuitry applied at the supply side is going to reduce the supply voltage and this reduction in supply voltage subsequently results in lesser power consumption of the transistors. The purpose of clk2 and the control circuit which consists of transistors T1, T5 and T6 is to reduce the leakage power consumption.

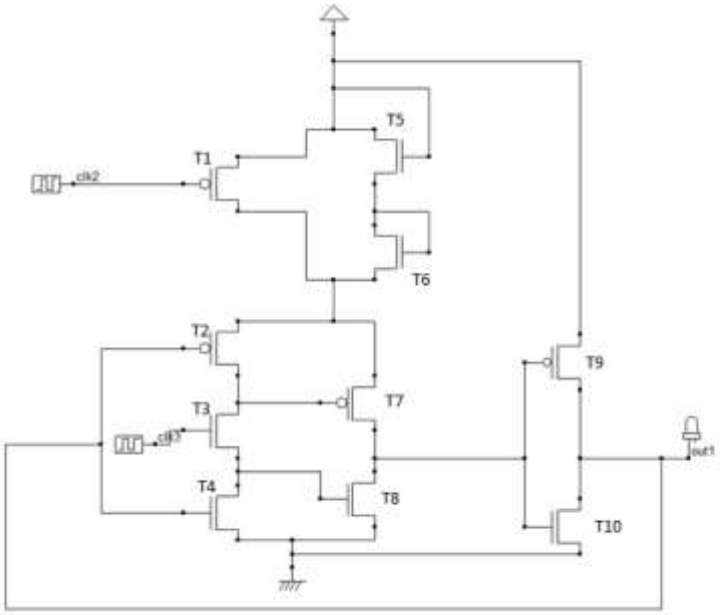

Figure 1: Schematic representation of frequency divider circuit using AVLS technique.

III. SIMULATION AND RESULTS

The simulation is done on MICROWIND 3.5 and its DSCH tool.

The simulation shows the relation between the input frequency clk3 and output frequency frediv_out1. The output frequency is divided by a factor of 2.

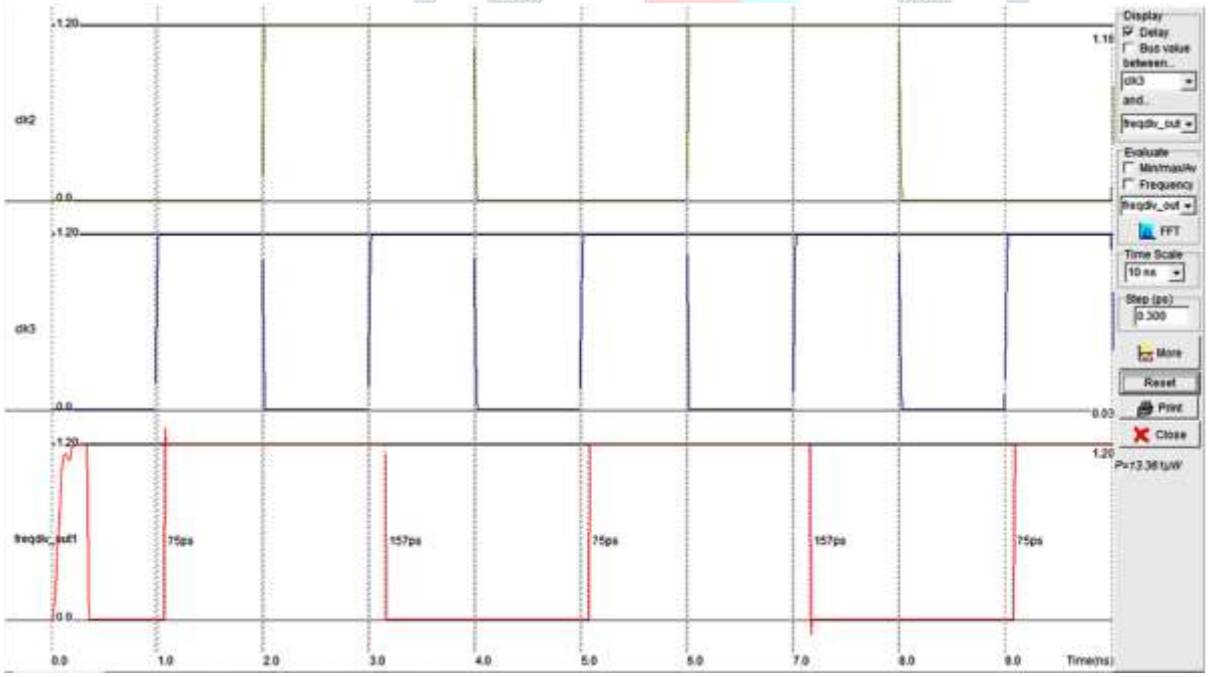

Figure 2: Waveform and Power consumption of the proposed circuit using 90 nm technology.

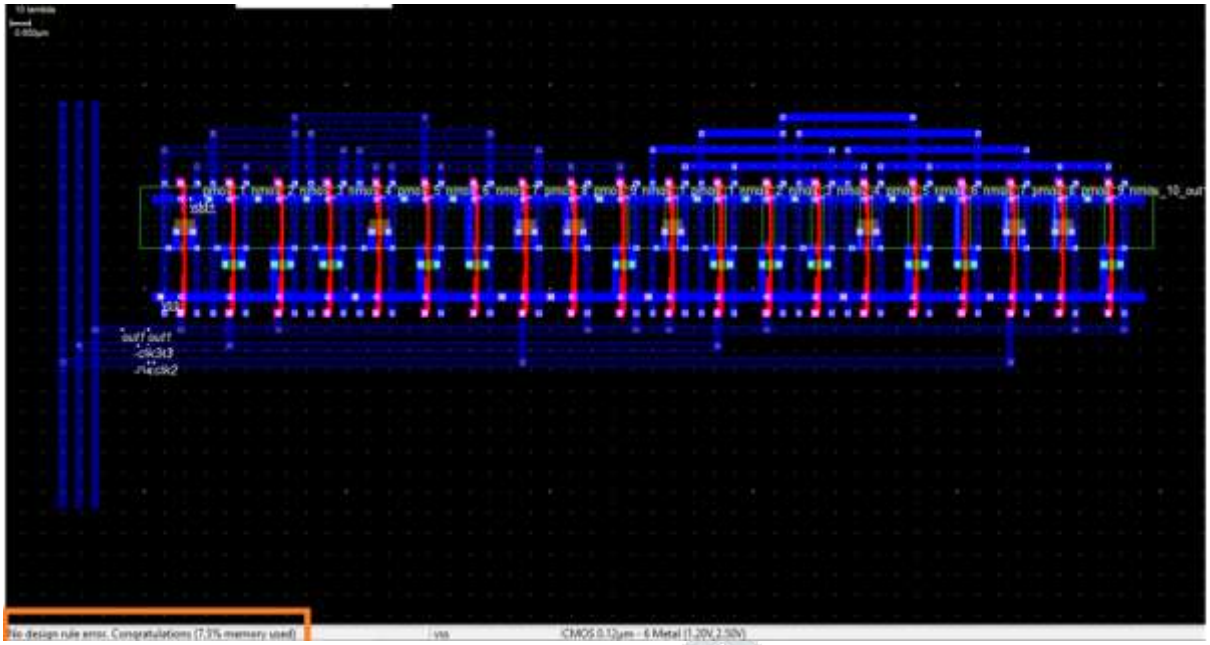

Figure 3: Layout design of the proposed circuit using 90 nm technology. The orange box shows there is no design rule error.

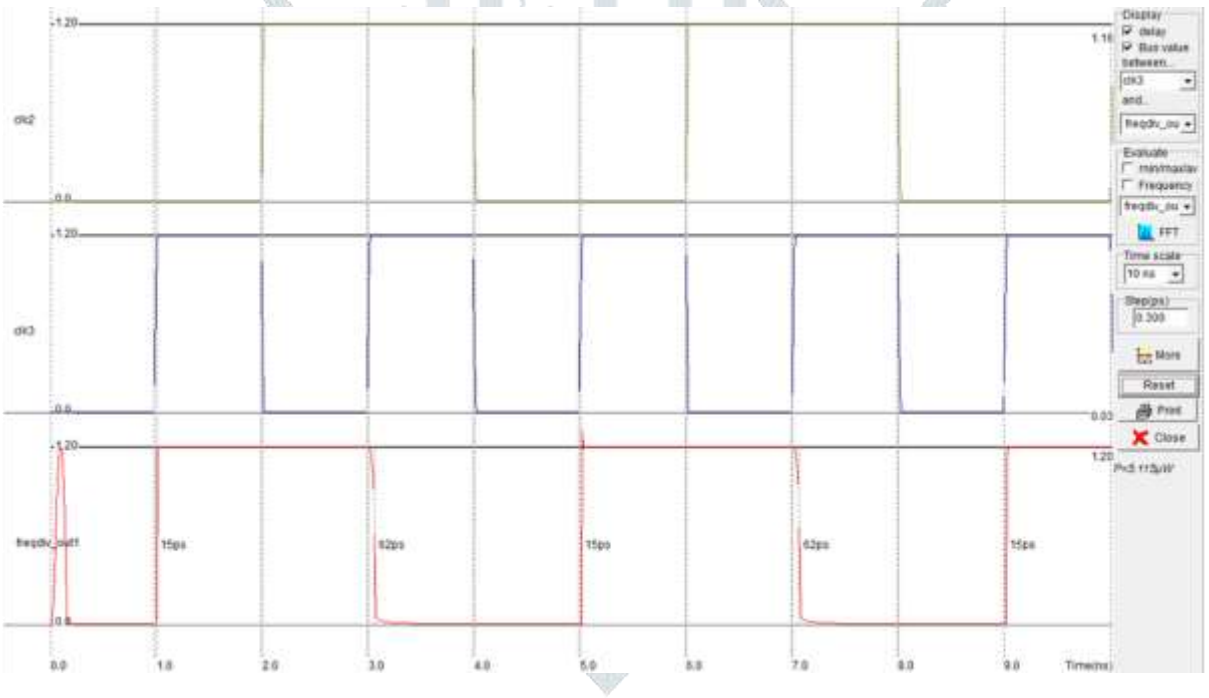

Figure 4: Waveform and Power consumption of the proposed circuit using 45 nm technology.

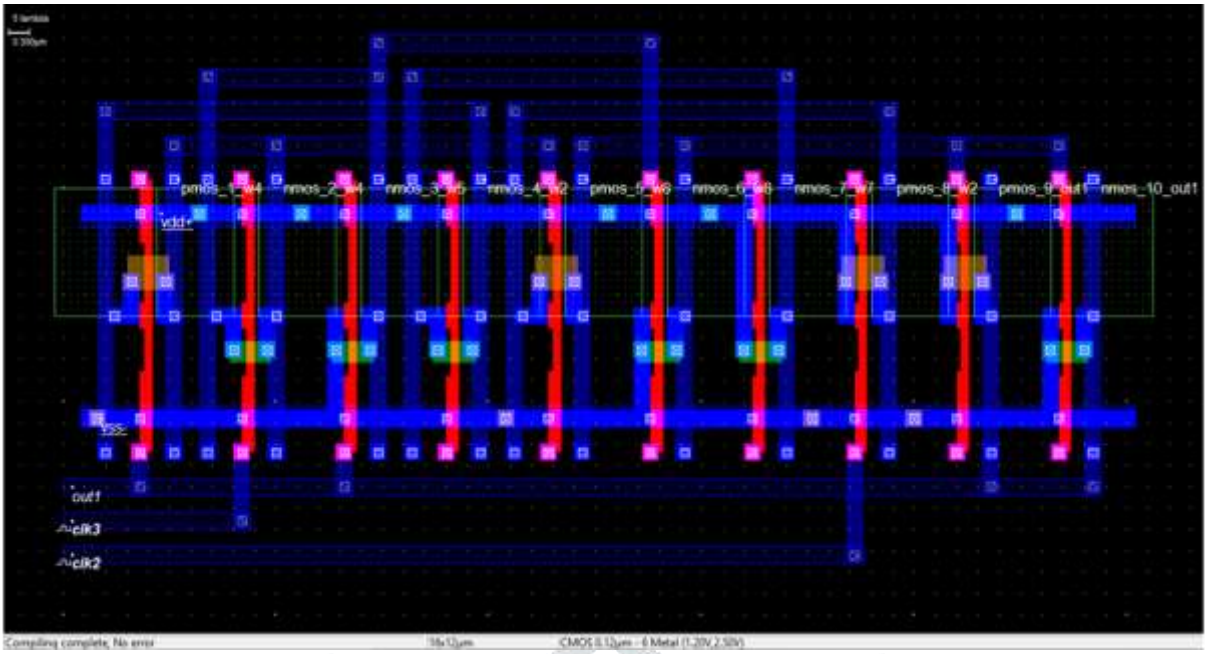

Figure 5: Layout of the proposed circuit using 45nm technology.

IV. RESULTS AND DISCUSSION

We have been able to achieve a power reduction of 99.5% power reduction when the circuit is implemented by using 45 nanometer technology compared to a contemporary design by Kailuke[9] and the reduction in layout area is 74.61%. The circuit is able to process maximum frequency of 12.5 Giga Hertz, which is good when compared to other frequency divider circuits. The only drawback is the lowest frequency of operation which is 200 Mega Hertz. The circuit by Kailuke [9] was able to process frequencies as low as 2 Mega Hertz. This makes the proposed circuit suitable for low power applications.

Table 1: Comparison of parameters of Contemporary Frequency Divider circuits with the proposed circuits.

PARAMETER	RAZAVI[7]	KAILUKE[9]	PROPOSED CIRCUIT USING 90nm	PROPOSED CIRCUIT USING 45nm
TECHNOLOGY	0.1µm	0.18µm	90nm	45nm
POWER CONSUMPTION	2.6mW	1mW	13.36µW	5.115µW
MINIMUM OPERATING FREQUENCY	5GHz	2MHz	200MHz	200MHz
MAXIMUM OPERATING FREQUENCY	13.6GHz	2.3GHz	12.5GHz	12.5GHz
NUMBER OF TRANSISTORS	12	12	10	10
LAYOUT AREA	3500µm^2	756.3µm^2	384µm^2	192µm^2

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