An Assessment on Delay and Power in Sequential Circuits and Efficient Designing Architectures

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Abstract: Sequential circuits are the key component in most of the VLSI system. Power utilization is a major task in integrated circuits. Behaviour of the sequential circuits depends upon the clock signals. Hence the clock signal contributes to the delay in the circuit and power dissipation because of the internal transistors. Power minimization techniques need to be used in the circuit design for efficient working. Here we have discussed in detail the types of delay and the sources of power dissipation and the techniques to measure it. We have also mentioned some predefined models that are effective in reducing the delay and power dissipation in the sequential circuit. This paper is the review of the existing techniques that are used to design a low power and high-speed synchronous circuit. The prime focus of our work is to summarizing the circuit performance characteristics like delay, power, and area utilization**.**

IndexTerms **- Sequential Circuit, Delay, Power Dissipation, Adiabatic Logic, Clock Gating, Power Gating, Dual-Edge Triggering, Near-Threshold Voltage.**

1. INTRODUCTION

Power optimization and speed of operation are the main area of interest for Integrated Circuit design engineers. SoC provides different digital blocks embedded on a chip for multifunctionality and therefore within the restricted area a larger number of components need to be fabricated [1]. The number of transistors is getting increased within the restricted chip size contributing to more power dissipation in the circuit. Hence different power minimization techniques need to be used for efficient working of the circuit [2]. On the other hand, system performance in terms of speed is also a major concern. Most of the VLSI system consist of sequential circuits which contain memory elements like flip-flop, and clock generating system. Flip-flops changes their state for every rising or falling edge of the clock. This means that the output of the flip-flops depends on the external input and the clock signal. Due to this dependency on the clock, the response of the flip-flops experiences a significant amount of delay. These unwanted characteristic effects the performance of the circuit. Therefore, we need to optimize the power consumption is the circuit and reduce the delay in the system. This paper suggests some techniques that are dedicated for the problem stated above.

This paper is organized as follows: section 2 gives an overview of Sequential Circuits, section 3 describes the type of power dissipation and its sources, a detailed note on delay in sequential circuits is given in section 4, section 5 describes delay and power efficient architectures and section 6 and 7 with conclusions and future scope respectively.

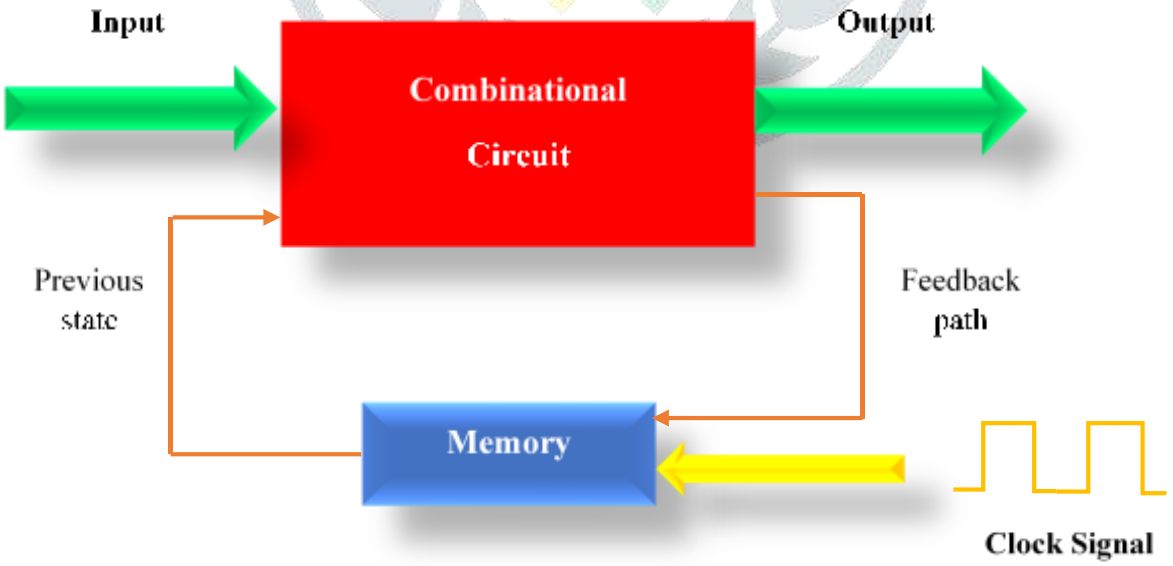

Figure 1 Block Diagram of Sequential Circuits

2. A BREIF OVERVIEW OF SEQUENTIAL CIRCUITS

A sequential circuit is one whose output depends on the present input and previous state of the system. Figure 1 shows a typical block diagram of sequential circuit. It contains a combinational circuit having external input and previous output as its input. The output is fed back to the input via a memory element. The memory element is triggered by the clock signal. Flip-flops are used to store the data in the form of bits. Various types of flip-flops are used depending upon the application. T flip-flop is preferred in

synchronous counters whereas D flip-flops are used in data shift registers. The terms shown in the block diagram of sequential circuits are described here in detail.

Figure 2 Combinational Logic Circuit

2.1 Combinational circuit

As the name suggests, a combinational circuit is the one having combination of different logic gates. Its output at any instant of time depends on the present input. There are n number of inputs and m number of outputs. Some common examples of combinational circuits are half adder, decoder, encoder, multiplexers etc.

2.2 Input/Output buses

Input/output buses are the group of wires at respective terminal of the block. These buses are unidirectional as indicated by the arrows. m, n are integers and they need not to be equal. The number of inputs can be less than number of output or vice versa. For example, decoder has less number of input lines than output and MUX having more input and single output.

2.3 Feedback Path and Previous State

As it was mentioned earlier that the output of sequential circuit depends upon externally applied input and previous output. The previous output is nothing but the previous state of the system for the next clock cycle. This previous state is given to the input through a feedback path.

2.4 Clock Signal

This signal is used to trigger the memory element. The flip-flops are triggered either on rising edge or falling edge. The frequency of the clock signal is known as the frequency on which the system is operating or operating frequency.

2.5 Memory

These are the elements used to store the present state of the system for the next state. Flip-flops are used as the memory elements as the store data in the form of bits. The output of the flip-flops is given as input to the system along with the external input. Most of the power dissipation and delay took place in the memory elements. Hence the proper designing of the flip-flops is the matter of concern.

3. CLASSIFICATION OF POWER DISSIPATION AND ITS SOURCES

Power dissipation is broadly classified into two types: static power dissipation and dynamic power dissipation [3]. In a digital CMOS circuit, leakage current and standby current are the sources of static power dissipation. The leakage current is due to sub-threshold conduction when the circuit is in inactive state, reverse bias current in the parasitic diodes, gate tunnelling current etc. The standby current is the DC current drawn uninterruptedly from supply voltage (VDD) to ground and the standby power is the product of supply voltage and standby current.

On the other hand, dynamic power dissipation is more dominant in digital circuits. In CMOS circuits the node voltage takes high-to-low and low-to-high transitions frequently. This transition contributes the most in the dynamic power dissipation. In some cases, even if the output is at a stable logic the internal nodes experience charging and discharging which causes unnecessary power consumption. Another source of dynamic power is short circuit current which flows because of the momentary shorting of VDD and ground during change of logic levels [3].

Equation 1 depicts the power dissipation due to charging-discharging of the node capacitances, also known as capacitive power dissipation:

$$P = \frac{1}{2} C_L V_{DD}^2 E(sw) f_{clk} \quad (1)$$

where C_L : capacitance at the output of the node

V_{DD} : supply voltage

$E(sw)$: switching activity

f_{clk} : clock frequency

Now the total dynamic power dissipation can be estimated by adding a virtual short circuit capacitance C_{SC} due to short circuit power dissipation with C_L in equation 1 shown above [3]. Table 1 shows the types of power dissipation, their sources with their description in digital CMOS circuit. On the basis of these analysis it is clear that the power dissipation due to signal toggling is foremost. Hence the aim is to reduce this dynamic power. Section 5 gives a clear insight on the techniques that are used to decrease this power consumption.

Table 1 Types of Power Dissipation and their Sources

Type of power dissipation	Source of dissipation	Description
Static power dissipation	Leakage current	The leakage current is due to the reverse bias current generated in the device. A MOSFET can be seen as a two-diode configuration, one between drain and bulk and another between source and bulk. These two diodes in reverse bias contributes in the leakage current.
	Standby current	Standby power dissipation happens because of the DC current drawn from the supply voltage to ground. This power will be the product of DC current and V_{DD}.
Dynamic power dissipation	Short circuit current	At the time of signal transition, a temporary path exists between the power supply and ground. This causes short circuit current to flow in the circuit. This power dissipation doesn't contribute much in the dynamic power dissipation, nearly 5-10%.
	Capacitive current	The transition of the signal from low-to-high and vice versa contributes more in dynamic power dissipation. Due to the signal transition the node capacitances get charged-discharged and therefore consumes huge amount of energy.

4. DELAY IN SEQUENTIAL CIRCUITS

From the figure 1 it can be understood that the sequential circuit is a group of combinational circuit and memory elements like flip-flops. Here we will discuss about the timing characteristics of the combinational circuits and flip-flops. Figure 3 shows the classification of delay in sequential circuits and each delay parameter is described here in detail with example.

4.1 Timing characteristics in combinational logic circuit

The output in combinational circuits at any instant of time depends only at the input applied. The circuit response is not instantaneous rather it experiences a certain amount of delay which is characterized by two parameters namely, Propagation delay (t_{pd}) and Contamination delay (t_{cd}) [4]. These delays are on the order of picoseconds to nanoseconds.

4.1.1 Propogation delay (t_{pd}): This is the time difference of change in the output logic level due to change in the input logic level. After t_{pd} the output maintains a stable logic and no further change in the output can be seen until the input is changed. Propagation delay should be made as low as possible for proper functioning of the device.

4.1.2. Contamination delay (t_{cd}): This is the time taken by the output signal to initiate the change in its logic level because of the change in input logic level. After t_{cd} the output enters into an intermediate value and then finally reaches the desired logic level.

Figure 4(a) shows the propagation delay and contamination delay in case of an AND gate. Initially the input X and Y are at logic 0 (or LOW logic level) and correspondingly the output Z of AND gate is logic 1 (or HIGH logic level). Now X and Y makes a transition from LOW to HIGH simultaneously but the output Z remains at LOW logic level for a certain time and this is called Contamination delay. After this the AND gate response is in between intermediate values indicated by crosses and finally maintains HIGH logic level and this complete duration is termed as Propagation delay. Here we have shown that both the inputs X and Y takes the value of logic 1 simultaneously. It is not practically possible for two signals to make a similar transition at exactly same point instead there will be a very small delay (in picoseconds) between the two inputs. But for simplicity we have neglected this issue and considered an ideal case to understand the concept of propagation delay and contamination delay easily.

4.2 Timing Characteristics in Sequential Logic Circuit

Here the flip-flops change their state when the clock signal makes transition. This means that the clock is the input responsible for the triggering of the flip-flops. Therefore, the delay associated in sequential circuits are related to clock signal. Timing parameters for the sequential circuit is listed below. These parameters are also the order of picoseconds to nanoseconds

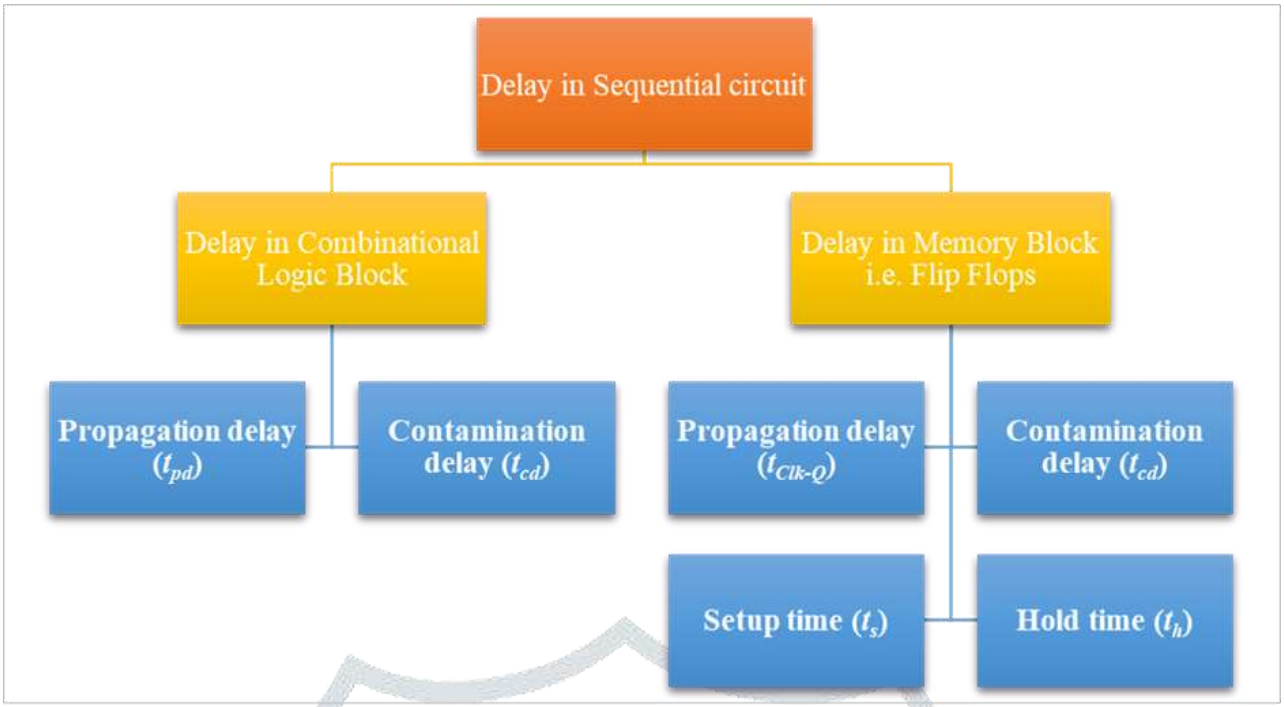

Figure 3 Types of Delay in Sequential Circuits

4.2.1 Propagation delay (t_{Clk-Q}): This is also known as Clock-to-Q delay. When the clock makes a transition (rising or falling) the output of the flip-flop changes. This change in the output is not sudden and the amount of time required by the flip-flop to reflect the new output is called propagation delay [5]. This is called clock-to-Q delay because it is the time difference of the instant at which clock signal and Q are at 50% of their steady state values.

4.2.2 Contamination delay (t_{cd}): This is the time required by the flip-flop to initiate the logic level change in its output at the time clock signal makes a transition (rising or falling).

4.2.3 Setup time (t_s): This is the time required for the input signal to be at a stable logic level before the clock makes transition [5].

4.2.4 Hold time (t_h): This is the time required for the input signal to be at a stable logic level after the clock makes transition [5].

Table 2 Literature Survey Of Timing Parameters Of Sequential Circuit

S.No.	Book Chapter	Author	Remark	Book/Publication
1.	Combinational Logic Design. (Chapter 2)	Sarah L. Harris and David Money Harris	In the second chapter of this book the authors have explained the working of the combinational circuits in detail. The delay associated with the combinational blocks are given with proper examples and figures. This chapter deals with the implementation of the circuit design with multiple logic gates, multilevel combinational block, their Karnaugh map simplification and the timing parameters.	Digital Design and Computer Architecture.
2.	A Quick Overview of Electronic Hardware. (Chapter 2)	Swarup Bhunia and Mark Tehranipoor	Here we get a quick overview of the electronic hardware, circuit theory, embedded systems, ASICs, FPGA etc. Section 2.3.4.2. gives an insight of the timing parameters of sequential circuits. Propagation delay, setup time, hold time are explained clearly with examples.	Hardware Security, A hands-On learning Approach.

In Table 2, we have discussed the books that are referred to understand the terms related to delay in combinational circuits as well as sequential circuits. Setup time and Hold time are necessary for the sequential circuit for their proper functioning. The input signal must maintain the logic level for t_s plus t_h amount of time. If this condition is not fulfilled then the circuit will not work properly. In figure 4(b) a T flip-flop is shown and the timing diagram along with the delay parameters are given. We know that the output of T flip-flop toggles for T = 1. We have shown this case in the timing diagram. Initially the output Q is at logic 0 and logic 1 is applied at the T input. The flip-flop here is assumed to be positive (rising) edge triggered. For the rising edge the output Q toggles but not rapidly. The Q maintains its previous value till t_{cd} units and then changes its logic level to HIGH the total delay in

toggling the output is $t_{clk\text{-}Q}$. It can be clearly visible from the waveforms that the input T is stable at logic 1 before and after the rising edge of the clock for t_s and t_p units respectively.

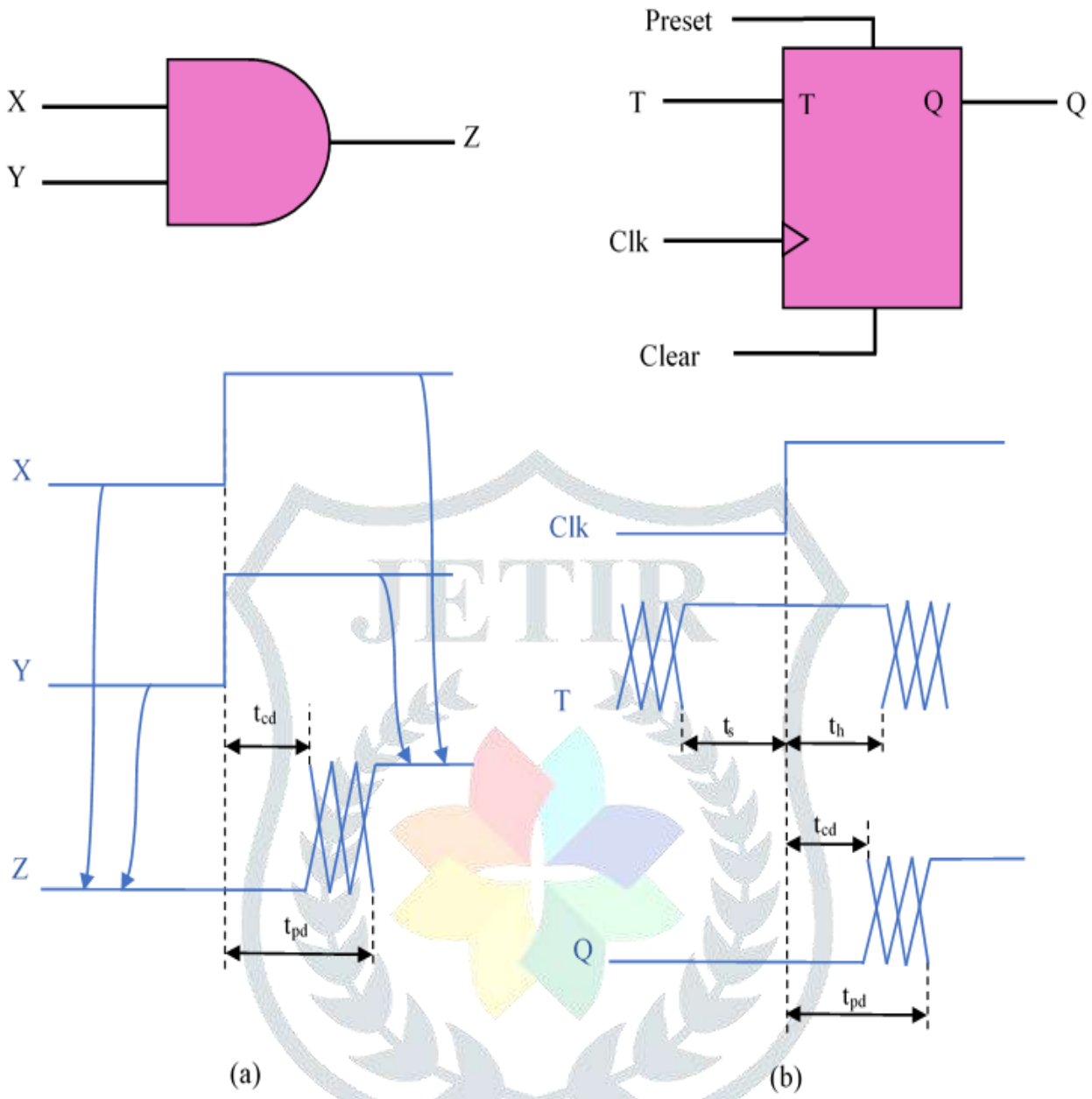

Figure 4 Timing Parameters in Sequential Circuits. (a) Propagation Delay and Contamination Delay in Combinational Circuits. (b) Propagation Delay, Contamination Delay, Setup Time and Hold Time in Sequential Circuits

5. DELAY AND POWER EFFICIENT ARCHITECTURES IN SEQUENTIAL CIRCUITS

There are many power efficient designs available in the literature. Here we have compiled some of the reliable architectures in sequential circuits design. From section 3 it is clear that the dominant power dissipation in the sequential circuit is dynamic power dissipation and the major cause of dynamic power dissipation is the charging and discharging of intermediate nodes. We have also discussed that the dissipation is due to the clock input signal. Hence the design objective is to control the unnecessary interference of the clock on the circuit elements.

5.1 Single Edge Triggering

In this design, the output of the flip-flop changes at either rising or falling edge of the clock. This is the basic architecture. Conventional single edge triggered flip-flops are easy to design and works effectively at low frequency but other designing needs to be incorporated for high frequency of operation. A conventional D flip-flop uses transmission gate to pass the input logic. Single edge triggered D flip-flop can also be implemented using MUX. These basic structures suffer delay, power dissipation and silicon area problem. The D flip-flop consist of two latches namely master latch and slave latch connected in series. When clock is low the data is latched by the master and when clock is high the data is transferred to the slave and the output is obtained. This system is slow and it is of initial stage. The waveform of single edge triggered flip flop is shown in figure 5. Here we have taken a positive or rising (single) edge triggered D flip-flop. The rising edge of the clock is shown by the arrow. The input data (D) is fetched in the flip flop and output (Q) changes accordingly.

Table 3 Comparison of Various Design Techniques with Circuit Performance Parameters

Parameters	Single Edge Triggering	Double Edge Triggering	Complementary Pass Transistor Adiabatic Logic	Clock Gating Technique	Power Gating Technique	Near-threshold Voltage Operation
Operating frequency	The operating frequency is **high** and varies from MHz to GHz.	Double edge triggered circuits performs well at **low frequencies.**	They work at **moderate** frequency.	This technique works at **moderate to high** frequency.	Power gated circuit works at **low to moderate** frequency.	These circuits work at **high** frequency.
Delay	Here the delay of **moderate** value.	The circuit delay is **moderate**.	Delay in this technique is **high**.	The circuit delay is **more**.	The circuit delay is **more**.	The delay is of **moderate** order.
Speed of operation	Since they work at high frequency so the operating speed of the circuit is **high**.	Since the circuit respond to both rising and falling edge so the speed of operation **increases**.	These circuit uses pass transistors so the often experience **low** speed of operation.	The speed of operation is **moderate**.	Operating speed is **low**.	Operating speed of the circuit is **high**.
Power dissipation	Power dissipation is **low**.	This dissipates **more** power.	The power dissipation in this technique is **less.**	**Low** power dissipation due to gating technique.	**Low** power dissipation	These circuit dissipates **moderate** level of power.
Area requirement on IC	**Less** area requirement.	**More** area requirement on IC.	**More** area requirement.	**More** area requirement because of gating mechanism.	**More** area requirement.	The area requirement is **less**.
Component description	Single edge triggered circuits are easily implemented using **CMOS**.	**Additional components** are required to make a dual edge triggered circuit.	**Complementary pass transistor** is used and circuit is implemented with **adiabatic logic**.	**Additional circuitry** is required to gate the clock signal from the circuit at the time of inactivity.	**Additional circuitry** is required to gate the power supply from the circuit.	**MOS** are used that are specially designed to work at **near threshold** voltages.
Ease of designing	These circuits are **easy** to design.	Designing level is **Moderate** to achieve.	Adiabatic logic-based circuits are **not easy** to design.	Here the designing is of **moderate** level.	These circuits are **tough** to design.	They are **tough** to design.

5.2 Dual Edge Triggering

As the name implies the flip-flops that are designed using double edge triggering technique can store the data on both the rising and falling edges [6], [7]. Unlike the previous technique this approach is having advantages in terms of speed and power. But the disadvantage is that the additional circuitry is required to make the flip-flop operate at both the transitions of the clock. This cost increase in the chip area. The problem with double edge triggering is that the output suffers glitches at high frequency of operation. Since the data is stored at both the edge transitions it is obvious that the circuit need some sufficient time to latch the data and due to very less time period of the clock signal the data cannot be stored properly and therefore the output seems to be noisy. The waveform of Dual-edge triggered D flip-flop is shown in figure 6. From the waveform it is clear that the flip-flop responds to every rising and falling edge of the clock. In both figure 5 and figure 6 we have assumed that the flip-flop is initially reset i.e. Q is at a low logic level before the first edge of the clock.

5.3 Complementary Pass Transistor Adiabatic Logic

This is a technique where a chain of NMOS transistors are used to implement complementary pass transistor logic for evaluation purpose and also CMOS transmission gates for recovery of energy. With the help of this approach the non-adiabatic loss is eliminated at the output node and makes it an energy efficient design [8]. Logic gates (AND, OR and XOR), multiplexer and flip-flops (D flip-flop, T flip-flop and JK flip-flop) are designed in [9] with this technique but here they used two phase power clock. The circuit implementation using this technique consumes lesser number of transistors which makes it area efficient as well.

5.4 Clock Gating Technique

Clock signal contribute most in the power dissipation. Clock gating is a technique to disable the clock when the circuit is inactive. Additional circuitry is required to produce a gated clock signal from master clock. In VLSI circuits the transistors are connected with the clock and they switch to ON-OFF state based on the clock signal. It is observed that when the output is at a stable logic level the internal nodes get toggle due to the clocking. This is the undesired activity and it also dissipates large power in the circuit. So, the clock gating technique is used to disable the clock signal from the circuit in such situation [10].

5.5 Power Gating Technique

This technique is similar to clock gating. Here the power supply is gated to reduce the unnecessary power dissipation. In section 3 we have discussed that there exists a path from VDD to ground during the signal transition. This causes a short circuit current to

flow and power dissipates in the circuit. Power gating makes the power supply disable from the circuit in such unwanted situation. This halts the power dissipation to some extent. The technique is not very famous because it is not easy to implement the on large complex CMOS circuits [11].

5.6 Near-Threshold Voltage Operation

For highly integrated, low power complex circuit design, the power supply should be as minimum as possible. In Near-threshold voltage operation, the power supply for the circuit is reduced to threshold voltage of the transistor. The operating point here contributes to low power consumption. This approach suffers with the designing challenges. [12]. Table 3 shows a comparative analysis of these techniques in terms of various circuit parameters.

6. CONCLUSION

In this work a detailed explanation about sequential circuits is carried out. The functional blocks of the circuit are explained briefly. The classification of power and delay is done extensively. Further, some designing methods and architectures that are efficient in terms of speed and power dissipation are discussed. As per the studies we have come to a conclusion that **single edge triggered** and **near-threshold voltage** circuits are efficient in terms of delay, power, speed and chip area. This work is done as a study on the sequential circuits. Memory elements are the integral part of computer devices. The future scope of this study would be to implement the digital CMOS circuits with improvement in delay and power consumption.

7. FUTURE SCOPE

According to the study of different circuit designing architectures the single edge triggered circuit performs well in all aspects. However, the power dissipation can be reduced further by using power gating techniques and near-threshold voltage devices. Following are the future aspect of this work:

- Designing of a sequential circuit like counter and enhancing their performance by using above mentioned techniques.
- Reducing the power dissipation by incorporating clock gating technique.
- High frequency digital to analog converters for mobile applications.

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