A MODIFIED 27 LEVEL ARCHITECTURE OF ASYMMETRICAL 3- PHASE MULTILEVEL INVERTER WITH IMPROVED TOTAL HARMONIC DISTORTION

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Abstract : Now a days the growth of interest in multilevel inverters has been increasing because there are enormous applications of there in FACTS and industrial drives etc., Although there are many topologies of multilevel inverters in literature, popular among them are cascaded H-bridge Inverters plays vital role in routine life. Harmonic content of output voltage can be decreased considerably by switching methods. Describes a harmonics reduced in a hybrid cascaded multilevel inverter circuit with new pulse width modulation (PWM) scheme. These scheme pulse width modulations in proposed method are uses reduce switching device. Then to reduced the switching losses and also reduced the harmonics in an inverter circuit. These methods are a combination of a conventional inverter and h bridge inverter. Both inverter are combined a new five level hybrid cascaded multilevel inverter. The multilevel carrier based pulse width modulation methods are used in this topology a Five level output voltage wave forms is shown in FFT window. MATLABE/SIMULINK is used to simulate the inverter circuit operation and control signals.

IndexTerms **- Multilevel inverter, Power Quality, Harmonic reduction, Asymmetrical cascaded multilevel inverter, induction motor, pulse width modulation technique, v/f control method, synchronous speed**

I. INTRODUCTION

Multilevel inverters have been under research and development for more than three decades and have found successful industrial applications. However, this is still a technology under development, and many new contributions and new commercial topologies have been reported in the last few years. The aim of this dissertation is to group and review recent contributions, in order to establish the current state of the art and trends of the technology to provide readers with a comprehensive and insightful review of where multilevel converter technology stands and is heading. This chapter first presents a brief overview of well-established multilevel inverters strongly oriented to their current state in industrial applications and then centers the discussion on the new multilevel inverters that have made their way into the industry. Multilevel inverters have been attracting increasing interest recently the main reasons are; increased power ratings, improved harmonic performance, and reduced electromagnetic interference (EMI) emission that can be archived with multiple dc levels that are synthesis of the output voltage waveform. In particular multilevel inverters have abundant demand in applications such as medium voltage industrial drives, electric vehicles, and grid connected photovoltaic systems. The present work provides a solution to design an efficient multilevel topology which is suited for medium and high power applications. In the subsequent sections the research background is discussed in detailed. Motivation and objectives are clearly outlined.

1.1 Medium and High Power Inverters

There are different power converter topologies and control strategies used in inverter designs. Different design approaches address various issues that may be more or less important depending on the way that the converter is intended to be used. The issue of waveform quality is one the important concern and it can be addressed in many ways. In practice capacitors and inductors can be used to filter the waveform [1-2]. If the design includes a transformer, filtering can be applied to the primary or the secondary side of the transformer or to both sides. Low-pass filters are applied to allow the fundamental component of the waveform to pass to the output while limiting the passage of the harmonic components. Thus quality of waveform can be adjusted. Note that, normal inverters always generate very low quality output waveforms. To make the output waveform qualitative, low pass (LC filter) are often added in the circuit. Thus, at this point of time readers might have a question that, why the quality of converter output is low? And why Low pass filter are frequently added in the circuit. Further, what kinds of solutions are available to increase quality of output waveform without losing its efficiency? All this are open problems associated with present day inverters. However, eventually all this will be addressed in this thesis. But at first we try to figure out the converter applications from low power to high power and then we summarize the requirements to meet the high power demand. Finally we try to present the problems and solutions available to meet the high power demand.

1.2 Challenging Aspects in Medium and High Power Inverters

The current energy arena is changing. The feeling of dependence on fossil fuels and the progressive increase of its cost is leading to the investment of huge amounts of resources, economical and human, to develop new cheaper and cleaner energy resources not related to fossil fuels [3]. In fact, for decades, renewable energy resources have been the focus for researchers, and different families of power inverters have been designed to make the integration of these types of systems into the distribution grid a current reality. Besides, in the transmission lines, high-power electronic systems are needed to assure the power distribution and the energy quality. Therefore, power electronic inverters have the responsibility to carry out these tasks with high efficiency. The increase of the world energy demand has entailed the appearance of new power converter topologies and new semiconductor technology capable to drive all needed power. A continuous race to develop higher-voltage and higher-

current power semiconductors to drive high-power systems still goes on. However, at present there is tough competition between the use of classic power converter topologies using high-voltage semiconductors and new converter topologies using medium-voltage devices. Power inverters are an amazing technology for industrial practice powered by electric drive systems. They are potentially helpful for a wide range of applications: transport (train traction, ship propulsion, and automotive applications), energy conversion, manufacturing, mining, and petrochemical, to name a few. Many of these processes have been continuously raising their demand of power to reach *higher production rates*, *cost reduction* (large-scale economy), and *efficiency* [4].

The power electronics research community and industry have reacted to this demand in two different ways: developing semiconductor technology to reach higher nominal voltages and currents (currently 8 kV and 6 kA) while maintaining traditional converter topologies (mainly two-level voltage and current source inverters); and by developing new converter topologies, with traditional semiconductor technology, known as *multilevel inverters* [5]. The first approach inherited the benefit of well-known circuit structures and control methods. Adding to that, the newer semi-conductors are more expensive, and by going higher in power, other power-quality requirements have to be fulfilled, thereby there may be need of additional power filters. Therefore it will be quite feasible to choose to build a new converter topology based on multilevel concept. This is the challenging issue right now.

1.3 Concept of Classical Inverters (Two-Level Inverters)

At present there is tough competition between the use of classic power converter topologies using high-voltage semiconductors and new converter topologies using medium-voltage devices. This idea is shown in Fig.1.1, where inverters are built by adding devices in series. In past, these inverters are only viable options for medium and high-power applications. But in present scenario, multilevel technology with medium voltage semiconductors are fighting in a development race with classic power inverters using high-power semiconductors, which are under continuous development and are not mature. Although, classical inverters are good for low power applications, but they fail to fill the requirements of high-power levels.In view of later, to retrieve the demerits of classical inverters we should know about the multilevel technology and the merits it offer. Multilevel inverters are a good alternative for power applications due to the fact that, they can achieve high power using mature medium-power semiconductor technology. Practically, multilevel inverters present great advantages compared with conventional and very well-known two-level converter. These advantages are fundamentally focused on improvements in the output signal quality (Voltage & Current) and a nominal power increase in the converter [6].

These properties make multilevel inverters very attractive to the industry and, nowadays, researchers all over the world are spending great efforts trying to improve multilevel converter performances such as the control simplification and the performance of different optimization algorithms in order to enhance the THD [7] of the output signals, the balancing of the dc capacitor voltage [8], and the ripple of the currents. For instance, nowadays researchers are focused on the harmonic elimination using pre-calculated switching functions, harmonic mitigation to fulfill specific grid codes, the development of *new multilevel converter* topologies (hybrid or new ones), and new control strategies [9]. However, before introducing about the multilevel inverters, let's make an overview about the classical inverters and their problems. To address the problems of conventional inverters, one should have an idea about the Medium to high-power range inverters and related challenging issues. Below are some of the facts summarized.

II. LITERATURE SURVEY

Asymmetrical Multilevel Inverter for Higher Output Voltage Levels (2015)

Now a day the growth of interest in construction inverters has been increasing because there are monumental applications of there in FACTS and industrial drives etc., though there are several topologies of structure inverters in literature, in style among them are cascaded H-bridge. Generally the management ways of those cascaded inverters are designed an assumption of getting all dc supply voltages same for all H-bridges. This paper discusses the skills of cascaded structure electrical converter to supply additional output voltage levels with same variety of H-bridges, however with completely different input voltage ratios. the best nature of input dc voltage sources is shown as a bonus in this paper. The planned inverter is then used to feed an induction motor drive and also the simulation results are shown The simulation results show that in this paper 3- section 23-level and 27-level asymmetrical cascaded H-bridge electrical converter are studied. The output voltage of three section Asymmetrical 23-level CHB offers 23.51 % THD, whereas 27-level asymmetrical CHB provides twelve.56% Th.D. while not PWM technique. Therefore compared to 23-level CHB, a 27-level unequal DE voltage quantitative relation consists of minute range of harmonics and increased output voltage quality. Finally the projected system is connected to induction motor for future industrial and automotive applications and therefore the simulation results are shown. [01]

Charge Balance Control Methods for a Class of Fundamental Frequency Modulated AsymmetricCascaded Multilevel Inverters (2007)

Modulation methods for structure inverters have generally centered on synthesizing a desired set of curved voltage waveforms using a mounted variety of dc voltage sources. This makes the common power drawn from totally different dc voltage sources unequal and time varied. Therefore, the dc voltage sources are unregulated and need that corrective management action be incorporated. in this paper, first two new choices are planned for deciding the dc voltage sources values for uneven cascaded structure inverters. Then two modulation ways are planned for the dc power leveling of those kinds of structure inverters. Using the charge balance management ways, the ability drawn from all of the dc supply are balanced aside from the dc source used in the primary H-bridge. The planned management ways are valid by simulation and experimental results on a single-phase 21-level inverter. In this paper, two new choices for the determination of the values of the dc voltage sources for uneven cascaded structure inverters are planned. Additionally, two modulation ways are planned for dc power balance realization for the planned uneven structure inverters. These modulation methods can increase the lifespan of the dc sources. Additionally, the quantity of charging and substitution times of the dc sources is small, which may result in a discount of the electrical converter maintenance prices. For structure inverters with An H-bridge cell, all of the dc voltage supply apart from the dc voltage source used in the first H-bridge become equally discharged and balanced over (N-1) cycles as a result of using the two charge

balance management ways. Simulations and experimental results on a 21-level electrical converter image verify the theoretical analyses. [03]

III. PROPOSED WORK

In case of 23 and 27 level Asymmetric Cascaded MLI three DC sources are used having 2 same and third different and 12 power switches are used. The Asymmetric Multilevel Inverter increases the number of levels in the output and reduces the number of input DC sources required. IGBT is used as semiconductor switch for designing the inverter circuit.

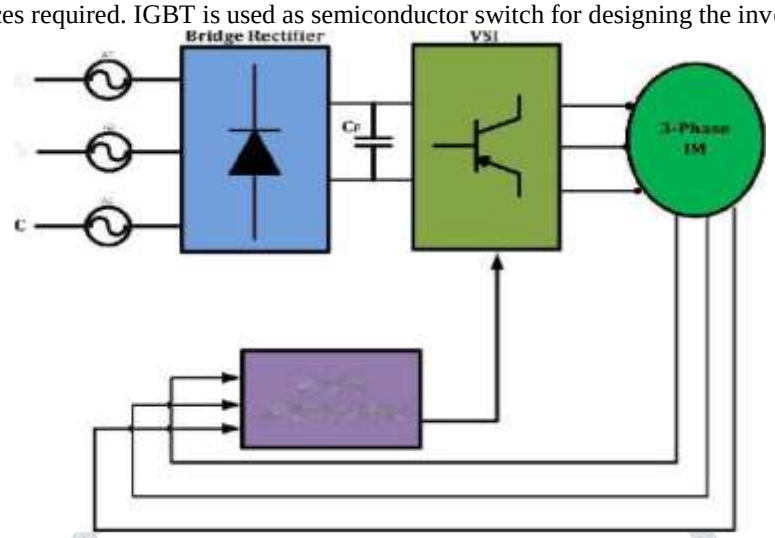

Figure 1: Proposed block diagram of 9-levels Hybrid Cascaded Multilevel Inverter

It has the high power rating, less conduction loss and less switching loss. These topology uses level-shifted multi carrier based new PWM method, used to produce a 27-level output voltage.

The Simulink model of 9-level multilevel inverter implemented in Matlab-Simulink is shown in Figure 2. It is basically a Cascaded H-bridge type of Multilevel Inverter.

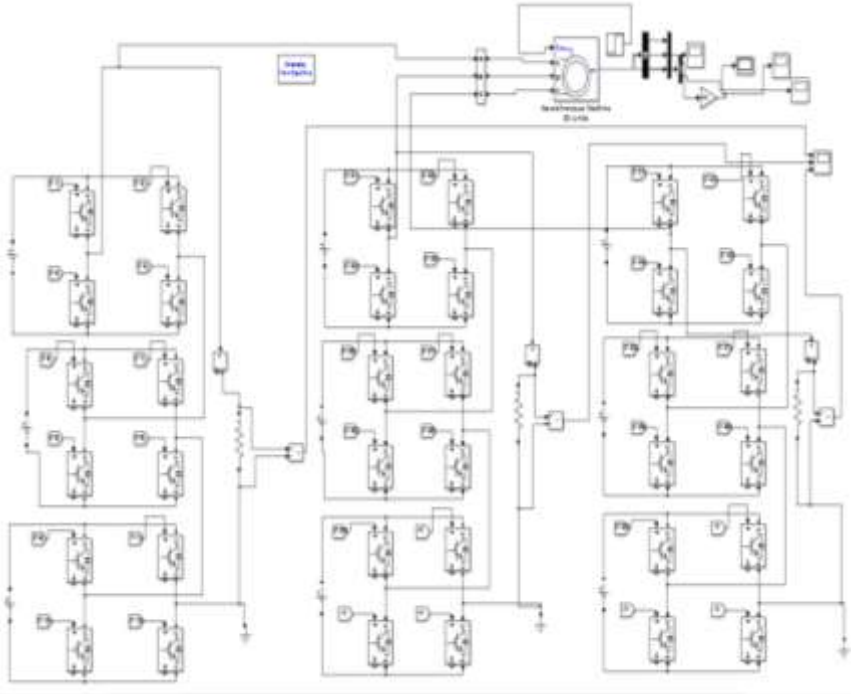

Figure 2: Simulink model of 23 and 27 Level with IM

Here the used DC source is Asymmetrical type, Asymmetrical source defines that it has different value of DC sources used in an Inverter. For 27-level inverter the DC sources are 100V, 200V, and 100V respectively. The Simulink model for 27-level multilevel inverter shown in figure 2.

3.1. Working and Analysis (23 Level)

Working of this inverter is nothing but how we make power switches (IGBTs) ON and OFF as per voltage level desired. We have generated switching pulses to obtain staircase output voltage which resembles nearly equal to sine wave. For different switching angles the power circuit behaves differently producing different waveforms. In this topology, we have generated 9 voltage levels as 1Vdc, $2V_{dc}$, $3V_{dc}$, $4V_{dc}$, $5V_{dc}$, $6V_{dc}$, $7V_{dc}$, $8V_{dc}$, $9V_{dc}$, $10V_{dc}$ and $11V_{dc}$.The circuit working for each level is described below:

A. For $V1_{dc}$ voltage level

Since S1, S3, S7, S8, S9 and S10 are ON or all power switches are OFF, the current will cancelled out in the bridge and hence it gives V1 voltage level.

B. For 2V_{dc} voltage level

Since S3, S4, S5, S7, S9 and S10 are ON and remaining switches are OFF, the voltage across load will gives V2 level.

C. For 3V_{dc}voltage level

Since S1, S2, S5, S6, S10 S11& S12 are ON and remaining switches are OFF, the voltage across load will gives 200V level.

D. For 4V_{dc}voltage level

Since S1, S2, S5, S7, S9 & S11 are ON and remaining switches are OFF, the voltage across load will gives 300V level.

E. For 5V_{dc} voltage level

Since S1, S3, S5, S6, S9 & S11 are ON and remaining switches are OFF, the voltage across load will gives 400V level.

F. For 6V_{dc} voltage level

Since S1, S3, S5, S7, S9 & S10 are ON and remaining switches are OFF, the voltage across load will gives 400V level.

G. For 7V_{dc} voltage level

Since S3, S4, S5, S6, S9 & S10 are ON and remaining switches are OFF, the voltage across load will gives 400V level.

H. For 8V_{dc} voltage level

Since S1, S2, S5, S7, S9 & S11 are ON and remaining switches are OFF, the voltage across load will gives 400V level.

I. For 9V_{dc} voltage level

Since S1, S2, S5, S7, S9 & S10 are ON and remaining switches are OFF, the voltage across load will gives 400V level.

J. For 10V_{dc} voltage level

Since S1, S3, S5, S6, S9 & S10 are ON and remaining switches are OFF, the voltage across load will gives 400V level.

K. For 11V_{dc} voltage level

Since S1, S2, S5, S6, S9 & S10 are ON and remaining switches are OFF, the voltage across load will gives 400V level.

L. For 0V_{dc} voltage level

Since S1, S5, S7, S9, S11 and S3 are ON or all power switches are OFF, the current will cancelled out in the bridge and hence it gives 0 V voltage level.

M. For -1V_{dc}Voltage level

Since S1, S3, S5, S6, S11, and S12 are ON and remaining switches are OFF, the voltages across load will gives -100V level.

N. For -2V_{dc}Voltage level

Since S1, S2, S5, S7, S11 and S12are ON and remaining switches are OFF, the voltage across load will gives -200V level.

O. For- 3V_{dc}Voltage level

Since S3, S4, S7, S8, S9 and S10 are ON and remaining switches are OFF, the voltages across load will gives -300V level. I. For- 300V voltage level.

P. For -4V_{dc} Voltage level

Since S3, S4, S5, S7, S9 and S11 are ON and remaining switches are OFF, the voltages across load will gives -400V level.

Q. For -5V voltage level

Since S1, S3, S7, S8, S9 and S11 are ON and remaining switches are OFF, the voltage across load will gives 400V level.

R. For -6V_{dc} voltage level

Since S1, S3, S5, S7, S11 and S12 are ON and remaining switches are OFF, the voltage across load will gives 400V level.

S. For -7V_{dc} voltage level

Since S1, S2, S7, S8, S11 and S12 are ON and remaining switches are OFF, the voltage across load will gives 400V level.

T. For -8V_{dc} voltage level

Since S3, S4, S5, S7, S8, S9 and S11 are ON and remaining switches are OFF, the voltage across load will gives 400V level.

U. For -9V_{dc} voltage level

Since S3, S4, S5, S7, S11 and S12 are ON and remaining switches are OFF, the voltage across load will gives 400V level.

V. For -10V_{dc} voltage level

Since S1, S3, S5, S7, S8, S11 and S12 are ON and remaining switches are OFF, the voltage across load will gives 400V level.

W. For -11V_{dc} voltage level

Since S3, S4, S5, S7, S8, S11 and S12 are ON and remaining switches are OFF, the voltage across load will gives 400V level.

For detail operation of new topology can also be understand by analyzing table 4.2 which is given below. Here 0 means switches are OFF and 1 means switches are ON.

Table 1: System parameters for 23-level Inverter

System Parameters	Value
Reference frequency	50 Hz
Carrier frequency	1.2K Hz
Load resistance	1Ω
Load inductance	1 mH
DC Sources	400V, 500V, 600V

Table 2 Switches operation

V./ S	Switches											
	S1	S2	S3	S4	S5	S6	S7	S8	S9	S 10	S11	S12
V_{dc}	1	1	0	0	0	1	0	1	0	1	0	1
$2V_{dc}$	0	0	1	1	1	1	0	0	0	1	0	1
$3V_{dc}$	0	1	0	1	1	1	0	0	0	1	0	1
$4V_{dc}$	1	1	0	0	1	1	0	0	0	1	0	1
$5V_{dc}$	0	0	1	1	0	0	1	1	1	1	0	0
$6V_{dc}$	0	1	0	1	0	0	1	1	1	1	0	0
$7V_{dc}$	1	1	0	0	0	0	1	1	1	1	0	0
$8V_{dc}$	0	0	1	1	0	1	0	1	1	1	0	0
$9V_{dc}$	0	1	0	1	0	1	0	1	1	1	0	0
$10V_{dc}$	1	1	0	0	0	1	0	1	1	1	0	0
$11V_{dc}$	0	1	0	1	1	1	0	0	1	1	0	0
$12V_{dc}$	0	0	1	1	1	1	0	0	1	1	0	0
$13V_{dc}$	1	1	0	0	1	1	0	0	1	1	0	0
$0V_{dc}$	0	1	0	1	0	1	0	1	0	1	0	1
V_{dc}	0	0	1	1	0	1	0	1	0	1	0	1
$2V_{dc}$	1	1	0	0	0	0	1	1	0	1	0	1
$3V_{dc}$	0	1	0	1	0	0	1	1	0	1	0	1
$4V_{dc}$	0	0	1	1	0	0	1	1	0	0	1	1
$5V_{dc}$	1	1	0	0	1	1	0	0	0	0	1	1
$6V_{dc}$	0	1	0	1	1	1	0	0	0	0	1	1
$7V_{dc}$	0	0	1	1	1	1	0	0	0	0	1	1
$8V_{dc}$	1	1	0	0	0	1	0	1	0	0	1	1
$9V_{dc}$	0	1	0	1	0	1	0	1	0	0	1	1
$10V_{dc}$	0	0	1	1	0	1	0	1	0	0	1	1
$11V_{dc}$	1	1	0	0	0	0	1	1	0	0	1	1
$12V_{dc}$	0	1	0	1	0	0	1	1	0	0	1	1
$13V_{dc}$	0	0	1	1	0	0	1	1	0	0	1	1

IV. RESULTS AND DISCUSSION

This paper shows the comparative study of output voltage of 23 and 27-level asymmetrical cascaded multilevel inverters cascaded is compared for the APOD techniques, and it also shows the THD profile and performance of the circuit with IM for PWM techniques, and also the compare all result with 23-level MLI.

Cascaded multi-level inverter shows the lowest THD profile without any type of filter and also any type of dependency of inductor and capacitor used for smooth the current wave form and due to less number of switching devices gate firing circuit also reduced that's why total cost and performance has been increased .

4.1 SIMULATION RESULT OF (23-LEVEL) ACMLI WITH IM USING APOD CHB

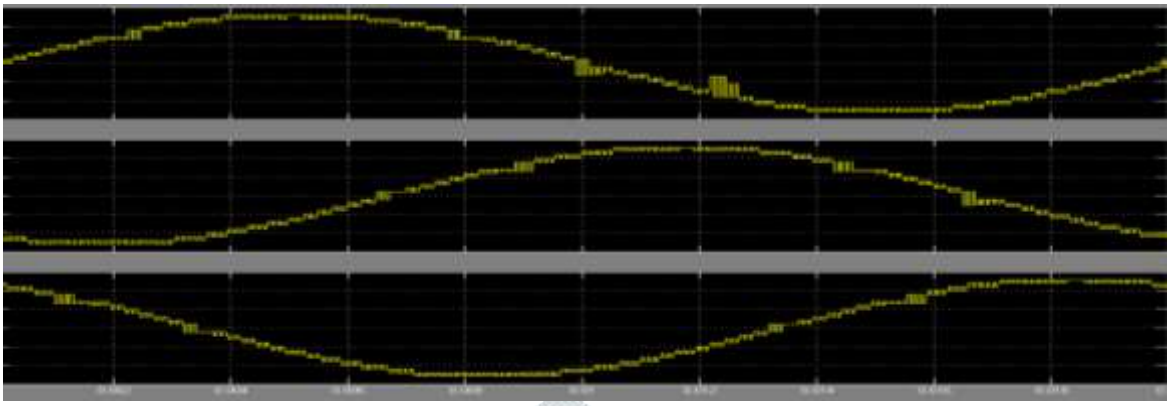

Figure 3: Output phase voltage waveform for asymmetric (9-level) MLI using APOD-HCB

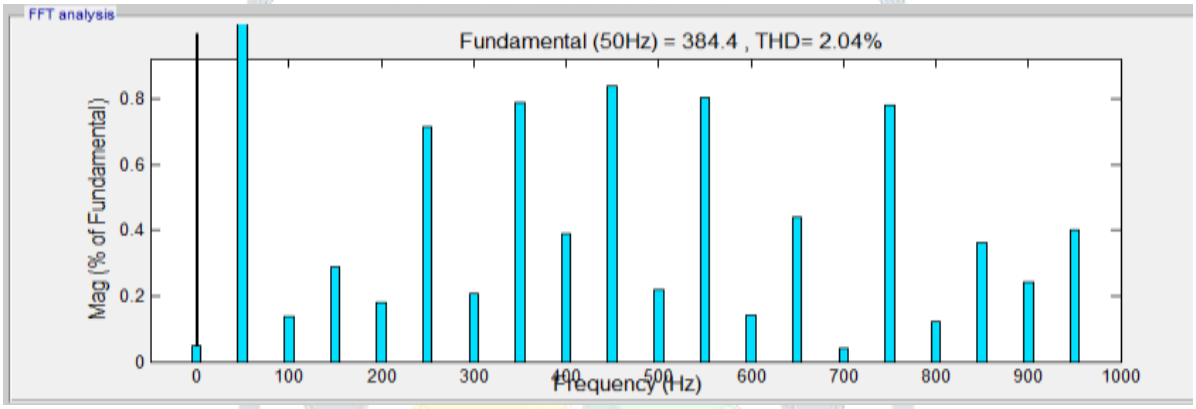

Figure 4: FFT analysis of voltage waveform of asymmetric (9-level) cascaded MLI using IPD-CLSPWM

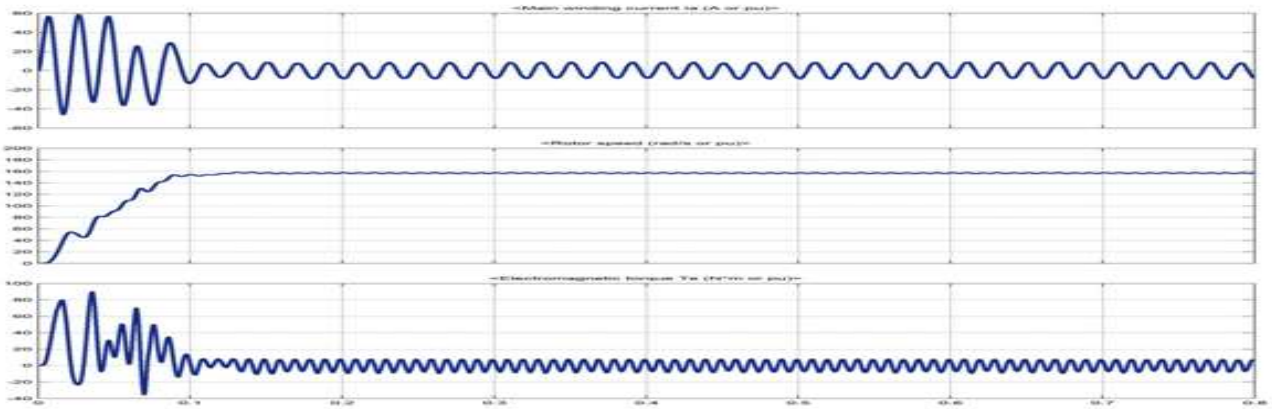

Figure 5: Motor output of (9-level) cascaded MLI using IPD-CLSPWM

4.2 . SIMULATION RESULT OF (27-LEVEL) ACMLI WITH IM USING APOD- CHB

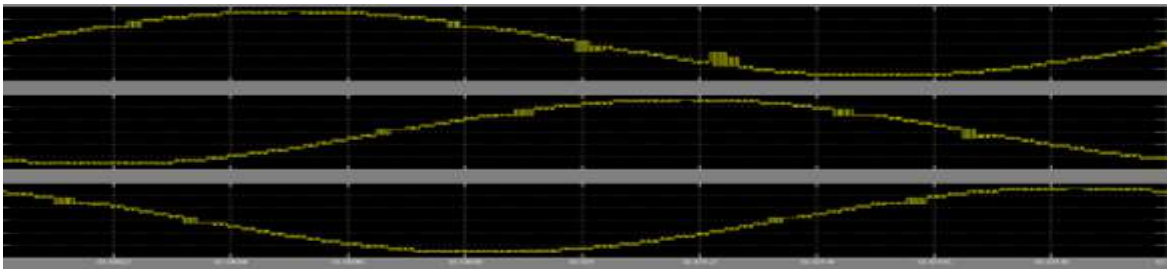

Figure 6: Output phase voltage waveform for asymmetric (27-level) MLI using APOD-CHB

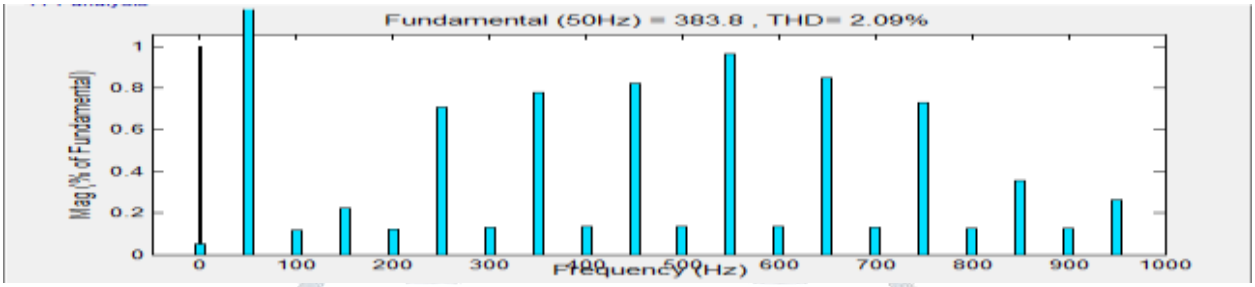

Figure 7: FFT analysis of voltage waveform of asymmetric (27-level) cascaded MLI using APOD-CHB

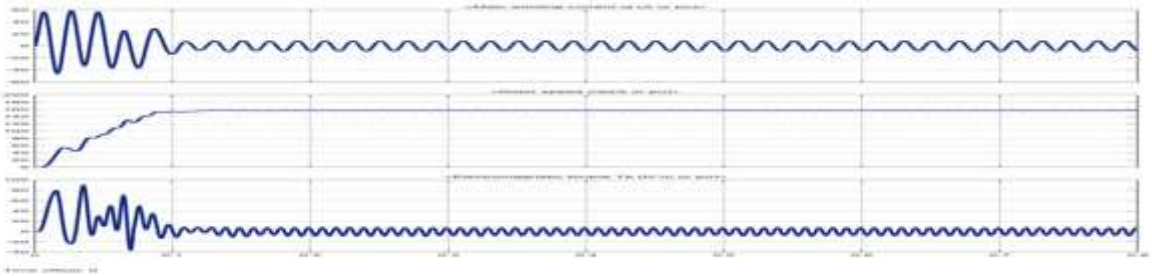

Figure 8: Motor output of (27-level) cascaded MLI using APOD-CHB

TABLE 5.1: The THD of the output voltage of 23-level MLI with IM Compared for APOD

System Parameters	APOD
THD (%)	2.09%
Speed of motor (N_r)	159 rad/sec

TABLE 5.2: Comparison of the THD of output voltage between 23- level ACHB and 27-level MLI

	23-LEVEL	27-LEVEL
Switching techniques	APOD	APOD
Voltage THD%	10.59%	2.09%

V. CONCLUSION

In this work, the multicarrier pulse width modulation (PWM) techniques for9-level have been presented. Performance factor like total harmonic distortion (THD) of the output voltage of asymmetric cascade H-Bridge multi-level inverter (CHB) have been evaluated, presented and analyzed. The total harmonic distortion (THD) of the output voltage of unbalanced cascade multi-level inverter (CMLI) is studied under different techniques such as APOD, compare for 23 and 27 level multi-level inverter (MLI) and less total harmonic distortion (THD) is observed for APOD techniques for 23-level and APOD techniques better for 27-level multi-level inverter (MLI). Therefore, it concluded that the 27-level cascade multi-level inverter (CHB MLI) provide a lower percentage total harmonic distortion (THD) as compared to 23-level multi-level inverter (MLI). The harmonic distortions present in the output voltage waveforms were experiential and calculate from side to side Fast Fourier Transform (FFT) analysis tool in Matlab and Simulink.

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