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VLSI Implementation of High Performance Approximate Multipliers for FPGA Application

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Abstract : It is possible to use a variety of computer arithmetic systems to carry out a complex multiplier. The efficiency of an FPGA-VLSI processor relies on how quickly its digital signal processing operations can be carried out. In order to achieve both high accuracy and speed, the authors of this work offer a concept for a 64-bit approximation multiplier technique that utilises compressors and partial product multipliers. For artificial intelligence (AI) based FPGA-VLSI applications, approximate multipliers are among the fastest multipliers available. The suggested study reveals a 64-bit approximation to a 64-bit multiplication. To implementation of the proposed 64 bit digital approximate multiplier, we are using the partial product or dada based multiplication technique; in which the 64 bit multiplication process complete in the partial form. 64 bit split into the 32, 16, 8, 4 and 2 bit multiplication. We are considering performance parameters in terms of the area, latency and PDP. The area is reducing upto 55%, latency and PDP is reducing approx upto 70% then existing work. Proposed multiplier gives 99% accuracy. The FPGA integrated circuit utilised for the simulation is a member of the virtex 7 family.

Index Terms **– Partial product, VLSI, Xilinx, FPGA, Approximate, Digital, Multiplier, Area, Latency, Power.**

I. INTRODUCTION

Important parts of modern circuits that increase the processing speed of processors are those that perform arithmetic operations such as multiplication, addition, and subtraction. Anyhow, the processor's multiplier unit is crucial to its speed. As a result, this boosts the appeal of fast multiplier design for use in ALU and other high-performance signal processors. In the last couple of decades, researchers have introduced a few novel multiplier engineering developments. Both Booth's multiplier and the modified version of it are well-known in modern VLSI design, although they both come with their own set of drawbacks. To get to the final response, this multiplier has to take a few intermediate stages, which slows down the processing time. These intermediate procedures include a few iterative operations, such as inspection and subtraction, which reduce processor performance exponentially with increasing bit counts in the multiplier and multiplicand. Since the development of fast processors is now a top priority, new technologies that can outpace the multiplier in question must be introduced. One more engineering method reliant on an approximate multiplier is explored in order to overcome the drawback of the conventional multiplier booth's multiplier and the modified multiplier booth's multiplier.

Error-tolerant applications like media signal preparation and data mining mean that precise processing units are not always necessary. They may be replaced with close equivalents. The study of approximation computing as a means to create error-tolerant software is on the rise. The fundamental components of these programmes are organised by adders and multipliers. Advanced sign preparation applications benefit from the suggested transistor-level implementation of approximation complete adders. Multipliers that use midway products may benefit from their suggested complete adders.

The development of approximate computing as a solution to the design of energy-efficient advanced frameworks is a relatively recent phenomenon. Mixture of media, acknowledgement, and information mining are all examples of applications that may function with less than perfect accuracy in calculations because of their inherent robustness to mistake. In such contexts, approximation circuits may play an important role as a potential choice for reducing space, power, and delay in sophisticated frameworks that can tolerate some loss of exactness, hence achieving higher performance in vitality efficiency.

Approximate Rather of relying on a guaranteed accurate result, applications may use approximation computing, a computation technique that recovers a possibly erroneous result.

Since approximation fundamental data (like control activities) might lead to undesirable outcomes like programme crash or incorrect yield, presenting estimates in non-basic data is a crucial need of approximate computing.

II. PROPOSED METHODOLOGY

The proposed study aims to provide a 64-bit approximation multiplier with high throughput and low latency for cutting-edge DSP applications. Prior to this, it is built for both 16-bit and 32-bit use in a wide range of programmes.

Proposed work is as followings-

- One of the goals is to create an approximate 64-bit by 64-bit multiplier.
- To implement using verilog code on the Xilinx platform.
- To determine the values of many factors, including area, power, delay, and power delay product (PDP).

- Evaluate the precision of the new multiplier against the previous approximation.

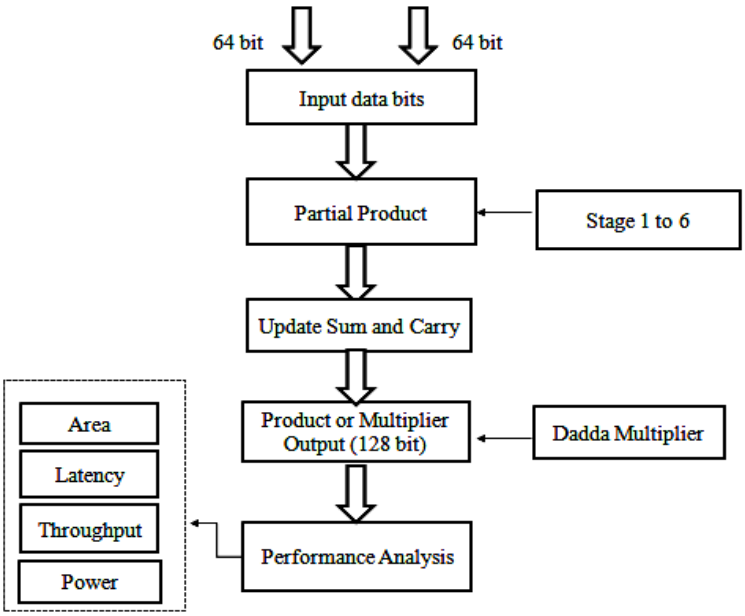

Figure 1: Flow Chart

The suggested flowchart is shown in figure 1. This process diagram makes it evident which modules contribute to the development and operation of the proposed approximation multiplier.

It simulates and displays the results of the following operations:

- Carry Save Adder
- Dadda or Partial product Multiplier
- Full Adder
- Half Adder

III. Simulation and Result

The suggested 64-bit approximation multiplier is realised in Xilinx 14.7 version utilising verilog language. The results of the test bench are validated and simulated using the Isim simulator. The suggested technique was developed using a behavioural modelling approach. The Artix and vertex Family has a lot of experience with actualization. This experimental setup results is based on the virtex 7 FPGA IC.

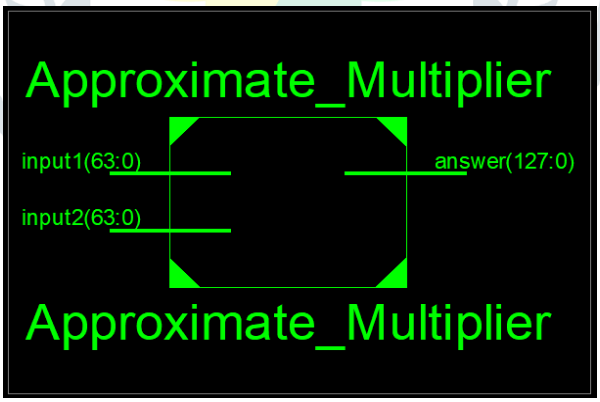

Figure 2: Top level View

Figure 2 provides a high-level illustration of the proposed 64-bit approximation multiplier. Input 'a' is 64 bits, whereas 'b' is 24 bits. This multiplier will provide 128-bit results for the 'c' output. The bit that is produced by a digital multiplier is the sum of the bits that went into creating the multiplier.

Binary Number Input-1 [64-bit]

Input (a) =

1010111111000011010101010111110000111100001111000011111111111110

Input (b) =

110101111111110000001111100000111111100000011111100000011111100

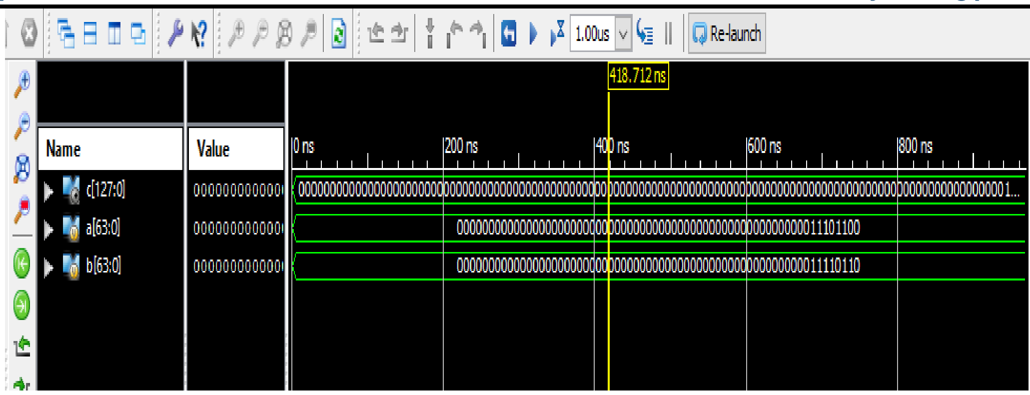

Figure 3: Result validation in Test Bench-1

Right now, we use the Isim simulator to accomplish our modelling and simulation. The window of a test bench is seen in Figure 3. In this case, we have a 128-bit output (c) and 64-bit inputs (a, b). Both a and b's values have been established. Multiplying a and b now yields c as an output.

Output (c) =

0111000101100100001001010001001010000110111011101010001010001100111100100000000000000000000000000000000
0000000000000000000000000

Hexadecimal Number Input-2

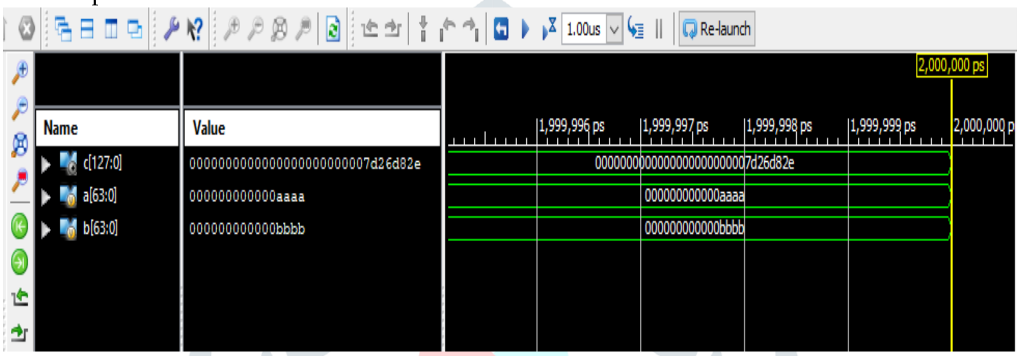

Figure 4: Result validation in Test Bench-2

In this case, we have two 64-bit hexadecimal inputs (a and b) and a 128-bit hexadecimal output (c). In this case, the value of 'a' is aaaa while the value of 'b' is bbbb. Multiplying a and b yields c as an output. Therefore, c equals 7D26D82E.

Table 1: Result Comparison

Sr No.	Parameter	Previous Work [1]	Proposed Work
1	Multiplier Size	16X16	64X64
2	Area [LUTs]	206	95
3	Latency [ns]	4.721	1.376
4	PDP [pJ]	29.627	9.35 pJ

In contrast to earlier work, the proposed multiplier is designed for 64-bit approximation multiplication. Based on these estimated values, it is safe to state that the proposed 64-bit multiplier is an improvement over its predecessor.

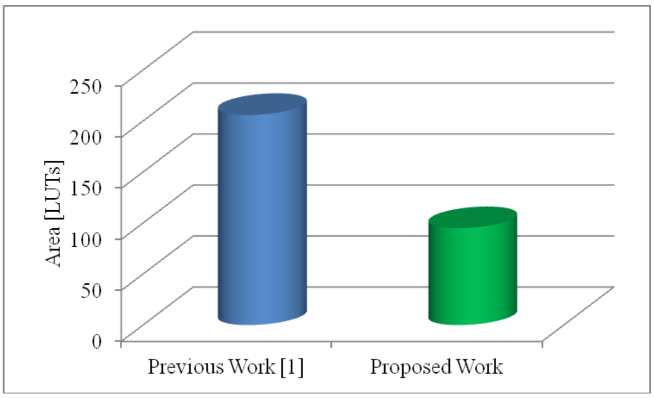

Figure 5: Comparasion of LUTs

Figure 5 represents the comparison of the look up table of the previous and proposed work. The proposed multiplier consume less no of look up table then exisitng.

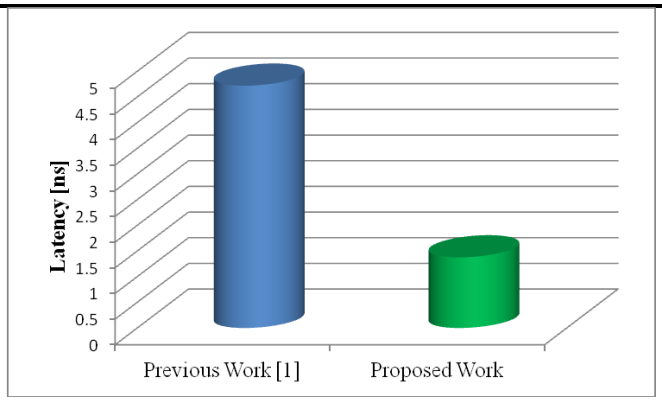

Figure 6: Comparasion of Latency

Figure 6 represents the comparison of the latency of the previous and proposed work. The proposed multiplier consume less time delay or latency then exisitng

IV. Conclusion

The suggested study reveals a 64-bit approximation to a 64-bit multiplicator. The FPGA IC from the Virtex 7 series is utilised to simulate the outcomes. The suggested approximation multiplier is optimised for 64-bit by 64-bit multiplication, whereas its predecessor was optimised for 16-bit by 16-bit multiplication. The optimized area in terms of LUTs is 206 for the existing work and 95 for the proposed work. The value of latency or delay is 4.721ns in the previous and 1.376ns for the proposed. The calculated PDP value is 29.627pJ for the existing and 9.35pJ for the proposed work. Previous work shows the unsigned and signed accurate architecture provides up to 25% and 53% reduction in LUT utilization, respectively, for different sizes of multipliers. Moreover, with unsigned approximate multiplier architectures, a reduction of up to 51% in the critical path delay can be achieved with an insignificant loss in output accuracy. The proposed multiplier utilizes reduced area upto 55%, logic delay or latency is reduced upto 70% and PDP is also reduced upto 70%. Therefore the proposed multiplier gives better performance than existing multiplier.

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