Design and Development of 21 level Multilevel Inverter with reduced switches for Renewable Energy Applications

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Abstract : Lately, a multilevel inverter takes an important role for medium voltage and high voltage-power applications. It has many advantages like minimum switching loss, more dv/dt stress, very low THD. But it has also drawbacks like for higher level required more switching devices, large size, more cost. This paper mainly proposed a newly invented topology with a reduced switches belongs to only eight switches, four voltage sources, and two power diodes to produce 21 level voltage waveforms. The major advantage of this proposed inverter ends in small size, lesser loss, along with low installation cost, and it is suitable for high voltage power applications. The simulation results for different switching angle calculation methods especially Equal Phase (EP) method and Half Height (HH) method are analyzed and presented. This proposed topology composes 8 switches, 4 power diodes and 4 voltage sources of different values. The outcomes of this proposed inverter topology results in small size, lesser loss, and very low installation cost. Besides, THD in the output waveform of the proposed inverter is low The proposed inverter has been simulated through MATLAB software.

Keywords— Multilevel inverter; Total Harmonic Distortion (THD); Equal Phase (EP) method; Half Height (HH) method

I. INTRODUCTION

A multilevel inverter is a device which consists of multiple voltages and power switches, which forms a unique structure to provide high voltages with low harmonics excluding of transformers or series connected synchronized switching devices. It has many advantages like minimum switching loss, more dv/dt stress, very low THD. But it has also drawbacks like for higher level required more switching devices, large size, more cost. This paper mainly proposed a newly invented topology with a reduced switches belongs to only eight switches, four voltage sources, and two power diodes to produce 21 level voltage waveforms. The major advantage of this proposed inverter ends in small size, lesser loss, along with low installation cost, and it is suitable for high voltage power applications. The conventional 2 level inverter provides more switching losses, EMI and high dv/dt stress, high level of THD in high power and medium voltage applications [1]. Due to these difficulties, the multilevel inverter was proposed in 1975 [2]. The term multilevel was initiated with the 3 level inverter and now it has been promoted to N number of levels. Multilevel inverter is mainly constructed with three different structures. They are (a) Flying capacitors (b) Diode clamped and (c) Cascaded H-bridges converter with separate dc sources [3]. THD predominantly depends on the degree of the level of the inverter and controlling technique of the switching devices. By efficient control scheme and by increasing the level of the output waveform of the inverter, THD can be minimized. But for conventional topology, the inverter

turns into higher shape and complex structure [4]. For the time being, reduced switches multilevel inverter is suggested for solving the problem of conventional topologies. In "Ref. [5]", a reduced switch multilevel inverter is invented. It utilizes 13 switches and 6 DC sources of different values to achieve 21 level output waveform. However, it still uses a higher amount of switching components.

In "Ref. [6]" a novel multilevel inverter is suggested which utilizes 12 switches and 4 DC sources. Hereafter, it uses less switching components than "Ref. [5]". In "Ref. [7]", another multilevel inverter is proposed comprised of 11 switches, 4 DC sources of different values and 3 power diodes for generating twenty-one level output. So, it uses less switching components than "Ref. [6]", and "Ref. [5]".

This proposed topology composes 8 switches, 4 power diodes and 4 voltage sources of different values. The outcomes of this proposed inverter topology results in small size, lesser loss, and very low installation cost. Besides, THD in the output waveform of the proposed inverter is low. Therefore, it is suitable for medium voltage and high-power applications. Switching angles of a multilevel inverter are conducted by following methods [8-9],

- Newton-Raphson Method.
- Equal Phase (EP) Method.
- Half Equal Phase (HEP) Method.
- Half Height (HH) Method.
- Feed Forward (FF) Method.

In this paper switching angles of the proposed inverter have been calculated by using Equal phase method and Half Height method. Finally, these two topologies have been compared for proposed topology. Corresponding work has been embodied as follows, Section II describes proposed inverter topology, Section III describes the comparison of proposed topology with existing topologies, Section IV shows the calculation of switching angles, Section V shows the simulation results and finally, the article ends with conclusions and references.

II. PROPOSED INVERTER TOPOLOGY

Fig. 1 shows the circuit diagram of the proposed 21 level inverter. 8 switches, 4 DC sources, and 8 power-diodes are used in it. The working principle of this inverter can be easily described with the help of TABLE I.
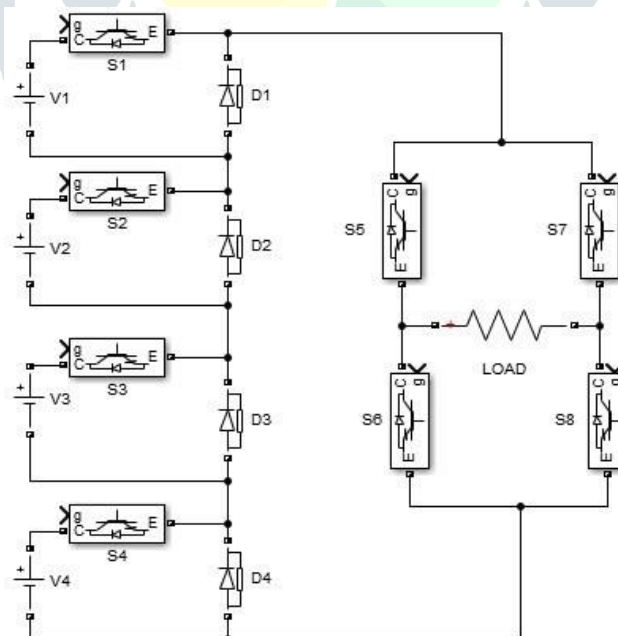

Fig. 1 Proposed Twenty-one level inverter topology

- Mode 1: In this mode, when switches S1, S2, S3, S4, S5, S6, S7, S8, are turned "off", the output voltage will be '0'.

- Mode 2: When switches S1, S5, S8, are turned "on", the output voltage across the load will be 'V1'.

- Mode 3: When switches S2, S5, S8, are turned "on", the output voltage will be 'V2'.

- Mode 4: When switches S3, S5, S8, are turned "on", the output voltage will be 'V3'.

- Mode 5: when switches S4, S5, S8, are turned "on", the output voltage across the load will be 'V4'.

- Mode 6: When switches S1, S4, S5, S8, are turned "on", the output voltage will be 'V1+V4'.

- Mode 7: When switches S2, S4, S5, S8, are turned "on", the output voltage will be 'V2+V4'.

- Mode 8: When switches S3, S4, S5, S8, are turned "on", the output voltage will be 'V3+V4'.

- Mode 9: When switches S1, S3, S4, S5, S8, are turned"on", the output voltage across the load will be 'V1+V3+V4'.

- Mode 10: When switches S2, S3, S4, S5, S8, are turned "on", the output voltage will be 'V2+V3+V4'.

- Mode 11: When switches S1, S2, S3, S4, S5, S8, are turned "on", the output voltage will be 'V1+V2+V3+V4'.

- Mode 12: When switches S1, S6, S7, are turned "on",the output voltage across the load will be '-V1'.

- Mode 13: When switches S2, S6, S7, are turned "on",the output voltage will be '-V2'.
- Mode 14: When switches S3, S6, S7, are turned "on",the output voltage will be '-V3'.

TABLE I. THE SWITCHING STATES WITH CORRESPONDING VOLTAGE LEVELS

Output Voltage	S1	S2	S3	S4	S5	S6	S7	S8
V1+V2+V3+V4	1	1	1	1	1	0	0	1
V2+V3+V4	0	1	1	1	1	0	0	1
V1+V3+V4	1	0	1	1	1	0	0	1
V3+V4	0	0	1	1	1	0	0	1
V2+V4	0	1	0	1	1	0	0	1
V1+V4	1	0	0	1	1	0	0	1
V4	0	0	0	1	1	0	0	1
V3	0	0	1	0	1	0	0	1
V2	0	1	0	0	1	0	0	1
V1	1	0	0	0	1	0	0	1
0	0	0	0	0	0	0	0	0
-V1	1	0	0	0	0	1	1	0
-V2	0	1	0	0	0	1	1	0
-V3	0	0	1	0	0	1	1	0
-V4	0	0	0	1	0	1	1	0
-V1-V4	1	0	0	1	0	1	1	0
-V2-V4	0	1	0	1	0	1	1	0
-V3-V4	0	0	1	1	0	1	1	0
-V1-V3-V4	1	0	1	1	0	1	1	0
-V2-V3-V4	0	1	1	1	0	1	1	0
-V1-V2-V3-V4	1	1	1	1	0	1	1	0

III. COMPARISON OF THE PROPOSED TOPOLOGY

A brief study which is based on the number of switches, diodes, sources of proposed topology with other existing topologies for 21 level output is carried out. The results are given in TABLE II. From this TABLE, it is clear that this proposed Inverter requires a lesser number of switches and voltages sources to achieve the required voltage waveform.

TABLE II. COMPARISON OF DIFFERENT MULTILEVEL INVERTER TOPOLOGIES

Inverter	Number of	Number of	Number of	Number of	Capacitors
Cascade H-bridge	21	10	40	-	-
Diode Clamped	21	1	40	380	20
Flying Capacitor	21	1	40	-	210
Ref. [5]	21	6	13	-	-
Ref. [6]	21	4	12	-	-
Ref. [7]	21	4	11	3	-
Proposed Inverter	21	4	8	4	-

IV. CALCULATION OF SWITCHING ANGLES

The several methods of estimating the switching angle are proposed in [8]. Here Equal phase (EP) method and Half Height (HH) method are considered for calculating switching angle for the proposed 21-level inverter.

A. *Equal Phase Method*

In this method, the estimation of switching angles are performed by the equation (1),

$$a_i = i * \left(\frac{180}{m}\right) \qquad (1)$$

Where, i= 1, 2, 3, 4, $m-1$, and m= number of output level. These switching angles are distributed averagely over the range 0 – 180 degree.
This method gives better output voltage waveform.

The switching pulses obtained through Equal Pulse Method Half Height Method and those are illustrated in Fig.2 and Fig. 3.
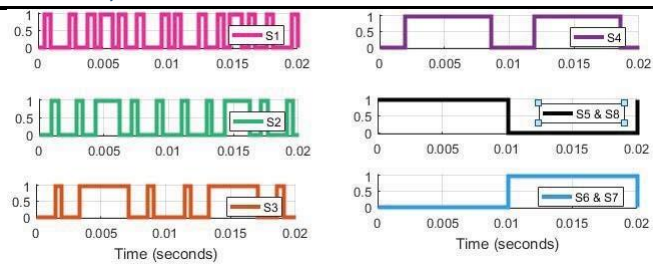
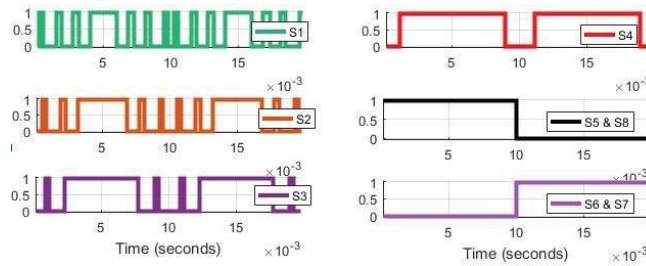Fig. 2. Switching pulse pattern for one complete cycle using Equal Phase method.

Fig. 3 Switching pulse pattern for one complete cycle Half Height method.

V.   SIMULATION RESULTS

- Input voltages: $V_1 = 35V$ dc, $V_2 = 70V$ dc, $V_3 = 105V$ dc, $V_4 = 140V$ dc
- Load: resistive type = 100 ohm
- IGBT: Internal Resistance, $R_{on} = 0.001$ ohm
- Snubber Resistance, $R_C = 100000$ ohm
- Snubber Capacitance, C_s = infinite.
- Diode: Internal Resistance, $R_{on} = 0.001$ ohm
- Snubber Resistance, $R_C = 500$ ohm
- Snubber Capacitance, $C_s = 250*10^{(-9)}$.
- Forward Voltage, $V_f = 0.8$ V

Fig. 4, shows the proposed 21-level voltage obtained for Equal Phase and Half Height methods and Fig. 5 illustrates the proposed 21-level current obtained for the same methods

The harmonic spectrum for the proposed inverter output. voltage has been computed with the aid of Fast Fourier Transform function (FFT) in MATLAB Simulink both for previously mentioned two methods as appeared in Fig. 6. The harmonic spectrum for the proposed inverter output current both for Equal Phase and Half Height methods have been calculated by using Fast Fourier Transform function (FFT) in MATLAB Simulink as depicted in Fig. 7.
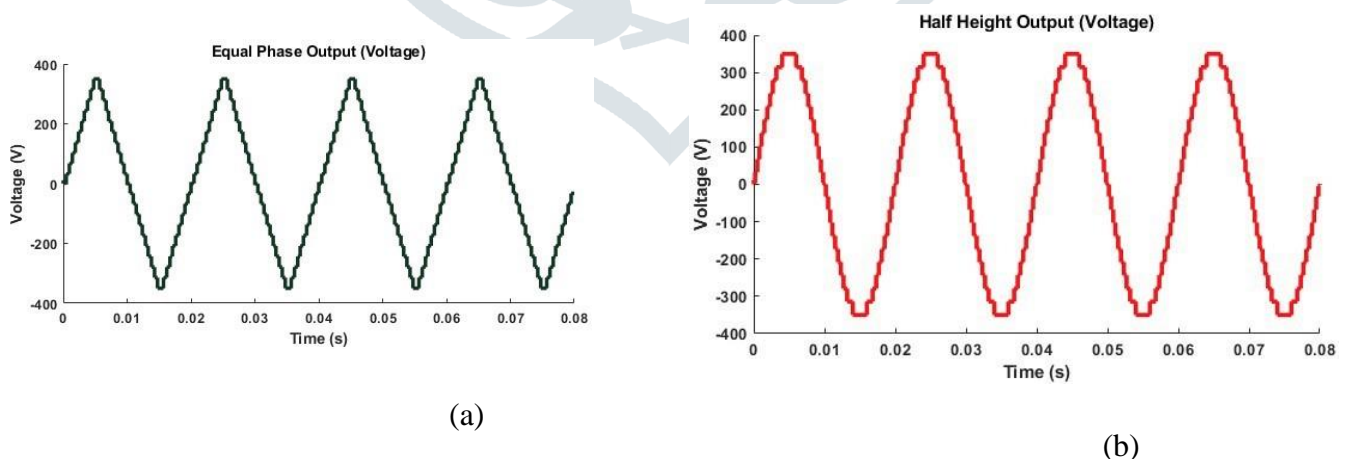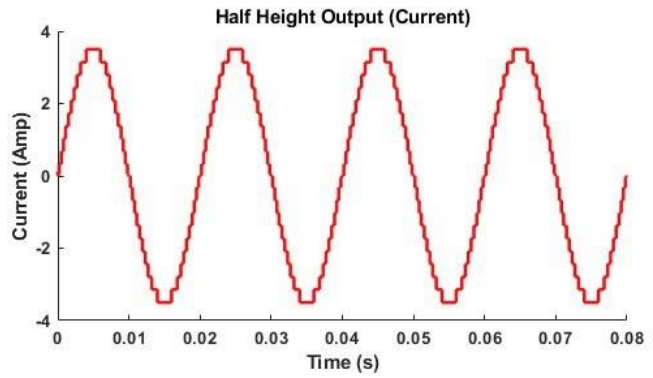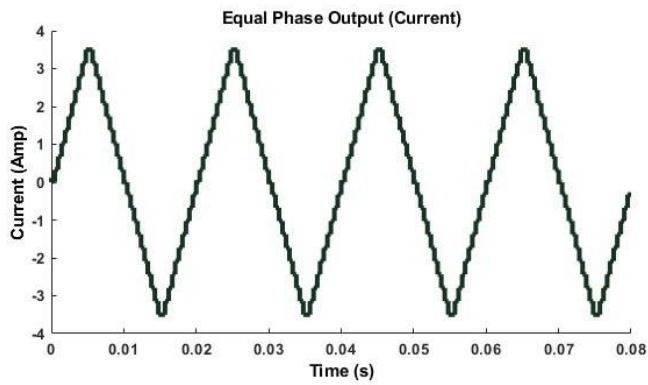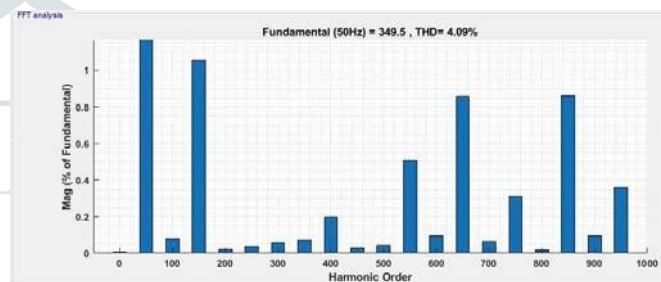

(a)

(b)
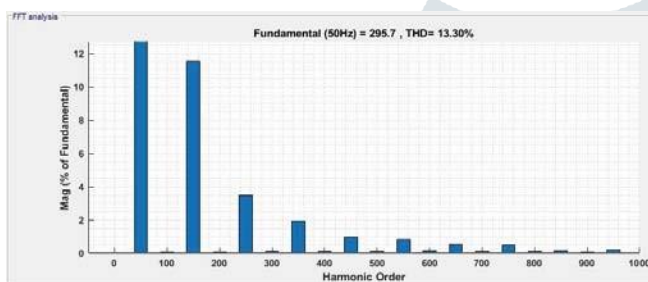
Fig. 4 Output Voltage (a) Equal Phase method (b) Half Height method.

(a).   (b)
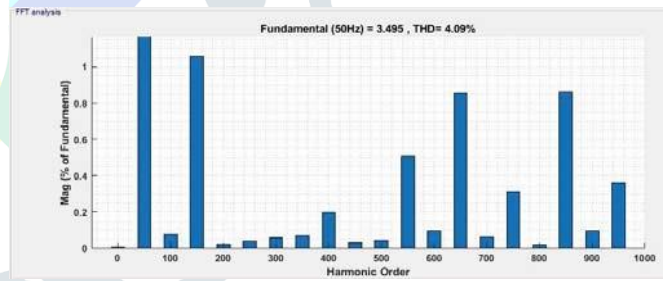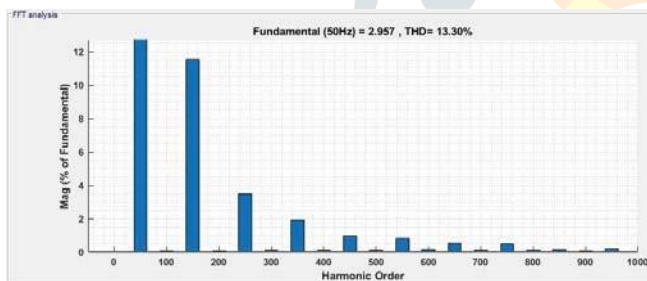
Fig. 5 Output Current (a) Equal Phase method (b) Half Height method.

(a).   (b)

Fig. 6 Output Voltage Harmonic Spectrum (a) Equal Phase method (b) Half Height method.

(a).   (b)

Fig. 7 Output Current Harmonic Spectrum (a) Equal Phase method (b) Half Height method.

The load voltage and current are distinguished in From the TABLE below, it can be summarized that load voltage and current of Half Height method are higher when compared with Equal Phase method. Hence, Half Height method provides better load voltage and current.

Table III Comparison of load voltage and table

| Method	Load Voltage (V)		Load Current (A)	
	Fundamental	RMS	Fundamental	RMS
Equal Phase Method	350	210.9	3.5	2.109
Half Height Method	350	247.4	3.5	2.474

The simulation result demonstrates that the Half Height method offers less THD than Equal Phase method. The results have been illustrated in the following chart.

Fig. 8 Comparison of total harmonic distortion among different methods.
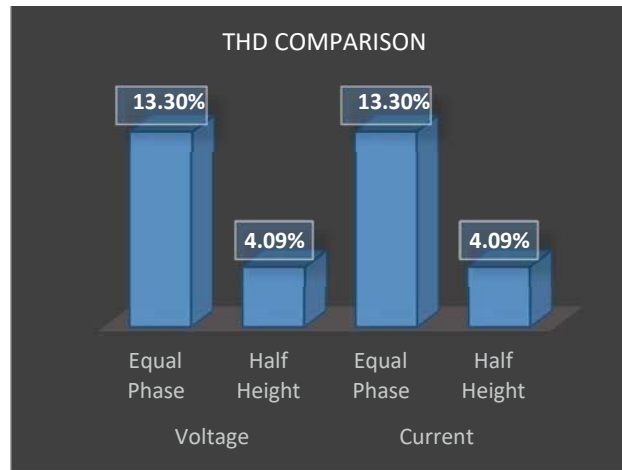
In the "Ref. [6]" the authors used several level shifted techniques for their proposed inverter. From this paper, it is appeared that the minimum THD for APOD technique obtained was nearly 11.13%. In the "Ref. [7]", 12.69% THD was obtained for the regarding proposed inverter. In this paper, 4.09% THD is introduced by the half-height method. The comparison result has been shown in the following chart.

Fig. 8 Comparison of total harmonic distortion with referenced works.
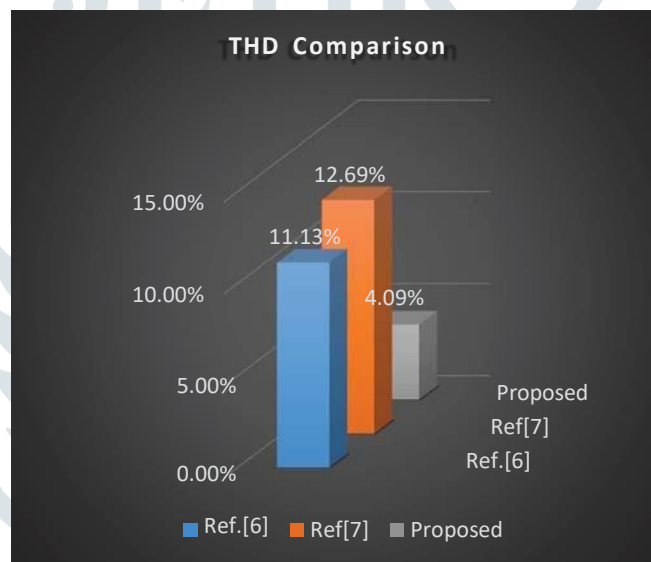
From the above chart, we can conclude that the proposed model offers less THD than among the existing reduced switch model.

VI.　CONCLUSIONS

The newly invented proposed inverter offers very less switching devices and dc sources for generating 21 level output voltage waveform. The outcomes of this proposed inverter topology results in smaller size, very low losses, along with quite low installation cost. In addition, THD in the output waveform of the proposed inverter is very low. Therefore, it is reasonable for medium voltage and high-power applications. The calculation of switching angles is obtained through Equal phase method and Half Height method. The simulation result shows that the Half Height method offers less THD compared with Equal Phase method. Besides, Half Height method achieves high RMS output voltage and current. Future work can be performed having made a 31-level inverter from the same circuit.

VII.   REFERENCES

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