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DESIGN OF LOW POWER FLASH ADC USING MEMRISTOR BASED ENCODER AND THREE STAGE COMPARATOR

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Abstract : This paper implements a 3-bit resolution Flash Analog to Digital Converter. The developed Flash ADC includes memristor-based encoders and 3-stage magnitude comparator, and the entire design was created using the Lt-Spice tool. The resistive ladder network is exposed to a 1.2V reference voltage. The flash ADC uses a two-stage pre-amplifier as a comparator. The main issue that typically arises in flash ADC is that as the number of resolution bits increases, so does the circuit's size and power consumption. As a result, we primarily focused on optimizing the encoder circuitry to lower the ADC's power consumption. Encoder is implemented utilizing MRL to decrease the area in order to save power consumption. Calculated and compared are the Flash ADC's performance metrics, including delay, average power, and transistor count.

Index Terms - Analog to Digital Converter (ADC), Memristor ratioed logic (Memencoder), Binary Decision Diagram (BDD), And-Inverter graph (AIG), Majority Inverter Graph (MIG).

I. INTRODUCTION

An analog signal is transformed into a digital signal by an analog to digital converter (ADC). The binary coded decimal is made up of the bits 1 and 0, is used to represent the digital signal. An analog input is instantly converted into an equal-valued digital output via a flash type ADC. As a result, flash type ADC is the quickest ADC. A voltage divider network, seven comparators, and a priority encoder make up the 3-bit flash type ADC. The following describes how a 3-bit flash type ADC works. There are 8 identical resistors in the voltage divider network. Over the whole network, a reference voltage VR is applied in respect to the ground. The integer multiples (from 1 to 8) of VR8 reflect the voltage dips across each resistor from bottom to top with respect to ground. All comparators' non-inverting terminals receive the external input voltage Vi. When applied to the inverting terminal of comparators from bottom to top, the voltage across each resistor lowers from bottom to top with respect to ground. Each comparator compares the external input voltage in addition to the voltage dips at the matching other input terminal. This shows that parallel comparison processes are carried out by each comparator. As long as Vi is greater than the voltage drops existent at the corresponding other input terminal, the comparator's output will be "1".

Similar to this, when Vi is less than or equal to the voltage drop existent at the corresponding other input terminal, the comparator's output will be "0". The inputs of the priority encoder are connected to all of the comparators' outputs. The important input, which has a value of 1, is translated into binary (digital output) via this priority encoder. As a result, the priority encoder only generates the digital output (binary equivalent) of Vi, the external analog input voltage. When a rapid rate of analog to digital data translation is required, the flash type ADC is used. The high priority input, which has a value of 1, corresponds to the (digital output) that this priority encoder produces. Consequently, the digital output (binary equivalent) of the external analog input voltage, Vi, is all that the priority encoder produces. When a quick conversion rate from analog to digital data is necessary, the flash type ADC is used.

The general block architecture of the Flash ADC is shown in Figure 1. It consists of a resistor ladder, comparator, and mem encoder.

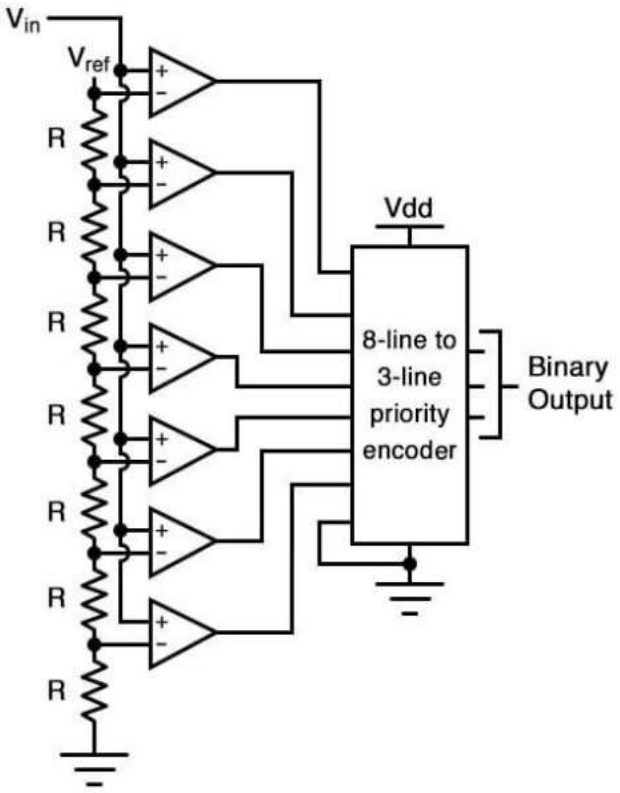

Figure 1: Flash ADC

II . LITERATURE SURVEY

Initially to develop an 180nm digital CMOS technology and build a 4-b Flash Analog to Digital Converter (ADC), the suggested flash ADC transforms the given continuous input signal into output binary code using a resistive ladder logic network, high-speed comparators and encoder logic. The flash ADC makes use of a unique encoder that was constructed using pseudo dynamic CMOS circuitry and required fewer transistors than earlier methods. The suggested ADC can run at its full sampling rate without the use of a time interleaving mechanism. The continuous input stream is converted into a digital output signal using a mixed signal device called an ADC. ADCs with high resolution, extremely high speed and less power are for a variety of System-on-Chip (SoC) applications, which frequently target portable applications. In many applications for wireless receiver systems, great resolution, fast speed and ultra-low power in the order of microwatts are crucial requirements. A modified double tail comparator circuit is employed in the two-step flash ADC that is presented. A high-speed 4bit flash ADC working at a 10GHz sample frequency is conceived and implemented in the suggested design. The design of comparators becomes increasingly important as flash ADC sample rates rise since it contributes to both less power consumption and high speed. To fulfill the necessary requirements in a 180nm CMOS manufacturing technology, various circuit design strategies are employed. The suggested flash ADC makes use of a unique encoder that was constructed using pseudo dynamic CMOS circuitry and used fewer transistors than other methods. The suggested ADC functions quickly and uses less power as a result. With a 1.8V operating voltage and a 0.686mW simulated power dissipation, the suggested ADC operates efficiently. Due to its appealing features, the suggested flash ADC is well suited for cutting-edge applications like high-speed wideband wireless receivers where speed is crucial [1].

The memristor, which is regarded as the fourth circuit component after the resistor, inductor and capacitor has been introduced. Memristors have some distinctive characteristics. It is capable of changing resistance when voltage is applied and it can hold its value even if the voltage is cut off. Memristors small feature size is an additional feature that helps in the development of incredibly small memory systems. The resistive switching property of memristors also enables the execution of logic primitives, making it possible to build logic functions utilizing the several logic design approaches examined in the research. A brief introduction to memristors and their uses in logic design have been covered. Following a brief introduction to the IMPLY design methodology, three scalable synthesis methods utilizing BDDs, AIGs, and MIGs are thoroughly addressed. The MAGIC design style is described and a various crossbar mapping and assessment problems are also mentioned towards the conclusion [2].

The technique of employing a memristor to create digital logic gates as an alternative to the current IC architecture. One of the forthcoming computing architectures will be this. Because memristors may be built on top of the polysilicon gate of an NMOS transistor, fabricating MRL gates is straightforward. The number of transistors on a chip will be denser. Compared to CMOS architecture, the proposed 3-bit encoder uses MRL and dissipates less power. This device is designed to simulate various combinational logic circuits, and the major goal of this study is to use LTSPICE to construct and analyze a 3-bit encoder using various logics. In the suggested process, a few transistors were replaced with memristors to create an encoder. Memristors serve as a pull-up network and use MRL to swap out the PMOS transistor encoder with memristor-based logic and traditional CMOS and pseudo NMOS logic, the memristor-based design is substantially greater effectiveness in terms of area and power. The trade-off between a circuit's power, area and speed is enduring. It is clear that this method of design results in a digital circuit that is more effective and requires fewer transistors overall. The need for novel methods to enhance the CMOS technique's efficiency and yield is still great, and efforts in this direction are very beneficial [3].

An adaptive flash ADC with less consumption of power is suggested here. While the drop in resolution is linear, the power reduction is exponential because of the ADC. The proposed system only uses leakage power because unused parallel voltage comparators are shifted to standby mode. The ADC operates at a sample frequency of 1 to 2 GSPS and is capable of functioning at 4-bit, 5-bit, and 6-bit precision. It dissipates 6mW at 4-bit and 12mW at 6-bit. Using Cadence tools, the ADC was designed and simulated in common 65nm CMOS technology. The suggested high-speed, low power, and programmable resolution flash ADC concept operates with a resolution that is determined by the peak voltage of the analog input. It uses less power and runs at a faster pace with a lower resolution. The built-in peak detector that will detect the peak level of the analog input signal and provides configurable feature is an advantage of the suggested ADC [4].

III. RESEARCH METHODOLOGY

3.1 Comparator

The Flash ADC's overall performance is determined by Comparator. Therefore, when constructing an ADC, several comparator features like speed, gain, latency, etc., should be taken into account. N-bit flash ADC requires 2N-1 comparators. Even a single bit increase in the resolution of the Flash ADC doubles the number of comparators needed.. The proposed comparator comprises of First two stages are called as preamplifiers and Third stage is called as latch stage. By acting as an inverter, this preamplifier increases the speed of the latch stage by enabling it to use the nMOS input pair M11–12 rather than the pMOS input pair. Additionally, the preamplifier produces voltage gain, which increases regeneration speed and reduces noise and input referred offset.

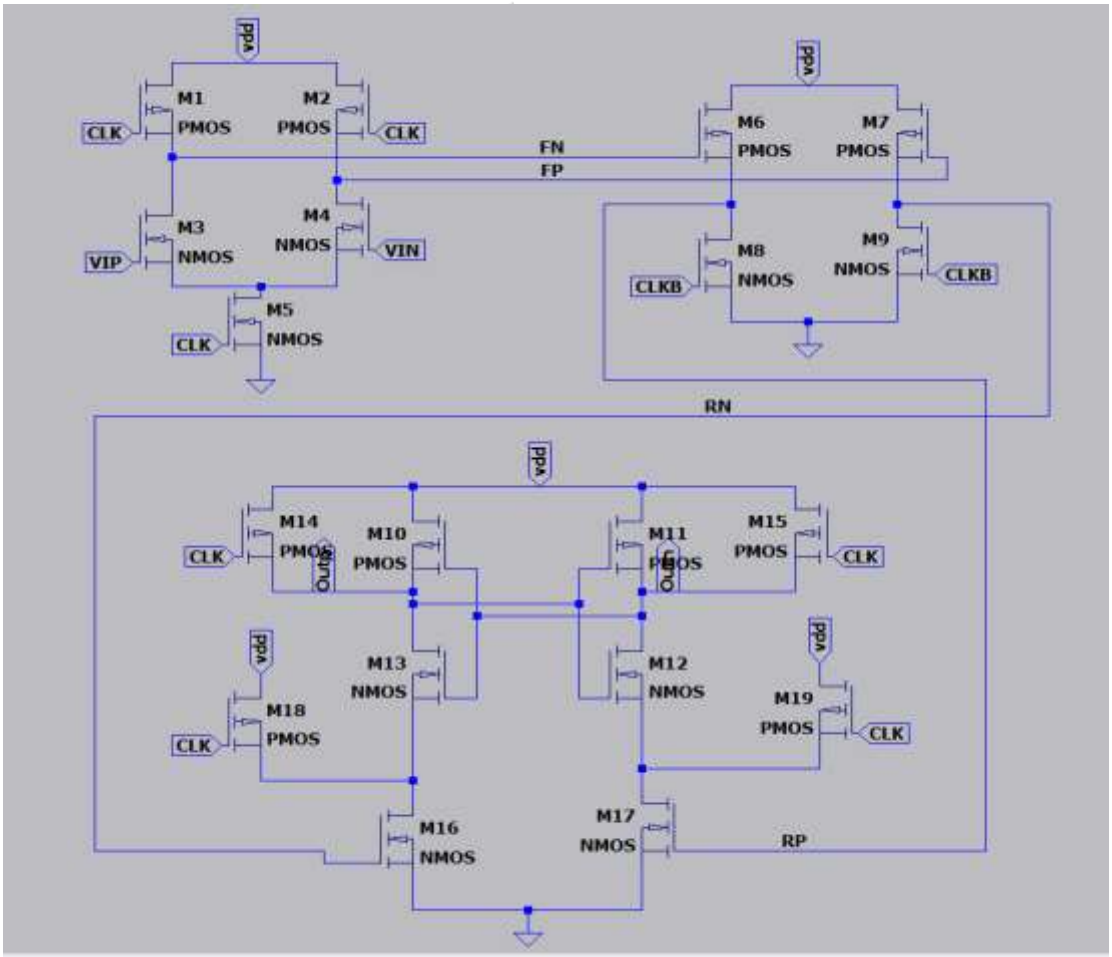

Figure 2: Three Stage Comparator

Figure 2 shows the 3-stage comparator in this work. The three stages are connected one after another. Compared with the Miyahara's comparator, the major difference is that one extra preamplifier (the second stage) is added. By acting as an inverter, this additional preamplifier allows the latch stage to use the nMOS input pair M11–12 rather than the pMOS input pair, increasing speed. Additionally, the additional preamplifier provides voltage gain, which accelerates regeneration and reduces noise and input referred offset. Although the extra preamplifier helps increase the speed, this extra stage itself incurs extra delay, because the amplified signal has to go through two phases as opposed to one, before arriving at the latch stage. Thus, it is necessary to discuss whether this extra delay overwhelms the benefit it brings about. The first-stage amplification, its outputs FP and FN fall to GND. This makes the second-stage input pair M8–9 have a large gate–source voltage equal to VDD. As a result, the current on M8–9 is large enough for quickly pulling up RP and RN. This means that the extra delay incurred by the second stage is small (about 20ps in post-layout simulation) compared to the large delay of the latch stage (about 200ps in post-layout simulation). This makes sense because the second stage is actually a dynamic inverter which does not incur much delay. Furthermore, compared to the first-stage output load in the Miyahara's comparator (M6–7 and M12–15 in Figure 2), the first-stage output load in the 3stage comparator is only M8–9 in Figure 2. The output load is reduced by several times, improving the amplification speed.

3.2 Encoder

Information in digital logic circuits with specific meaning is encoded into corresponding binary bits. Encoder is a circuit which does this encoding function. The encoder's function is to encode when one of the input bits is of effective level, and the encoder's output changes in accordance with its input bits. The circuit has 'N' outputs and 'M' inputs and they are related by M = 2N.

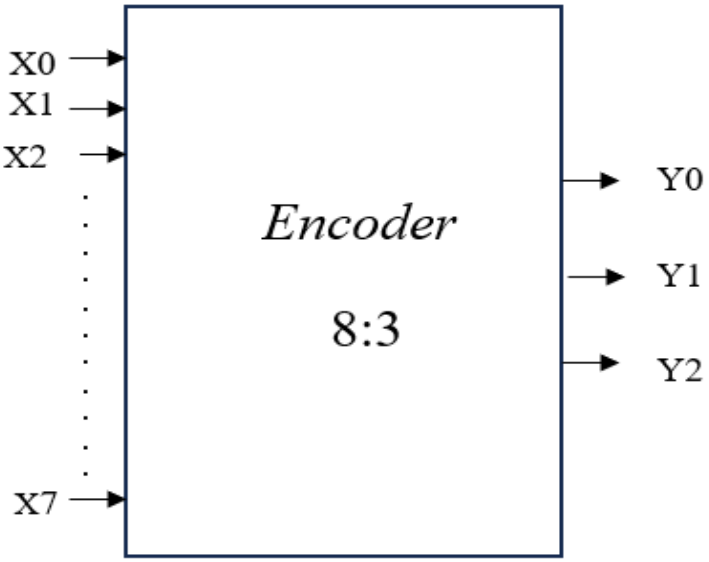

Figure 3: Three-Bit Encoder

From the Encoder truth table, the outputs and inputs are related by

Y0 = X1 + X3 + X5 + X7

Y1 = X2 + X3 + X6 + X7

Y2 = X4 + X5 + X6 + X7

Table 1: Truth Table Encoder

X0	X1	X2	X3	X4	X5	X6	X7	Y2	Y1	Y0
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

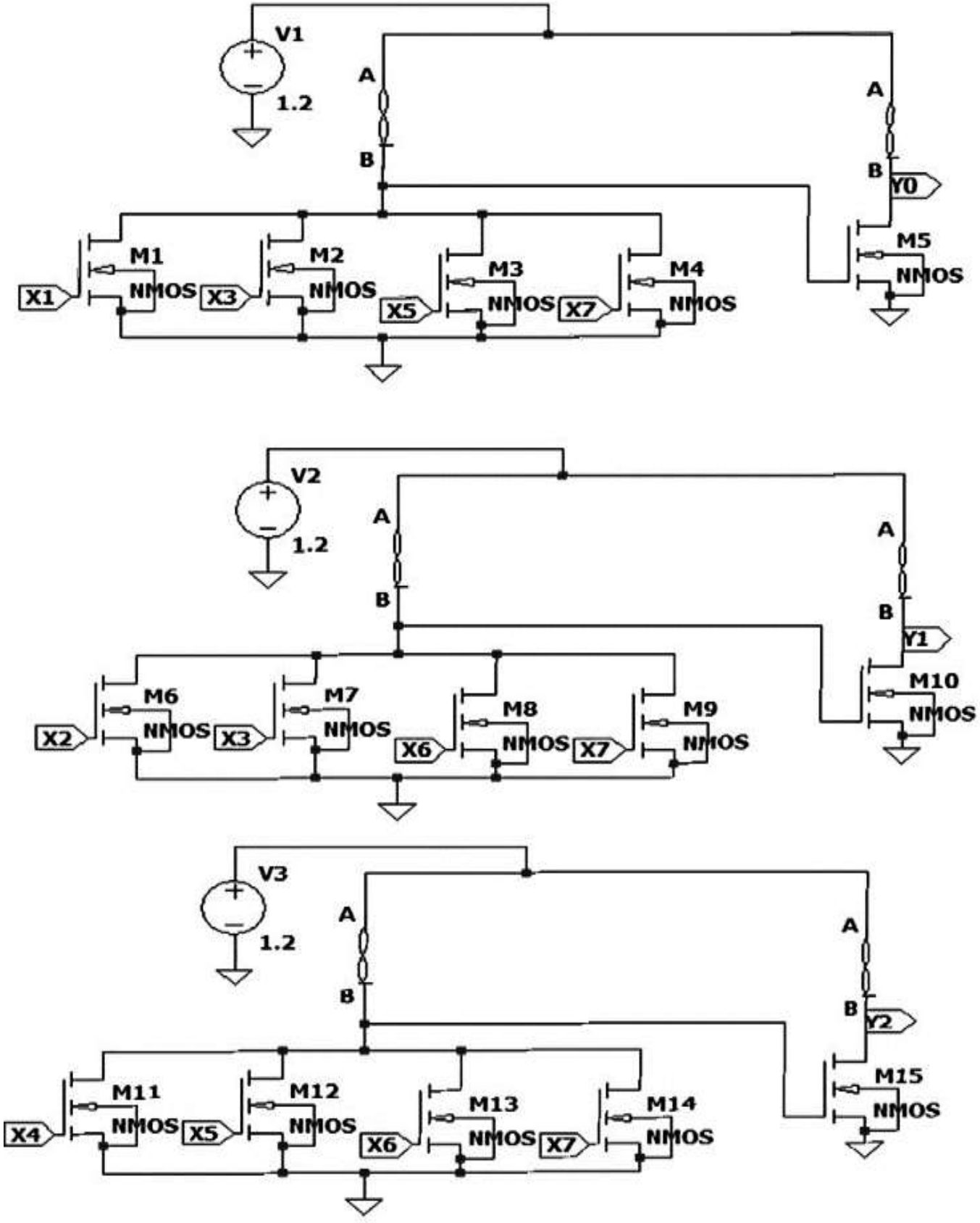

Figure 4: Schematic Of Encoder Using Memristor Based Logic

From these relations, logic circuit can be implemented using CMOS, Pseudo NMOS and MRL. In the Encoder circuits, X1- X7 are input bits and Y2, Y1, Y0 are output bits. In Encoder circuit by using MRL, M1, M2, M3, M4 act as pull-down network and a Memristor acts as pull-up network. M1, M2, M3, M4 and Memristor constitute a 4-input NOR gate. X1, X3, X5, X7 are the input signals that passes via NOR gate and the signal at the drain of M1 is inverted signal of (X1 + X3 + X5 + X7). M13 and Memristor constitute an inverter. The output of 4-input NOR gate is given as the input of inverter. The signal at the drain of M13 is Y0 = X1 + X3 + X5 + X7.

IV. RESULTS AND DISCUSSION

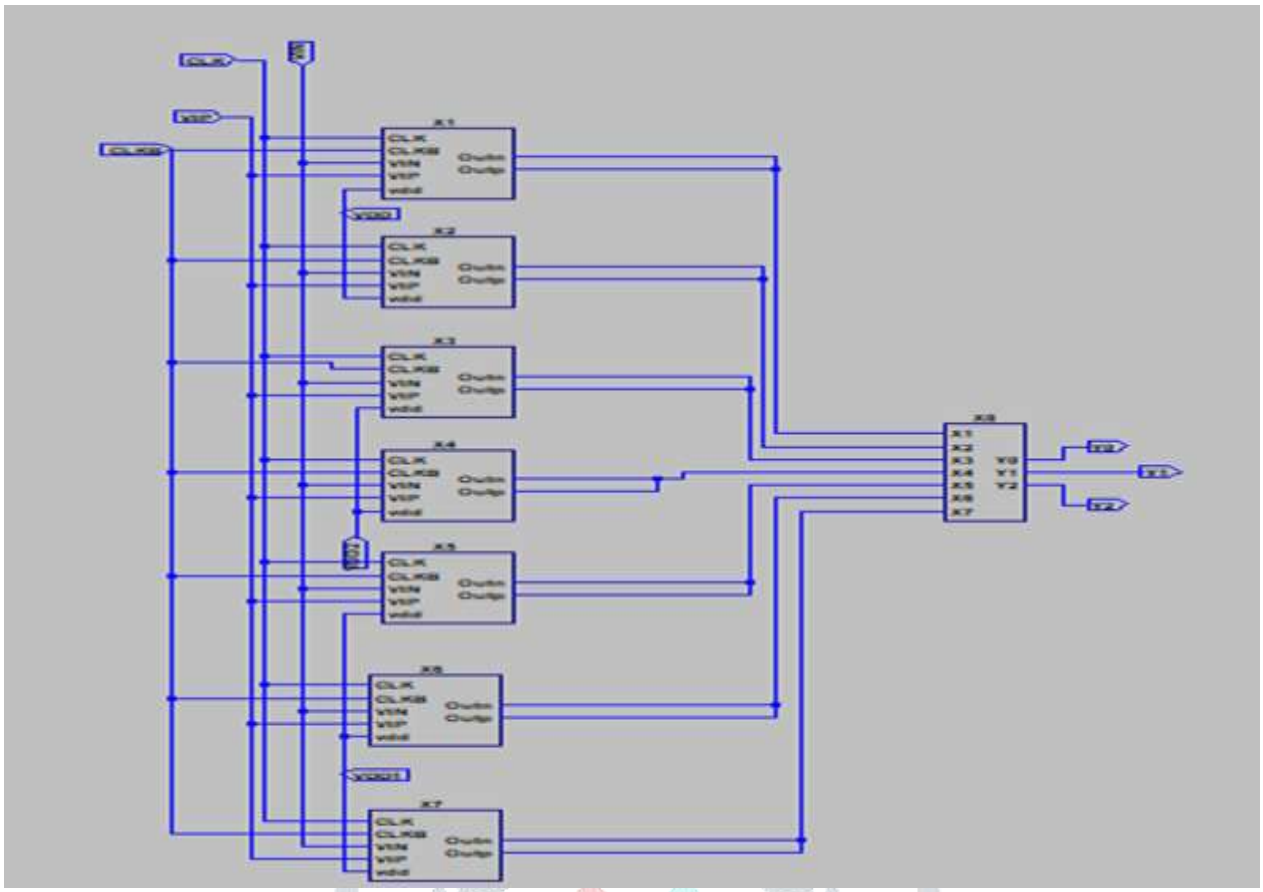

Figure 5: The Schematic of The Proposed Flash ADC

Figure 5 shows the generic schematic representation of the proposed flash ADC which comprises of 3 stage comparator and memencoder.

Figure 6: Waveforms Of Proposed Flash ADC

The result of the proposed flash ADC as shown in the above waveform of figure 6. The analog sinusoidal input is given to the proposed flash ADC and obtained the digital output as shown in the above waveform.

Table 2: Comparison Table

	Power	Delay	No of Transistor
Existing	187mW	38.5µs	170
Proposed	60.2mW	468.5ns	155

This paper represents an optimized architecture for Flash ADC with Memristor technique which is designed using LT-SPICE Tool. From the design and analysis, this work will be an improvisation of flash ADC design using advanced three stage comparator and 3-bit memristor encoder technique. The outcomes are better compared to the existing designs of flash ADC. The proposed design has lesser area and power dissipation and will operate at highest speed. The number of transistors required to develop the design is also very less compared to the CONVENTIONAL FLASH ADC design. The proposed design is implemented in LT-SPICE Tool and Optimized in terms of power by 67.8% and delay 90%. The power optimization is achieved through the use of memencoder of memristor technique and delay optimization is obtained through the use of high speed advanced three stage comparator. The proposed Flash ADC design is suitable for high performance and less cost for below 5nm technology and small IC's.

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