Non Linear Carrier Controlled Power Factor Correction Boost Converter

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***Abstract*— Power factor plays a vital role in industries; Power quality is critical to efficient operation of equipment. One contributing element to power quality is power factor. A Non-Linear Carrier Control (NLC) method is proposed here for power factor correction (PFC) boost converter which provides high power factor (PF) and low total harmonic distortion (THD) in wide input voltage and load range. The proposed (NLC) method employs a zero current duration (ZCD) demodulator that detects ZCD in each switching cycle to estimate current conduction duration of the boost inductor. Using the estimated signal of ZCD demodulator, the proposed controller generates a compensated duty signal with a PFC converter to properly operate in continuous conduction mode (CCM) or discontinuous conduction mode (DCM). Unlike the conventional NLC PFC converter where the line current is distorted in DCM resulting in poor PF and high THD. The proposed NLC method can provide higher PFC performance regardless of CCM and DCM while maintaining the simple control loop of conventional NLC method that does not require inner current loop and using relatively smaller inductance.**

I. INTRODUCTION

Power factor correction (PFC) converters have been indispensable in various applications such as lightings, TVs, computers, and so on. Since drastic electricity demands in those electric devices leads to increase harmonic currents on power grids, lots of installation of the electric power system is required, for example, power plants and transmission lines. For the reason, harmonic regulation gets more stringent such as IEC61000-3-2- and various PFC converters and control methods have been proposed and employed widely in various applications, so far. Among various types of PFC control method, non- linear carrier controlled (NLC) method was proposed and has been utilized for middle to high power range.

Harmonics are a distortion of the normal electrical current waveform (i.e) the current and voltages are distorted and deviated from sinusoidal waveform, generally transmitted by non-linear loads example for non-linear loads switch-mode power supply, speed motor, drives, photocopies, personal computers, machines etc. and it is interference in AC power signal created by frequency multiples of sine wave.

THD is defined as the ratio of the equivalent root mean square (RMS) voltage of all the harmonics frequencies over the RMS voltage of the fundamental frequency. Thus it can be calculated as

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} V_{n_{rms}}^2}}{V_{fund\_rms}} \qquad (1)$$

For the low to middle power range, discontinuous conduction mode (DCM) or critical conduction mode (CCM) PFC converters have been studied and widely employed. For the middle to high power range, continuous conduction mode (CCM) PFC converters usually have been employed, in which the root mean square (RMS) current is smaller than one of the CRM or DCM PFC converters using relatively low inductance.

Generally, the CCM PFC offers high performance when it operates in CCM. But, when it enters DCM operation as the load decreases or the line input increases, the input current can be distorted resulting low PF and high THD. This may lead to employ physically large inductance considering tolerance of inductance in order to guarantee CCM operation under as much of load condition. Accordingly, new control methods have been actively researched to overcome this problem.

Among various control methods for CCM PFC converters, the non-linear carrier control (NLC) method (also referred to as one cycle control (OCC) or modulated carrier (MCC) control method) has attracted considerable attention due to its simple control loop which does not require sensing line input voltage and current loop so that it provides fast dynamic response compared to the conventional CCM PFC boost converter.

To overcome the problems of the operation mode while maintaining the advantages of the conventional NLC method, this paper proposes new NLC method for PFC.

II. ZERO CURRENT DURATION DEMODULATOR

A. *Non- linear carrier controller*

The conventional NLC PFC converter where the line current is distorted in DCM resulting in poor PF and high THD. This is because the boost converter operates in CCM operation during the entire cycle of the ac line and results in low THD of 2.4%.

The charging current of the output capacitor is discontinuous resulting in larger capacitor size and EMI issues. As similar to the buck-boost converter, the efficiency is poor for high gain i.e. very large duty cycle. Therefore, high gain operation cannot be achieved with this converter efficiency can be as poor as 60% for a duty cycle of 0.7. Whereas it has highest efficiency for duty cycle of 0.5.

There is no isolation from input to output which is very critical in many applications like the power supply of gate driver of power semiconductors.

In this method, as the load decreases, THD performance deteriorates gradually reaching up to 21.81% at 10% load condition. At the low line input of 110Vrms, THD values with this method start to deteriorate because it starts to enter DCM operation at 30% load condition.

B. *Zero Current Duration (ZCD) Demodulator*

This paper proposes new NLC method for PFC. The proposed NLC method employs a zero current duration (ZCD) demodulator that detects a ZCD in each switching cycle to estimate the current conduction duration of the boost inductor. The ZCD demodulator converts the measured duration to a compensation signal. With the compensation

signal from the ZCD demodulator, a new controller generates appropriate duty cycles in either of CCM or DCM operation. Therefore, the proposed MCC method no longer requires relatively large boost inductance compared to the conventional NLC boost converter. Additionally, the proposed control method uses a resistive and capacitive (RC) low pass filter to detect average inductor current for better noise immunity.

This paper proposed new NLC method for PFC boost converter to provide a high PF and low THD in a wide line input voltage and load range while maintaining the simple control structure and fast dynamic response of the conventional MCC method. In addition, the proposed MCC method provides more flexibility in designing a boost inductor so that it does not consider using a big enough inductor to guarantee CCM under as much load range as possible to meet the harmonic regulation. Therefore, the proposed control method could be a good candidate as a controller for high performance PFC boost converter that covers wide line input voltage and load range.

III. Method Of Implimentation

A. Block Diagram of Proposed Method

In this paper we use unique methodology to implement the proposed concept the detailed block diagram of the proposed method is shown in figure 1 and it composed of control part, display unit, sewing motor, single phase inverter, driver unit, boost converter, rectifier and filter.

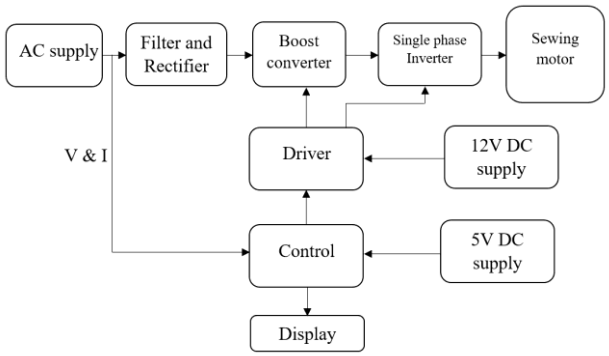

Fig. 1. Block diagram of the NLC PFC

A 230V AC supply is given to the filter circuit where the capacitor act as a filter, which passes the low frequency signal and bypasses the high frequency signal, capacitors are used to smooth the pulsating DC output after rectification.so that nearly constant DC voltage is supplied.

A rectifier is an electrical device of one or more diodes that converts alternating current (AC) to direct current (DC).the result is DC voltage that pulses at twice the frequency of the input. Then DC supply is given as input to the boost converter. A boost converter is a DC-DC power converter that steps up voltage from its input to its output. (i.e) an output voltage greater than the input voltage. A boost converter is sometimes called as step-up converter since its "steps up" the source voltage.

Thus Control part is composed of an output voltage error amplifier, ZCD demodulator, PWM generator and inductor current sensing resistor.

ZCD demodulator detects duration of the zero inductor current in each switching cycle at DCM operation and converts duration to compensational signal. An output voltage from the boost converter is compared with the reference voltage where the error of this output voltage is overcome by the output voltage error amplifier. The divider helps to divide the output voltage and then compared with the reference current.

At the PWM generator, duty control signal is compared with the saw tooth waveform and generate the appropriate duty cycle able to cover the CCM and DCM operation. The control circuit generates the duty control signal using output signal from the ZCD demodulator and an average inductor current and the output voltage of the output error amplifier.

Then the output of the microcontroller given to the driver MOFET circuit as input signal. And the microcontroller input signal level is in order of 5V. Driver TLP250 contains an input stage and an output stage. Which is suitable for MOSFET and IGBT. Unlike the other MOSFET driver it is optically isolated from each other. Whenever input stage LED light falls on output stage photo detector diode, output becomes high. This circuit will trigger the MOSFET based on the input.

Thus the corrected voltage is again given to the boost converter as a input to perform the operation, then this DC voltage is converted into AC by using single phase inverter to show the harmonic reduction and sewing motor is connected with the inverter for Power factor correction (i.e) high power factor and LPF to reduce the noise immunity. you.

B. Non- Linear Carrier Controlled Power Factor Correction.

The PFC controller maintains an input current i_{in} in proportion to following an Ac input voltage V_{in} while keeping an output voltage V_O as a specified reference V_{REF}. With this assumption, n input impedance of the PFC converter can be expressed as

$$R_e = \frac{V_{in}}{I_{in}} \tag{2}$$

Where R_e is an emulated resistance.

The input current I_{in} can be expressed with a function of the average current of the boost inductor $\langle i_L \rangle$ and can be expressed as

$$i_{in} = \langle i_L \rangle = \frac{1}{T_s}\int_0^T i_L(t)dt \tag{3}$$

Where T_s is the switching period of the controller and is the instantaneous inductor current, which can be detected through a sensing resistor, R_{cs}.

Meanwhile, assuming negligible power losses between the input and output, and slowly-varying v_{in}, a voltage conversion ratio of the boost converter can be obtained as (4) by applying the volt-sec.

$$V_{in} = \frac{D_2}{D_1 + D_2} V_o \tag{4}$$

Where D_1 is the duty ratio of the MOSFET and D_2 is the time interval ratio of the discharging inductor current.

Substituting (2) and (3) into (4), a relationship between the output voltage and the average inductor current $\langle i_L \rangle$ can be rearranged as

$$R_e . \langle i_L \rangle = \frac{D_2}{D_1 + D_2} V_o \tag{5}$$

Then, the control equation can be expressed as

$$\left(1 - \frac{i_L}{V_{COMP}}\right).(D_1 + D_2) = D_1 \tag{6}$$

Where V_{COMP} is equal to V_O/R_e and represents the control signal from the output voltage error amplifier.

As mentioned previously, the average inductor current gradually changes in proportion to the ac input voltage in a line frequency and the other parameters R_e and V_o are constant. Accordingly, if the amount of time of D_1 and D_2 is measured properly and can be input of (6), the appropriate duty ratio D_1 can be naturally generated by the sensed average inductor current $<i_L>$, which makes the sinusoidal input current waveforms in proportion to the input voltage regardless of CCM and DCM operation.

C. ZCD Demodulator Implimentation

To solve the left term in (6), the control circuit requires information on amounts of time of D_1 and D_2. However, because the unit of both D_1 and D_2 is time, it needs to be converted to a voltage signal acceptable to the controller. The ZCD demodulator detects the amounts of time of D_1 and D_2 and converts them to a compensation voltage signal VBDCM. The ZCD demodulator simply consists of a detecting capacitor CD, current to voltage converter comprises of current source IB and zener diode ZD, rising edge triggered D-FF (flip flop) and RC low pass filter.

The following steps and procedures of the ZCD demodulator circuit operation.

- During a high gate signal, the D-FF stays in the reset state so that the Q-bar output remains high regardless of the inverted V_D signal input to CLK of D-FF.
- After a gate signal switches from high to low, D-FF is enabled and a drain to source voltage v_{DS} increase up to V_o by the MOSFET is turned off as well. Accordingly, I_{CD} flowing through C_D increases as v_{ds} increases and makes a detecting voltage V_D, which is clamped by Z_D. And V_D is input to CLK of the D-FF through the inverter logic. However Q-bar output of D-FF still remains high.
- While the MOSFET is turned off, and inductor current is gradually discharged. As soon as it is fully discharged, resonance is initiated by the boost inductor and parasitic capacitance of MOSFET. This causes fluctuation of v_{ds} and C_D is repeatedly charged and discharged by I_{CD}. During the discharging, when I_{CD} is lower than '$-I_B$', V_D is changed to zero. At the transition of V_D, a rising edge signal occurs at CLK of D-FF. Then, the Q-bar output of D-FF is changed but, maintained as low until the next high-gate signal resets the D-FF. The pulse V_{ZCD} generated from D-FF is flattened by the RC-filter R_{DF} and C_{DF}. Finally, V_{ZCD} becomes a compensation signal V_{BDCM} in the proposed control method. At CCM operation, the Q-bar of D-FF. On the other hand, as discontinuous conduction duration increases, gradually decreases from the maximum output voltage.

D. PWM Generator

Finally, in this method, a duty ratio, D_1 to satisfy (6) can be simply obtained by comparing a duty control signal V_{DC} with a periodic saw-tooth wave form having constant slope as follows:

$$V_{DC} = \left[1 - \frac{i_L}{V_{COMP}}\right].V_{BDCM} = V_S.\left[\frac{t_{on}}{T_S}\right] = D_1 \qquad (7)$$

Where V_S is the peak voltage of the saw-tooth waveform and t_{on} is the MOSFET turn on time

In addition, (7) can be realized as a PWM circuit

The conventional MCC method is derived based on the assumption of that the boost converter operates in CCM. As mentioned in Section I, a line input current can be distorted when the conventional MCC PFC boost converter operates in DCM. In this section, a condition for operation in DCM is confirmed and current distortion in DCM is analysed.

The control equation of conventional MCC can be also derived from (5) as

$$R_e.\langle i_L \rangle = (1 - D_1).V_o \qquad (8)$$

The average inductor current (i_L) is the amount of two average currents flowing through a MOSFET and output diode. Accordingly, (8) can be expressed with the average MOSFET current (i_L) as follows:

$$R_e.\langle i_s \rangle = (1 - D_1).V_o \qquad (9)$$

Substituting (9) with (i_s) derived from Fig. gives a relationship between a line input voltage $v_{in}(t)$ and output voltage V_o as follows:

$$\langle i_s \rangle = \frac{|v_{in}(t)|}{2.L_B} D_1^2 T_S = D_1(1 - D_1).\frac{V_o}{R_e} \qquad (10)$$

Where vin (t) is the line input voltage V_{inpk} sin(wt).

And a duty ratio D_1 can be derived using (10) as

$$D_1 = \frac{1}{1 + \frac{R_e|v_{in}(t)|}{R_o k.v_o}} \qquad (11)$$

Where R_e is V_o/I_o , and K is $2L_Bf/R_o$, that is the load parameter commonly used in DCM analysis.

When the boost converter operates in DCM, D_1 meets the following condition,

$$D_1 < \left(1 - \frac{|v_{in}(t)|}{v_o}\right) \qquad (12)$$

On the other hand, D_i is equal or higher than the right term in (12) while the boost converter operates in CCM.

Substituting (11) into (12) gives DCM operating condition as

$$K < \left(1 - \frac{|v_{in}(t)|}{v_o}\right).\frac{v_{inpk}}{2.v_o} \qquad (13)$$

In addition, during DCM operation of the conventional MCC, (8) can be replaced to the expression for the input current using (11) as follows;

$$I_{in} = \langle i_L \rangle = \frac{|v_{in}(t)|}{K.R_o} \frac{v_o}{v_o - |v_{in}(t)|} D_1^2 \qquad (14)$$

The electrical specifications and parameters are introduced in Fig. are equally applied to this simulation. Among the normalized line input current waveforms, 'SIN_REF' is sinusoidal waveform for a reference, K of 0.11 is a calculated result at full load condition whose THD is 1.55% and K of 0.23 is a result at the load condition of 200W whose THD is 7.2%.

At the result, THD variation can be estimated depending on a load, frequency and inductance. Assume that THD at 'A' point is at full load condition. If the load is reduced to the half, THD increases up to 8% depicted as 'B' point. If THD at 'B' point cannot meet a requirement, then inductance

should be double. This is one of disadvantage of the conventional MCC where the boost inductance should be designed enough big considering a line input voltage and load condition.

Therefore, the proposed MCC method introduced in the paper is expected to provide high PFC performance regardless of the line input voltage and load condition unlike the conventional MCC method.

IV. Simulation and Results

A. Simulation

The simulation of this project is done using MATLAB 2016b in a system with i5 fifth generation processor, 4gb ram.

The figure 6.1 shows the simulation diagram of the PFC boost converter. The connection of this diagram is made as same as of the requirement. A PFC boost converter is connected with a rectifier and filter, with an AC supply. Through the rectifier an AC supply is converted into DC supply. Filter is to smoothen the pulsating DC output after rectification. Without the load connection boost converter shows the power factor output of 0.87 and harmonics at high level. Thus the simulation method is easy to verify the desired output.

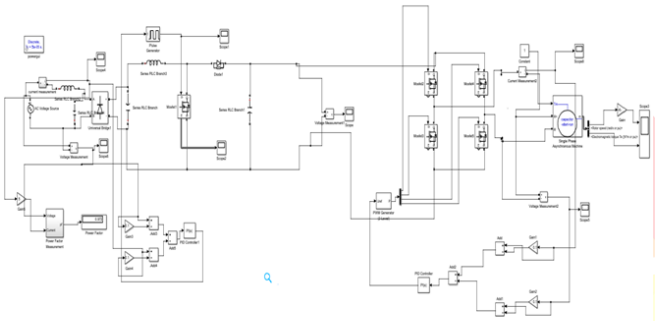

Fig. 2. Simulation diagram of PFC boost converter

The figure 2 shows the simulation diagram of the NLC PFC boost converter included with microcontroller and driver unit. Thus the controller performs voltage or signal correction with the help of using PWM generator and ZCD demodulator. Which compensates the signal and generate the duty signal.

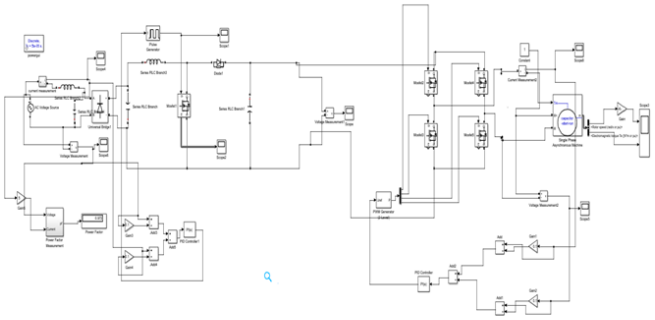

Fig. 3. Simulation diagram of NLC PFC boost converter

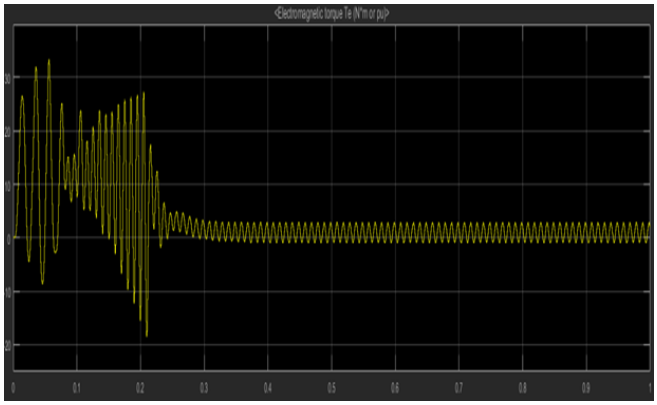

Fig. 4. Simulation output of the power factor

This signal act as input to the driver circuit which triggers the MOSFET and boost up the signal to the load and converted into AC signal through the single phase inverter. The sewing motor which operates through the auto transformer of voltage between 100V – 130V act as a load which gives the power factor output of 0.97 and the simulation output shows the lower harmonics with this NLC PFC boost converter. Thus it gives fast dynamic response, good flexibility, ripple reduction and noise reduction using RC low pass filter.

Figure 4 shows the power factor correction clearly. The signal analysis shows the 3 cycle waveform. FFT shows the harmonic is reduced to 3.52% .

V. Conclusion

A. Conclusion

This "NON-LINEAR CARRIER CONTROLLED PFC BOOST CONVERTER" to provide a high PF and low THD in a wide line input voltage and load range while maintaining the simple control structure and fast dynamic response of the conventional method. In addition, this method provides more flexibility in designing a boost inductor so that it does not consider using a big enough inductor to guarantee CCM under as much load range as possible to meet the harmonic regulation.

This NLC method and feasibility were verified using 400W PFC boost converter. This showed outstanding performance of THD of 2.39% and 5.76% under each input voltage of 220 V_{rms} and 110 V_{rms} with full load condition, respectively. Moreover, THD of less than 7% was maintained even though the load was decreased up to 20%. Therefore, this method could be a good candidate as a controller for high performance PFC boost converter that covers wide line input voltage and load range.

B. Future Work

This NON-LINEAR CARRIER CONTROLLED PFC BOOST CONVERTER method gives better efficiency. For further power factor correction instead of the single PFC boost converter an INTERLEAVED converter (i.e) a multiple PFC boost converter with a series or parallel connection will give twice the efficiency of NLC PFC boost converter and reduces I^2R losses and inductor AC losses.

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