Performance Analysis of CMOS and FinFET Based Adiabatic SRAM Cell at 32nm Technology

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***Abstract*—In VLSI system design, Power consumption and energy dissipation of a circuit have become very crucial factors. There are different techniques to reduce the power and energy consumption of the circuit in which adiabatic technique is one amongthem. The power and energy recovery capability of thecircuits can be optimized using adiabatic technique andpower consumed in VLSI circuits can be reused. SRAM (Static random-access memory) has good speed to access the data but it has more power dissipation. Hence SRAM cell with adiabatic logic has been proposed in both CMOS (180nm and 32nm) and FinFET (32nm) to reduce the power and energy consumption. This adiabatic SRAM cell operatessame as typical 6-T SRAM cell. SCRL (Split level charge recovery logic)is used to design SRAM cell's latch. The Monte Carlosimulation is also performed forboth CMOS and FINFET technologies using HSPICE and results shows FinFET based SRAM cell has 2.37 times less power consumption as compared to the CMOS based SRAM cell.**

Keywords: Adiabatic logic,SCRL, FinFET, Monte Carlo simulation, HSPICE

I. INTRODUCTION

Scaling of CMOS technology improves performance of the IC but it is challenging due to various SCE (short channel effects). Double gate MOSFETs or FinFETs are used to overcome such limitations since it has ability to reduce short channel effects [1]. The advancement in nanometer technologies, operating frequency and chip density increased. This constituted power consumption in portable devices a major concern. In non-portable devices, it is important to reduce power consumption to minimize cooling cost and potential reliability. To overcome this VLSI (very-large-scale integration) designer's goal is to meet performance requirements.

In digital circuits, memory cells play crucial role in accordance with power, speed and performance. Most of the power is drained by memory cells. The mostly affected circuit because of scaling is the SRAM (static random-access memory). This happens because of minimum sized transistors used in SRAM cells to overcome the area overhead [2]. Trapezoidal pulse shaped power supplies can reduce the power consumption in SRAM circuits which is referred as *adiabatic SRAM cell*.The trapezoidal voltage signals enable the charging and discharging at memory cell nodes which reduces the power consumption. SRAMs consume high power because of it's the high accessing rates andhigh capacitance. Half of the power consumed in CPUs is due to the SRAMs [3] in an extremely power efficient designs. Adiabatic 1ogic has emerged to reduce the dynamic power consumption without sacrificing noise immunity and driving abi1ity.

II. BACKGROUND

A. *FinFET Device*

FinFET has better electrical characteristics such as high-speed performance, good sub-threshold slope and importantly reduced short channel effect. The physical structure of the FinFET helps it to perform differently fromthe traditional bulk MOSFETs. As shown in Figure 1, fin on the top of the silicon acts as a channel. Whereas source and drain are located on either sides of the fin and the gate covers the fin sidewalls to control the conductivity of the channel. The effective length of the channel depends on the thickness of the fin. The fin wrap allows in reducing the leakage current by improving the channel's electrical characteristics. The reduced leakage current reduces the circuits overall power consumption. Hence, the FinFET proves to be a low power and reliable device.

FinFET technology can be scaled down beyond 28nm since it has many advantages compared to CMOS which include lower leakage, high drive current,high speed, lower power consumption and better mobility.

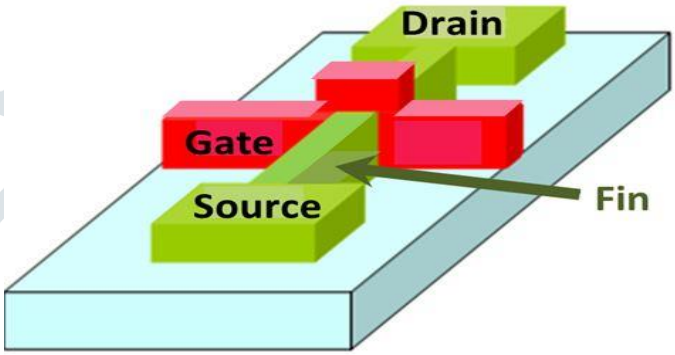

Fig 1: Internal structure of FinFET

Since FinFETs have high control on SCEs and DIBL (Drain induced-barrier lowering)[4], it is better alternative for CMOS.

B. *Adiabatic Logic*

Adiabatic Logic finds importance in low power VLSI circuits in which reversible logic is implemented. The total heat or energy of the adiabatic circuit's remains constant. Most research has focused on building adiabatic logic using CMOS butFinFET technology has more advantages compared to similar technologies.There are two fundamental rules to be followed in adiabatic circuits. Firstly, transistorsshouldn't be turned on when there is a potential difference between the

source (S) and drain (D).Secondly, transistorsshouldn't be turned off when current is flowing in it.

In adiabatic logic circuits [5],the energy in capacitor is recovered and fed back to the power supply. Ideally, adiabatic logic circuits dissipate zero power and have importance in low power designs. Typically, theoperation of the adiabatic circuit has four phases i.e. hold, evaluate, recover andwait. ECRL, PF AL, CAL and SCRL are the most popular adiabatic logic techniques.SCRL circuits dissipate less power when compared with general CMOS logic circuit since it requires less energy.

III. PROPOSED ADIABATIC LOGIC

A. SRAM CELLS

The CMOS and FinFET based SRAM cell using SCRL adiabatic logic is implemented as shown in Figure 2 and 3 respectively. It has a latch and two access transistors similar to the typical 6-T SRAM cell but SCRL logic is used within the latch.

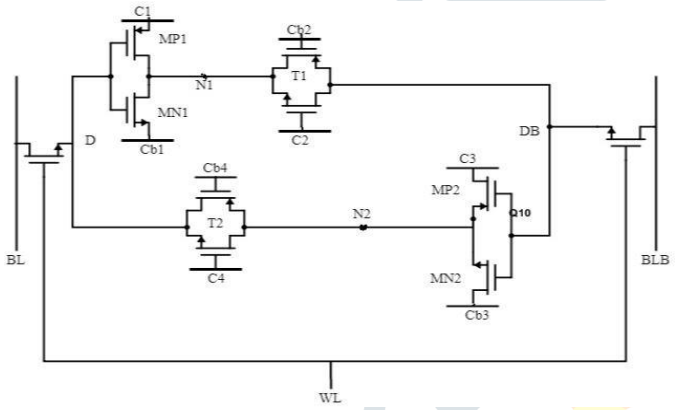

Fig2: SCRL Schematic for CMOS SRAM

MP1, MN1 and MP2, MN2 denotes the NOT gates or inverters. T1 and T2 form the transmission gates respectively.

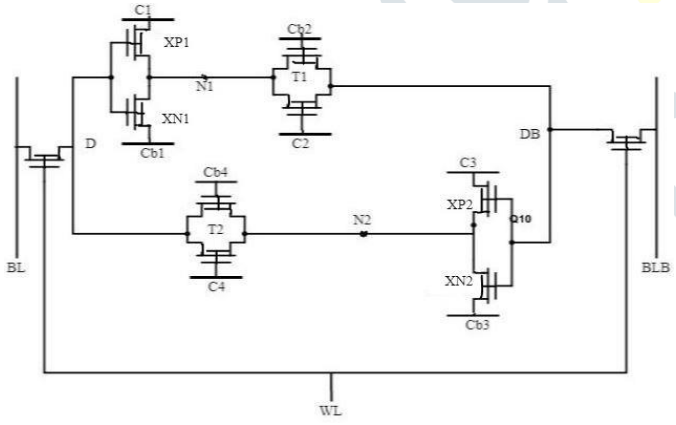

Fig 3: SCRL Schematic for FinFET SRAM

C1 and C3 acts as clock with half swing from 0 to Vdd/2 or Vdd/2 to Vdd. C2 and C4 acts as clock that has full swing i.e. 0 to Vdd or Vdd to 0. Initially internal nodes are precharged to Vdd/2. The trapezoidal Supply to the clocks is given as shown in Figure 4 for the SCRL based SRAM cell.

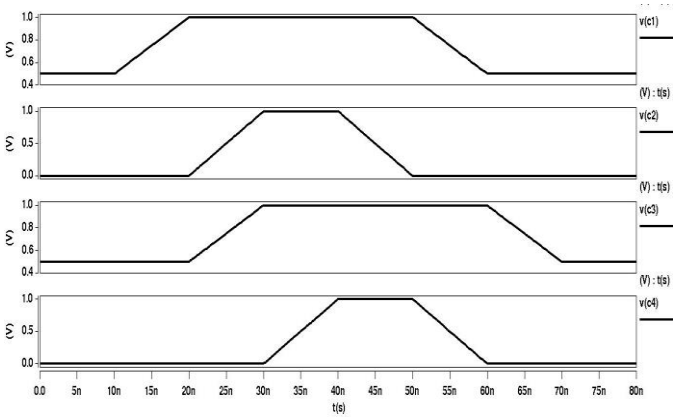

Fig 4: Trapezoidal power supply signals

Assume initially'0' is stored in the cell. When WL is 1, logic 1 is written into the through the bit line. At time t1, D increases from 0 to V_{dd} which turns ON the transistor MN1 and N1 will remain at $V_{dd}/2$. Now DBfalls from V_{dd} to 0 where N2 is kept at $V_{dd}/2$. At time t2, D is maintained at V_{dd} and clock C1 slowly increases from $V_{dd}/2$ to V_{dd}. The node N1 will follow the clock bar CB1, since the transistor MN1 is in ON. At time t3, clock C2 raises from 0 to V_{dd} by tuning ON the transmission gate [T1] and this connects the N1 and DB. Simultaneously MP2 is adiabatically turned ON and node N2 varies accordingly with clock C3. The Clock C3 gradually rises to V_{dd}. At time t4, C4 increases V_{dd} which turns ON transmission gate connecting N2 and D. At time t5, C2 is turned adiabatically off since the voltage at N2 and DB remains the same. At time t6, C1 slowly falls to $V_{dd}/2$ gradually raising N1to $V_{dd}/2$. At time t7, the transmission gate [T2] is adiabatically turned OFF by decreasing C4 to zero. At time t8, C3 falls to $V_{dd}/2$ which sets N2 at $V_{dd}/2$ where as D and DB will be used in the next stage of the cycle.

B. MONTE CARLO SIMULATION

Monte Carlo simulations works on computing results from random samples and analyze themstatistically. This simulation is similar to random experiments and to the experiments where there is no particular result.In Monte Carlo [6] simulation random samples are generated and the circuit is statistically evaluated and as the number of random samples increases, the accuracy of the results also increases.

The Monte Carlo method as a mathematical form uses a huge number of independent variables to find a definite integral of a function for an interval and the average of these dependent values and then dividing them by the interval or the size of the region for which the random samples were chosen. This varies with the typical method of approximating a definite integral. In integrated circuit (IC) design, this simulation finds applications in quantum mechanics and communications engineering.

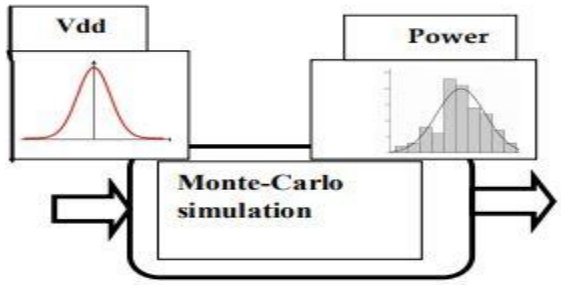

Fig5: Monte Carlo Simulation

Monte Carlo simulation is easy to implement and it also provides desired reliable results. In this Paper Monte Carlo simulation is done for the proposed circuits and results of power, energy, mean, variance, standard deviation values are tabulated.

IV SIMULATION RESULTS AND DISCUSSION

Monte Carlosimulation is performed and results are presented which demonstrates the performance of FinFET based adiabatic circuits. Average Power consumption and total energy of FinFET are compared with CMOS. Simulations are performed on HSPICE using 32nm PTM models for CMOS and BSIM_CMG models for FinFET.Figure 6shows the simulation results for CMOS based adiabatic SRAM cell.

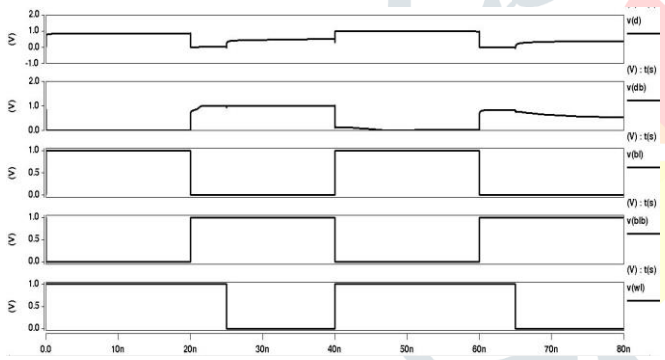

Fig 6: Output waveforms for CMOS based SRAM

Figure 7 shows the simulation results for FinFET based adiabatic SRAM cell.

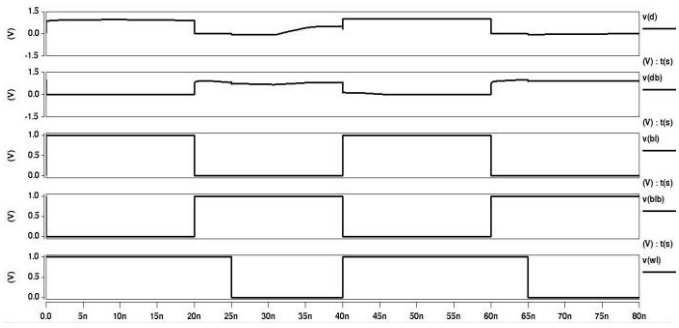

Fig7: Output waveforms for FinFET based SRAM

Table 1: Comparison of power and Energy with respect to FinFET and CMOS based SRAM

	CMOS(180nm)[1]	CMOS(32nm)	FinFET(32nm)
Total Energy (joules)	$0.37e^{-12}$	$5.996e^{-14}$	$6.00e^{-15}$
Avg. Power (watts)	$3.718e^{-06}$	$1.463e^{-06}$	$0.6155e^{-06}$

Power dissipation and total energy for CMOS and FinFET based SRAM cell are compared respectively and are shown in Table 1.

Table 2: Monte Carlo simulation results with respect to Power

	CMOS(32nm)	FinFET(32nm)
Mean	$1.463e^{-06}$	$0.6155e^{-06}$
Avg. Deviation	$4.502e^{-12}$	$0.07421e^{-12}$
Median	$1.463e^{-06}$	$0.6155e^{-06}$

Table 2 shows Monte Carlo simulation results which indicate Mean, Average deviation and Median with respect to Power.

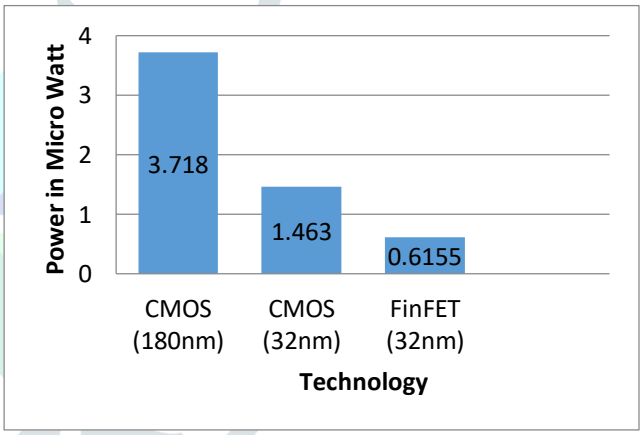

Fig 8: Power dissipation of CMOS and FinFET based SRAM (In micro watt)

This method has the advantage that it calculates the exact sample mean and an accurate numerically stable sample variance.Figure 8 shows the bar plot of Power dissipation for CMOS and FinFET based SRAM cell using SCRL adiabatic logic.

V. CONCLUSION

In this paper, simulations are performed for SRCL adiabatic SRAM cells based on CMOS (both 180nm and 32nm) and FinFET at 32nm and results compared.

Figure 8 clearly indicates 3.718uw power for CMOS based SRAM cell with 180nm and 1.463uw power for CMOS based SRAM cell with 32nm.similarly 0.6155uw power for FinFET based SRAM.Following are the conclusions for the proposed design

i. 2.5413 times less power can be achieved by replacing 180nm CMOS based SRAM cell with 32nm CMOS based SRAM.
ii. 2.37 times less power can be achieved by replacing 32nm CMOS with 32nm FinFET.

iii. There is a substantial decrease in energy dissipation of 32nm FinFET based SRAM cell as shown in table 1.

Hence, results conclude that adiabatic FinFET circuits consume less power when compared with adiabatic CMOS circuits.

REFERENCES

[1] S Dinesh Kumar, Noor Mahammad Sk., "A Novel Adiabatic SRAM Cell Implementationusing Split Level Charge Recovery Logic", 19th International Symposium on VLSI Design and Test, 2015.

[2] SudarshanPatil and V S KanchanaBhaaskaran "Optimization of Power and Energy in FinFET Based SRAM Cell Using Adiabatic Logic", 2017 IEEE.

[3] J. Montanaro, R. T. Witek, K. Anne, A. J. Black, E. M. Cooper, D. W. Dobberpuhl, P. M. Donahue, J. Eno, W. Hoeppner, D. Kruckemyer et al., "A 160-mhz, 32-b, 0.5-w cmosrisc microprocessor," Solid-State Circuits, IEEE Journal of, vol. 31, no. 11, pp. 1703–1714, 1996.

[4] Mahmoud Darwich, Ahmed Abdelgawad, MagdyBayoumi "A Survey on the Power and Robustness of FinFET SRAM", 2016 IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS), 16-19 October 2016, Abu Dhabi, UAE.

[5] K.Srilakshmi, A.V.N. Tilak, K. SrinivasaRao"Performance of FinFET Based Adiabatic Logic Circuits" 2016 IEEE.

[6] SamikRaychaudhuri Oracle Crystal Ball Global Business Unit 390 Interlocken Crescent, Suite 130 Broomfield, C.O. 80021, U.S.A. "INTRODUCTION TO MONTE CARLO SIMULATION" 2008 IEEE.

[7] Yong Moon, Deog-Kyoon, "An Efficient Charge Recovery Logic Circuit", IEEE journal of Solid-state Circuits, Vol.31, No.4 , April 1996

[8] Keval Kamdar,Aishwarya Acharya and Poonam Kadam", Low Power Multiplier Design using Adiabatic SCRL Logic" Proceedings of 2017 IEEE International Conference on Circuits and Systems (ICCS 2017).

[9] Saed G. Younis, "Asymptotically Zero Energy Computing Using SplitLevel Charge Recovery Logic," PhD thesis, 1994.

[10] Raja sekar G, Boobalan A, Ramkumar M "A Survey of Different Adiabatic Techniques for Low Power" International Journal of Advanced Research in Computer and Communication Engineering Vol. 5, Issue 3, March 2016.

[11] SobhanaTayenjam, S. R. Sriram, B. Bindu School of Electronics EngineeringVIT University, Chennai Campus Chennai, India "Design of FinFET based Frequency Synthesizer" , 2015 IEEE.

[12] Revathy.G, Abdul Razak "Design and Study of performance of nano-scale FINFETs with reduced switching energy using spacer Optimization" 2015 IEEE.

[13] Pathak Jay Electronic Engineering Dept. SVNIT, Surat, INDIA Email: A. D. Darji Electronic Engineering Dept. SVNIT, Surat, INDIA" Analysis of the Source/Drain Parasitic Resistance and Capacitance depending on geometry of FinFET", 2015 IEEE.

[14] A. N. Bhojand N. K Jha, "Parasitics-aware design of symmetric and asymmetric gate-workfunctionFinFET SRAMs," IEEE Trans. on VeryLarge Scale Integration (VLSI) Systems, vol. 22, no. 3, pp. 548-561, Mar. 2014.