Power Line Communication based Design for Testability for a CMOS Receiver

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***Abstract*—The internal nodes of circuit become less accessible as the complexity of the circuit increases, due to less number of I/O pins available for access. To overcome this problem at IC Level, we propose power line communication (PLC) that uses the dual power pins for distribution of power in networks for application/ observation of test data. This design ensures robust operation in addition to good data speed under variations and droops of the supply voltage. The PLC receiver is designed and verified in CMOS 0.18µm technology with a supply voltage of 1.8 V using Synopsys HSPICE Tools. The measurement results show that the receiver can tolerate a voltage drop of up to 0.22V for a data rate of 10Mb/s. The power dissipated by the receiver is decreased by 26.5% under 1.8 V supply, and the delay is reduced by 56.76% over the existing design.**

Keywords—Power Line Communication; Power Efficient CMOS PLC receiver; Power Consumption; Stacking Method.

I. INTRODUCTION

Today's VLSI technology is advancing in such a way that the designers can incorporate a large number of functions inside a chip. Microprocessors are one of the best examples for this. Day by day the size of ICs reduces and the operations it can perform are increasing. So many challenges still exist such as, the need of proper provision for the thermally generated heat removal, the number of the input output pins that an IC needs, proper power supply injection etc., due to which there exists limits on incorporating functions inside ICs. Also routing inside the IC too has a major role in it.

There should also be the provisions in ICs like sensors to detect what is happening inside each and every point and if anything happens wrongly, the normal state have to be recovered. Even though the increase in system complexity is an advantage in the sense that the size of ICs can be reduced, with that there should be new inventions for proper data passage inside the same.

Recent advancements in silicon processing technologies allows as many as nine copper metal layers can contain 3.1 billion transistors as in Intel Itanium® processor in 32 nm CMOS technology.

In high level of integration, the limiting factors in packaging are thermal heat removal, I/O pin count, stable power supply requirement, large power consumption, etc. As the number of functions increase, the available less number quantity of I/O pins imposes challenges to IC designers. The increase in system complexity and decrease in reliability requires monitoring the internal state of the chip especially in deep sub-micron silicon technologies[1].

The control of the individual sensors requires dedicated pins and routings which are expensive in terms of cost and design hours.

The power flows to any internal node of a chip through power distribution network (PDN) for which the use of power pins for a a dual purpose is highly attractive for data communications[2][3]. It saves pins and routing of the data signals to the internal nodes, particularly attractive to control a adequate number of sensor nodes, which does not require a high data rate. Also it offers flexibility on placements of sensor nodes without careful preplanning as there is no need for routing, hence this design opens up possibilities for fault diagnosis, transient logic values monitoring during built-in self-test and for on-line/off-line testing[4].

In power line communication, it efficiently uses the power distribution networks inside ICs since they are the only components that reach each and every node. So if there have a provision to pass the test data, which are used for fault diagnosis, scan design etc. to whichever areas we need to apply the test that will be an attractive way of communication in ICs, So that the routing overhead inside the ICs to pass these testing data can be intelligently avoided. So in PLC, the power distribution networks are used for power delivery and also data communication.

The test data are superimposed on the power signal and are transmitted through the power distribution networks of ICs rather than the separately allotted routing paths. Also the number of power pins can be reduced since there is no need to carry the test data through the input pins. Of course, adopting such a power line communication always has to overcome the extreme noise level at the power lines. So there should be effective methods to overcome the same.

Essentially there is the need of receivers at each and every node to extract these data signals efficiently from the power lines. Many variants of the same already exist, but a power efficient design is not yet met. Why the receiver should be power efficient is because, otherwise if each unit of receiver consumes such huge power, the overall power consumption of the entire chip will increase by a large value, which is hard to afford.

The Power line communication (PLC) system achieves communications between an external control module and one or multiple internal nodes of an IC through the power distribution network. To reduce the cost of complex ICs, the number of pins can be reduced that are used to control internal nodes.

The external transmitter present in PLC superimposes the data on the power supply to send the data through the power pin(s) and the power distribution network of the IC to an internal node(s), without affecting the performance of the

chip. The PLC receiver at an intended node will be now able to extract the data from the power distribution network. Each receiving node has a pre-assigned unique identification code, which enables the data to be delivered to the intended node(s).

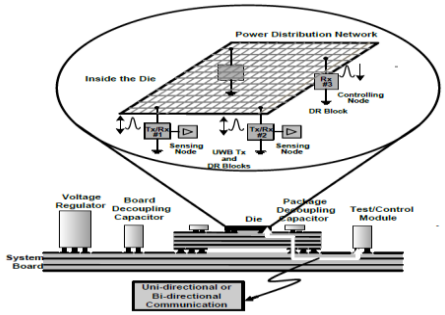


Figure 1. VLSI Circuit for a Power line communication system [5]

Figure 1 shows a PLC system for a Very Large Scale Integration circuit environment. The Test/Control module sends data superimposed on a power line of the system board. The signal travels via power pin(s) to the power planes of a package, and finally through the power distribution network and reaches at the intended node(s). The channel characteristics of the power distribution network of a target IC are important to select proper frequency bands.

Few PLC receivers are developed using CMOS technology by Dr. Dong S. Ha's team [8]-[10], which suggested the possibility of power line communications in ICs. The 0.18μm CMOS PLC receiver contains a sensing circuit, a differential amplifier with an offset cancellation, and a positive feedback latch as proposed by Thirugnanam et al. in [8]. The DC voltage of the signal is removed by the offset cancellation which is based on a fixed bias voltage that is highly sensitive to supply voltage fluctuations [13][14].

The 0.13μm CMOS PLC receiver capable of coherent detection using ultra wideband (UWB) data signals was proposed by Chawla et al. in [9], which achieves a higher sensitivity than the existing designs, but higher circuit complexity results in large power dissipation [15][16]. Also it relies on a fixed bias voltage to remove the DC voltage from the signal transmitted by PLC [11][12].

This paper is organized to describe existing designs in section II, proposed design in section III, the corresponding results are discussed in section IV and finally section V concludes the paper.

II. Existing PLC Receiver Design

In literature, there exist many designs that are developed at the earlier stages at 0.18μm CMOS technology. Figure 2 represents the PLC Receiver deisgn proposed by proposed by R. Thirugnanam in [6]. It comprises of a sensing circuit, a differential amplifier, and a latch. The sensing circuit is a simple common source with diode connected load that detects the transmitted signal in the power line and down shifts the DC level of the signal to a lower value.

The output of the single ended sensing circuit is applied to a differential amplifier. One input of the differential amplifier is connected to a constant reference voltage, and the other input to the drains of M3 and M4 whose gates are connected to the clock signal. When the clock signal is low, the input of the differential amplifier and the output of the sensing circuit are interconnected, and the amplifier amplifies the sensed signal and compares it with the reference signal. When the clock is high, M3 is off and M4 is on, the amplifier disconnects from the sensing circuit, and the M5 acts as diode with resistance 1/gm[7][17].

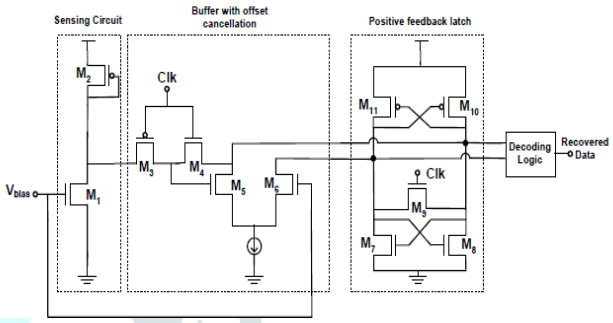


Figure 2. PLC receiver proposed by R. Thirugnanam

This PLC receiver has a shortcoming that the offset voltage at the output of the differential amplifier is directly affected by the fluctuation of the supply voltage. The offset voltage may pull up or down the latch according the fluctuation of the supply voltage to disrupt the operation. Also, the turn-on resistance associated with M3 weakens the strength of the output signal which reduces the sensitivity of the receiver.

The PLC Receiver block diagram proposed by V. Chawla's receiver is shown in Figure 3. The receiver comprise of a sensing and amplifying circuit along with a merged mixer integrator and a comparator. The sensing circuit senses and amplifies impulse data on the power line, while shifting down its DC level. A merged mixer-integrated circuit correlates the received signal with a template signal generated by a template generator. The output of the merged mixer-integrator is applied to the comparator, which translates the sensed pulses to logic values.

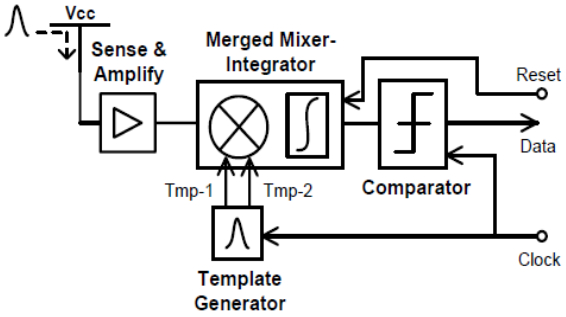


Figure 3. PLC receiver proposed by V. Chawla

Figure 4 shows the sensing and amplifying circuit. It is simply a cascaded two stage of the differential amplifier. One of the inputs of the first amplifier is connected to the supply voltage, and the other one connected to a RC filter tied to the supply voltage. The filter extracts the DC voltage of the impulse signals superimposed on the power lines [18].

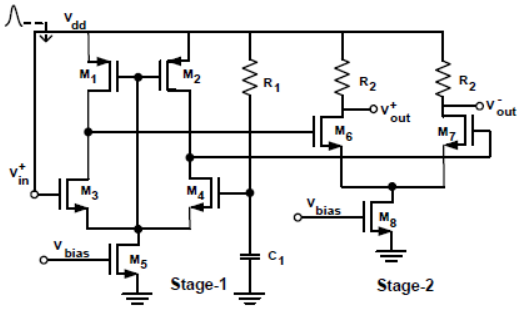


Figure 4. Sensing and amplifying circuit proposed by V. Chawla

The merged mixer-integrator circuit is shown in Figure 5. The circuit consists of two single-balanced mixers with cross-coupled outputs. The mixer outputs are loaded with capacitors C1 and C2. The transconductors (M15 and M16) at the bottom of the two single-balanced mixers are driven by two similar, but time separated, template signals. The template signals are digital impulses generated by Template Generator[19].

Binary amplitude shift keying (ASK) modulation is adopted for our PLC receiver. Binary ASK is attractive for low data rate systems due to simple modulation and demodulation schemes, which lead to low power consumption. To achieve the bit error rate of 10^{-6}, the binary ASK (in which M=2) requires more than 11.0 dB of Eb/No.

The symbol rate is equal to the bit rate for binary ASK. At the same time, the data signal should not be excessive to maintain the integrity of power supply. Adoption of an error correction scheme is a solution to meet the both requirements.

An ASK demodulator consists of three stages, an envelope detector, an average detector, and a comparator. ASK demodulator circuits can be classified into voltage-mode, current-mode, and mixed-mode. An inverting amplifier amplifies the voltage of the received signal, and the modulated signal is reconstructed by the OR gate. The low-pass filter removes the noise and extracts the envelope from the carrier, and the comparator recovers the digital data based on the threshold voltage. A voltage-mode ASK demodulator has a lower circuit complexity compared with the other two modes as it does not require a conversion between voltage and current.

The data is represented as the branch current for a current-mode ASK demodulator. The modulated signal is rectified by the current mode squarer with a small impedance, and the carrier signal is eliminated using a 3rd -order Gm-C low pass filter. A level detector extracts the digital data from the envelope information. The data for a mixed-mode ASK demodulator is represented in both nodal voltage and branch current, which intends to benefit the advantages of both modes. The operational transconductance amplifier (OTA) converts the input voltage into current, and the current mode envelope detector. The current level detector translates the current into digital values.

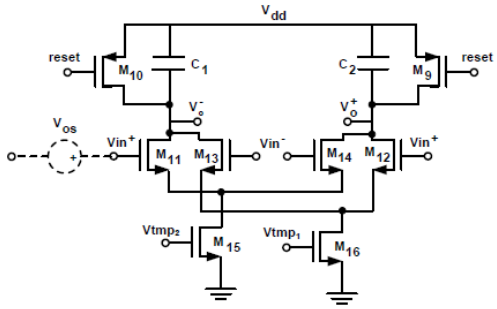


Figure 5. A merged mixer- integrator circuit proposed by V. Chawla

The comparator circuit shown in Figure 6(a) converts the impulses into digital. It has an input gain stage and a regenerative latch stage. The input stage comprises of M17–M21, where M17 and M18 are input transistors and M19 and M20 are included to minimize static current of the input stage. A regenerative latch is back-to-back inverter pairs. The template generator circuit diagram is shown in Figure 6(b). One of the inputs to the NOR gate is inverted and the other input is non-inverted due to the introduction of the inverter. Every time the input switches from logic-1 (Vdd) to logic-0 (0), a glitch is generated at the output (Vtmp), which serves as the reference waveform for the correlation.

The glitch duration can be adjusted by varying the delay between the two inputs of the NOR gate by using switched capacitor bank 2. A reference is generated at every clock transition from 0 to Vdd. The switched capacitor bank 1 synchronizes the template waveform with the received impulse by controlling the delay[20].

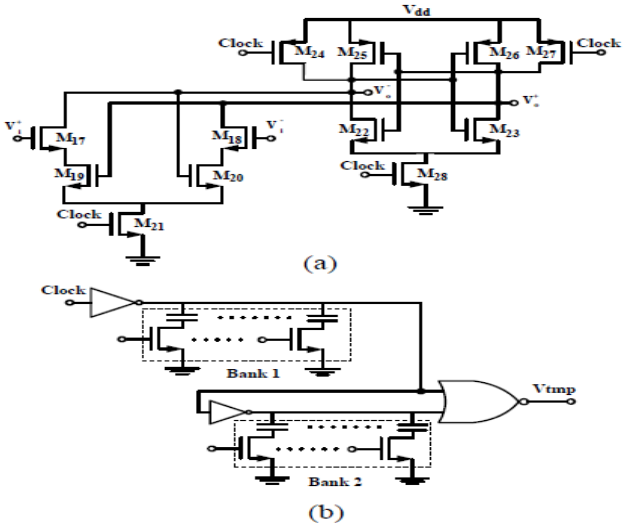


Figure 2.6: (a) A comparator circuit and (b) A template generator circuit proposed by V. Chawla

The focussed advantage of figure 2.6 PLC receiver is that it can mitigate the voltage fluctuation effectively. However, the receiver is complex to consume large power, notably use of two differential amplifiers for the sensing stage and the merged mixer-integrated in the second stage. Also, the presence of several number of transistor for the PLC contributes more noise on the input of the comparator, which is rather sensitive to the noise due to adoption of one threshold voltage.

III. PROPOSED PLC RECEIVER

Figure 7 shows the proposed PLC receiver block diagram. It consists of three blocks, namely, signal extractor, level shifter and logic restorer. The level shifter reduces the DC level of the superimposed signal, so that the level-shifted signal can be processed by the following signal extractor where the signal gets amplified in order to yield a differential signal. The Schmitt trigger based logic restorer extracts the logic values from the obtained analog signal. The logic restorer has a differential input and translates the sensed analog signal into a logic value based on the threshold of its hysteresis.

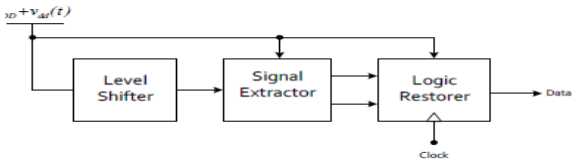


Figure 7. Block diagram of the proposed PLC receiver

The internal CMOS circuits of proposed PLC Receivers are shown in figures 8,9,10.

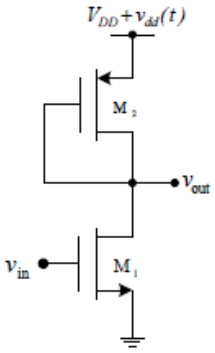


Figure 8. Level Shifter

The level shifter is designed by using a common source amplifier with a diode connected load that is capable of propagating the data signal *vdd*(t) imposed on the supply voltage VDD to the output, while reducing the signal *vdd*(t) DC voltage level to one half of VDD.

$$\text{PSRR}=-\frac{g_{m1}}{g_{m2}}=-\frac{\mu_n\left(\frac{W}{L}\right)_1\left((V_{gs}-V_{th})\right)_1}{\mu_p\left(\frac{W}{L}\right)_2\left((V_{gs}-V_{th})\right)_2}$$

The above equation shows that the PSRR can be reduced through a small W/L and a small overdrive voltage present for M1 and a large (W/L) and a large overdrive voltage of M2.

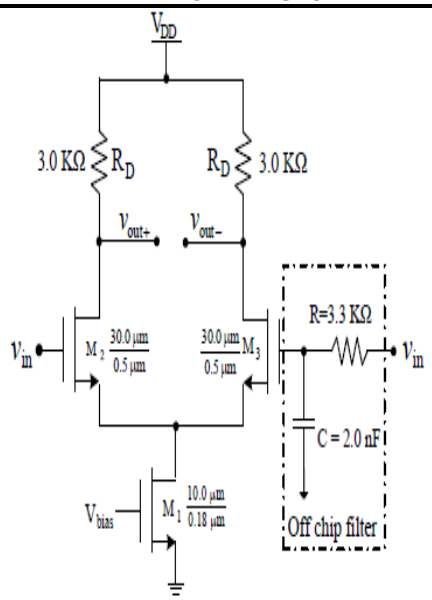


Figure 9. Signal Extractor

The output of the level shifter is the data signal with a DC value of 0.5VDD from which the signal is amplified and removes the DC Voltage from the signal. It is a differential amplifier where one input is from RC low-pass filter, which extracts the DC value of the signal, which can possibly vary or fluctuate, while removing the signal ideally. The differential amplifier will also convert a single-ended input into a differential output. The voltage gain of this differential amplifier can be represented as below.

$$A_V = -g_{m2/3}R_D$$

Where g_{m2} =$g_{m3}$and can be expressed as $g_m = \mu C_{ox}\left(\frac{W}{L}\right)(V_{gs}-V_{th})$.

Figure 10 shows the logic restorer which contributes to a great part to enhance the noise immunity of designed system. It is a differential Schmitt trigger based circuit with tunable hysteresis [2] property. The focussed advantage of using a differential Schmitt trigger is that, it is excellent in handling the situations of extreme noise and disturbances.

The components that contribute to the hysteresis are the symmetrical loads and the pair of cross coupled inverters. Stacking method is incorporated in the pair of cross coupled inverters to reduce the power consumption considerably. Each transistor in the normal cross coupled inverter pair is replaced by four transistors each having a width of W/4 and due to which the leakage power reduces by a greater extent.

By adjusting the currents through the symmetrical loads, the regenerative feedback mechanism of the pair of cross coupled inverters can be adjusted to control the hysteresis property. Symmetrical loads are selected to achieve the linearity. According to the application of the data signals, the clock signals switches and thus the currents applied to this differential amplifier will also change. It simply adjusts the deviation between the low and high threshold voltages and hence enhances the immunity to noise of the receiver.

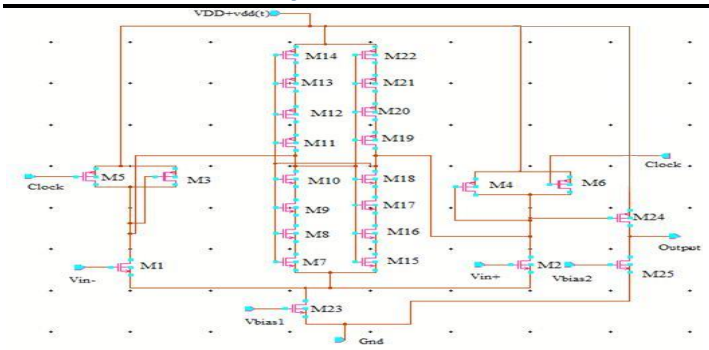


Figure 10. Logic Restorer - 1

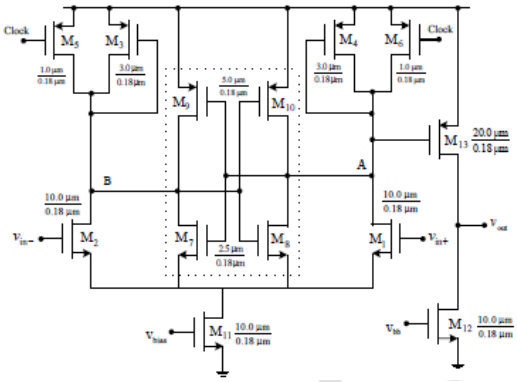


Figure 11. Differential schmitt trigger with tunable Hysteresis based Logic Restorer – 2

The Schmitt trigger based Logic Restorer, shown in figure 11 shows that the hysteresis through the regenerative feedback circuit, which is a pair of cross-coupled inverters. The transistor size of the inverter pair, specifically M7, and M8, are smaller compared with M1 and M2, so that transistors M1 and M2 have more influence on the current. When a new date signal is applied to the logic restorer, the clock is turned to high to turn off M5 and M6 (which are voltage controlled current sources).

The pair of cross-coupled inverters goes into a high or low state and the logic restorer output is interpreted as a logic value according. Then, the clock signal becomes low, the transistors M5 and M6 are turned on to active state. The difference between the high and the low switching voltages of the Schmitt trigger becomes wider due to the additional current supplied by the two transistors. Hence, it requires a larger differential voltage to change the state of the inverter pair, which increases the immunity to noise and disturbances.

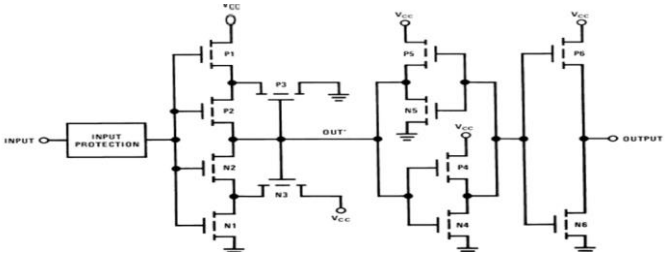


Figure 12. Logic Restorer - 3

The logic restorer - 3 as shown in figure 12, has a standard input protection at the input of the Schmitt trigger which is also connected to the gates of four stacked devices. It uses two P-channel MOSFETs and two N-channel MOSFETs. The transistors P3 and N3 operate as source followers which introduce hysteresis due to feedback from the output voltage, out'. When the input is at logic-0 (0V), the transistors P1 and P2 are turned ON, and N1, N2 and P3 are turned OFF. Since out' is logic high, N3 is turned ON and acts as a source follower then the drain of N1 i.e., the source of N2, is now at $V_{CC} - V_{TH}$.

If the input voltage is up by one threshold above ground, then the transistor N1 begins to turn ON, N1 and N3 both being turned ON combine to form a voltage divider network biasing the source of N2 at roughly half the supply. When the input is a threshold is greater than 0.5 times that of VCC, then the transistor N2 begins to turn ON and regenerative switching starts to occur. Any increase in voltage on the input causes out' to drop, then the source of N3 follows its gate, hence out' influences N3 in the voltage divider that makes out' nearer to logic - 0. Meanwhile P3 starts to turn ON, which makes its gate to logic low by the rapidly dropping out'. The transistor P3 turns ON which brings the source of P2 active low and turns OFF the transistor P2 and hence out' becomes logic - 0.

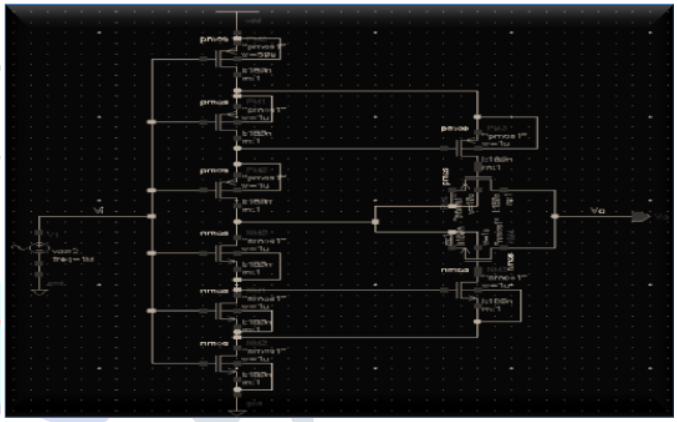


Figure 13. Logic Restorer - 4

The Schmitt trigger based logic restorer circuit-4 is shown in Figure 13 and the corresponding aspect ratios are P1,P4 and P5 are 50/0/18µm and the P2, P3, N1, N2, N3, N4and N5 are 1/0.18µm. The circuit consists of an inverter and eight transistors.

When the enable signal is high, then the transistors P1 and N1 is ON, and the applied input sinusoidal waveform is larger than the threshold voltage then transistors P2, P3 are OFF and transistors N2, N3 are ON. Then the transistors P5 and P4 are ON and OFF respectively, while the transistors N2, N3, N4 and N5 are ON by switching the output voltage to low. Similarly, when the enable signal and the applied input waveform are low, then the output voltage has shifted to high. By switching transistors P1, P2 to OFF and ON, P3, P4, P5 are switched into ON, OFF, ON and OFF and the transistors N1, N2, N3, N4 and N5 are OFF.

The Schmitt trigger based logic restorer circuit-5 is shown in Figure 14 and the correspond their aspect ratios are P1 is 50/0/18µm, P2 is 0.4/0.18µm, P3 and N4 are 10/0.18µm, P4 and N3 are 1/0/18µm and N1 and N2 are 2/0.18µm. The circuit consists of an inverter and eight transistors. The inverter inverts the given pulse waveform for enabling the multiplexer to work satisfactorly.

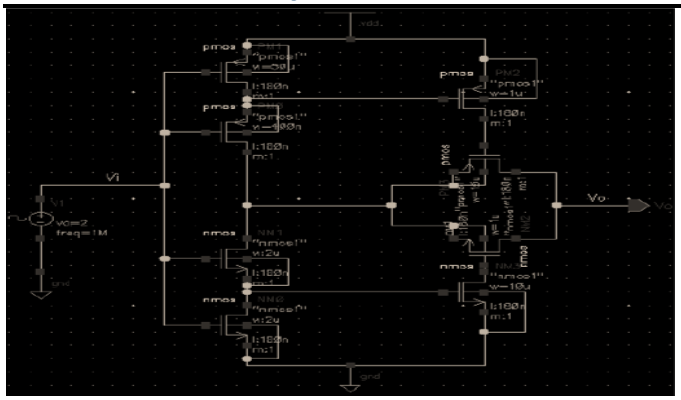


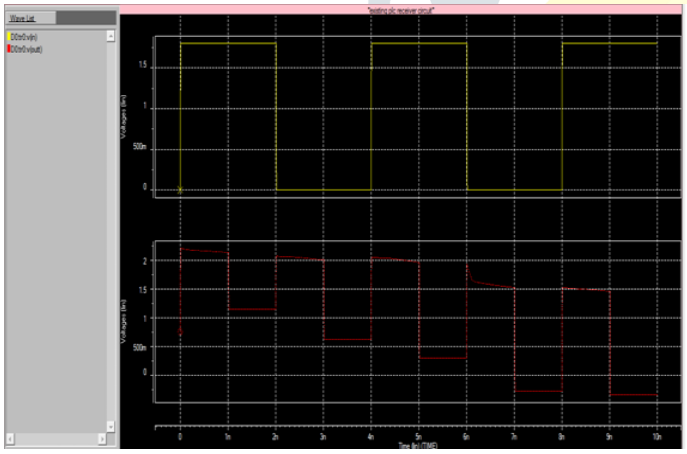
Figure 14. Logic Restorer - 5

When the enable signal is high, then the inverted signal is connected to transistor P1 by switching of into ON condition and the non inverted signal is connected to N1 by switching of into ON condition. When the applied sinusoidal input waveform is larger than the threshold voltage then the transistors P2 is turned OFF and N2 is turned ON.

The transistor P4 is ON because of the input voltage of P2 is greater than the voltage of pulse input of P1. By this the transistor P3 is OFF and the transistors N1, N2, N3, and N4 are ON. When the enable signal is high the output voltage switches to low. Comparably when the enable signal is low, then the output is high by switching transistors P1, P2 are OFF and ON. The transistors P3 and P4 are ON and OFF respectively. And transistors N1, N2, N3 and N4 are OFF.

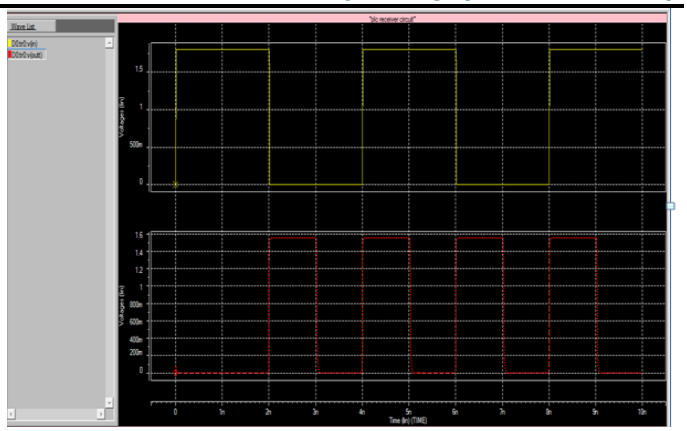
IV. Results and Discussion

The designs for the PLC Receiver are simulated in HSPICE Synopsys Tools using SPICE Coding. The output signals of the PLC Receiver design with various logic restorers are shown in figure 15 to 19.



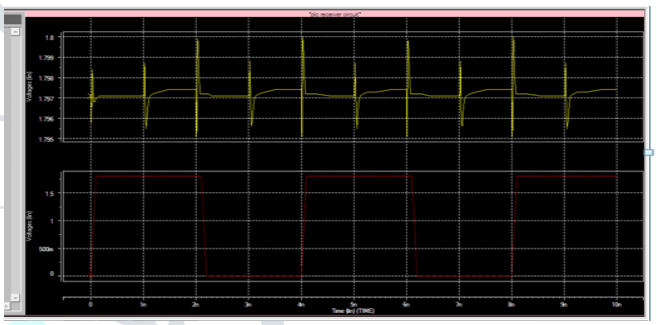
Fgure 15. Input and Output waveforms of PLC Receiver using Logic Restorer – 1

Figure 15 shows the waveforms of input and output of the PLC Logic Restorer-1, where the input is given as 1.8V maximum but the output is unstable with varying potential between -5V to 2.3V.



Fgure 16. Input and Output waveforms of PLC Receiver using Logic Restorer – 2

Figure 16 shows the waveforms of input and output of the PLC Logic Restorer-2, where the input is given as 1.8V maximum but the output is stable with a time lag of 2ns and the maximum potential is 1.6V.



Fgure 17. Input and Output waveforms of PLC Receiver using Logic Restorer – 3

Figure 17 shows the waveforms of input and output of the PLC Logic Restorer-3, where the input is given as 1.8V maximum but the output is unstable with spikes generated near the transitions of signal in power lines and the potential obtained is around 1.7V.

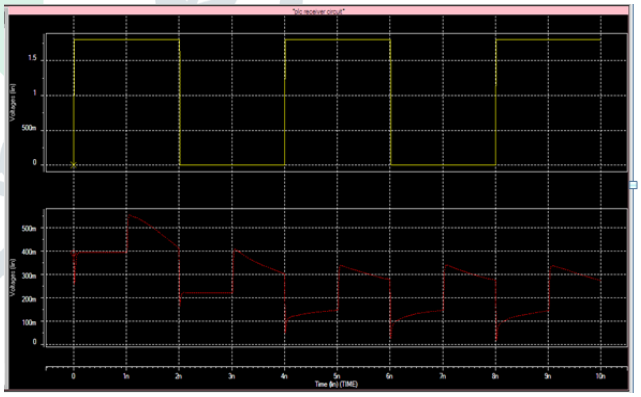
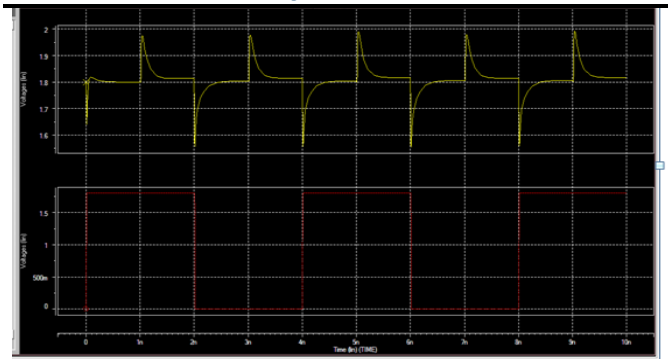


Figure 18. Input and Output waveforms of PLC Receiver using Logic Restorer – 4

Figure 18 shows the waveforms of input and output of the PLC Logic Restorer-4, where the input is given as 1.8V maximum but the output is unstable and the maximum potential is 600mV. This design is well suited for low power high speed applications.

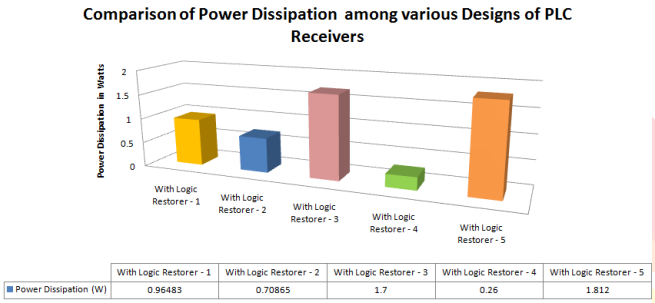


Fgure 19. Input and Output waveforms of PLC Receiver using Logic Restorer – 5

Figure 19 shows the waveforms of input and output of the PLC Logic Restorer-5, where the input is given as 1.8V maximum but the output is stable and the maximum potential is same as that of input i.e., 1.8V.

The output is stable only for PLC Receiver with logic restorer 2,3 and 5. But still amog them the logic restorer 5 is more stable and has less delay than the receiver with other two circuits.

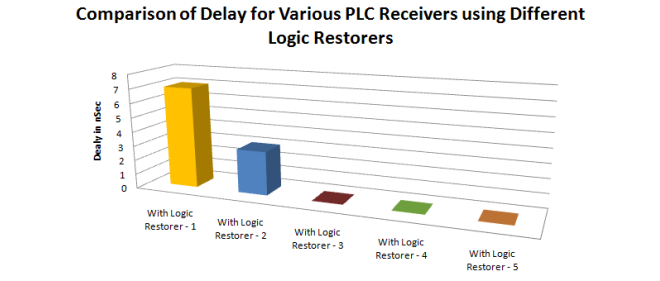
The simulated values of various PLC Receivers with different Logic Restorers are shown in figure 20, 21 and 22.



	With Logic Restorer - 1	With Logic Restorer - 2	With Logic Restorer - 3	With Logic Restorer - 4	With Logic Restorer - 5
Power Dissipation (W)	0.96483	0.70865	1.7	0.26	1.812

Figure 20. Comparison of Power Dissipation of various PLC Receivers

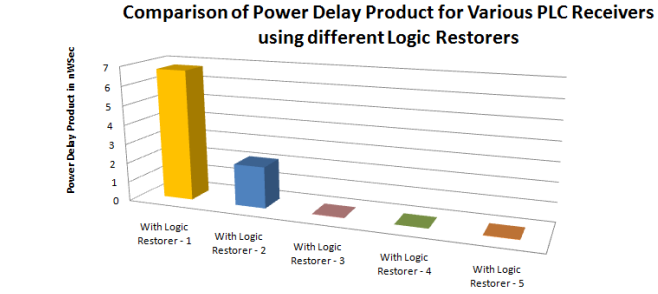
From figure 20, the power dissipation of PLC Receiver with Logic Restorer – 4 is minimum which is 73% less than that of with Logic Restorer-1, 63.3% less than that of with logic restorer-2, 84.7% less than that of with logic restorer-3 and 85.65% less than that of with logic restorer-5.



	With Logic Restorer - 1	With Logic Restorer - 2	With Logic Restorer - 3	With Logic Restorer - 4	With Logic Restorer - 5
Delay (nSec)	7.014	3.034	0.013	0.006	0.01

Figure 21. Comparison of Delay of various PLC Receivers

From figure 21, the delay of PLC Receiver with Logic Restorer –4 is minimum which is 99.9% less than that of with Logic Restorer-1, 99.8% less than that of with logic restorer-2, 53.8% less than that of with logic restorer-3 and 40% less than that of with logic restorer-5.



	With Logic Restorer - 1	With Logic Restorer - 2	With Logic Restorer - 3	With Logic Restorer - 4	With Logic Restorer - 5
Power Delay Product (nWsec)	6.7673	2.15	0.0221	0.00156	0.01812

Figure 22. Comparison of Power Delay Product of various PLC Receivers

From figure 22, the power delay product of PLC Receiver with Logic Restorer–4 is minimum which is 99.9% less than that of with Logic Restorer-1, 99.9% less than that of with logic restorer-2, 92.9% less than that of with logic restorer-3 and 91.3% less than that of with logic restorer-5.

V. Conclusion

The use of the power distribution networks of ICs for data communications as well as delivery of power. This work intends to improve previous PLC receivers with three major design objectives, mitigation of the supply voltage fluctuations and droops, improving the noise immunity, and reducing power dissipation. The PLC receivers have advantages like reduced number of I/O pins, greater reliability, etc. But still certain disadvantages like operation constraints due to alignment error, high sensitivity for low power design, difficulty in installing for long distances, etc. They find applications in many areas like Automatic Meter Reading, Building Automation, Heating Ventilation and Air Conditioning (HVAC), Home Automation, Industrial Automation, Lighting Control, Remote Monitoring and Control, Sensor Control and Data Acquisition, Security Systems/Keyless Entry, Smart Grid, etc and many more. The PLC receiver comprises of three blocks i.e., a level shifter that reduces the offset voltage to approximately 0.5VDD, a signal extractor i.e., a differential amplifier that extracts the superimposed data signal on the power line and the input connected via a RC low-pass filter is used to mitigate the supply voltage fluctuations and droop. The last sub-block is the logic restorer which obtains the digital logic values of the differential signal. The Schmitt trigger configuration helps in improving the noise immunity of the receiver. The designs are developed in 0.18µm CMOS technology using SPICE coding and are simulated in HSPICE Synopsys Tools operating at 1.8V. The results show that the PLC receiver can tolerate the supply voltage drop by 0.42 V or 24%. Three parameters power dissipation, delay and figure of merit i.e., power delay product are compared for various PLC receivers with different logic restorers. Among them Logic Restorer – 4 proved to be a best choice for implementation.

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