Performance analysis of a pulse-triggered D-flip-flops design for ultra-low power applications

[1]N.N.S Hima Bindu, [2]T. Gowri
[1] Post Graduate Student, Department of ECE, GITAM (Deemed to be University)[2] Assistant Professor, Department of ECE, GITAM (Deemed to be University)
[1]himabindu614@gmail.com,[2] gowri3478@gmail.com

Abstract*— In this paper, a novel architecture is presented for the pulse-triggered D-Flip-Flop in the CMOS 250nm technology. This novel architecture utilizes a transmission gate to control the input data and leakage power. The pulse generator is also modified to reduce the number of required transistors and the clock pulse delay. In addition, pull-up PMOS transistor is controlled by input data to reduce the power dissipation. The proposed architectures have improvement in terms of different architectures that are implemented using 250nm technology to reduce the power delay performance in comparison with different D-Flip-Flop architectures. The proposed D-Flip-Flop architectures are simulated using Top Spice. By using mobile applications, we can implement these architectures in cadence using 90nm technology.

Index Terms*— clock pulse delay, Delay performance, leakage power, Pulse-triggered flip-flops, power dissipation, Transmission gate*

I. INTRODUCTION

Nowadays in digital circuit design, the basic elements are Flip-Flops which are used extensively. This problem converts more significant while facing IC's. Flip- Flops can be clocked (synchronous) or simple (asynchronous). The simple ones are commonly described as latches, while the flip-flops were described for clocked ones. Around a lone pair of cross- coupled inverting elements, simple flip flops can be built. Except at the transition of a dedicated clock signal clocked devices ignore their inputs. So, such devices are specifically designed for synchronous systems.

Latches and Flip-Flops are utilized as the data storage elements. Flip-Flop is a device which stores a single bit of data. One of the two states represents "one" and the other state represents "zero". For storage of state such data storage can be used and such a circuit is labeled as sequential logic in electronics. When it is used in FSM (finite state machine), the output and next state not only depends on its current input, but also on its current state. It is also used for synchronizing input signals and counting of pulses.

There are mainly three groups of Flip-Flops. They are: (1) Pulse Triggered- Flip-Flops, (2) Transmission Gate Flip-Flops, (3) Master Slave Flip-Flops. PT-FFs are usually used because of its single-latch architecture, speed and low power consumption. Based on the pulse generator PT-FF's are divided into two groups. 1) Implicit PT-FFs – here the latch contains pulse generator, 2) Explicit PT-FFs – these are more efficient when it comes to power, but its speed is lower than implicit.

Mainly to trigger the latch, the triggering pulse is used in the PT-FFs. PT refers data that enter into flip-flop on the rising edge of the clock pulse, but the output does not reflect the input state until the falling edge of the clock pulse. As this type of flip- flops are sensitive to any of change in the input

levels during the clock pulse is HIGH, the inputs should not be changed before the falling edge and must be kept prior to the clock pulse's rising edge. A Transmission gate is a combination of a PMOS and a NMOS pass gate in parallel. Combining NMOS and PMOS logic lows and highs well produces a transmission gate that passes both logic levels efficiently.

The combination of two JK flip-flops connected together in a series configuration is known as Master-Slave Flip-Flop. In these, one acts as **"**master**"** and other one acts as a **"**slave**"**. The output of the master flip flop is connected to the two inputs of the slave flip flop and its output is fed back to inputs of the master flip flop. From results it is clear that due to the proposed D-Flip-Flop architecture, the Power Delay Performances (PDPs) has been improved compared to other D-FF architecture.

II. PROPOSED ARCHITECTURES

2.1 Conventional PT-Flip-Flop architectures

Mainly the conventional PTFF's are generated into different architectures that are to be shown. These architectures have some unique advantages and disadvantages.

2.1.1 The Utilized ep-DCO Flip- Flop Architecture:

The utilized explicit PTFF (ep-DCO) Fig.1 design is based on NAND logic topology. Power consumption of the device is a little improved due to connecting MP1 to the Pulse clock. This improvement is because of the reduction of ON time of MN2 transistor. When MN2 transistor is connected to the Pulse clock, [1] it can reduce the time in which this transistor is in ON state. Therefore, the current dissipation of the device too would be reduced. The inverters I1 and I2 are consumed to continue node X value. The critical path of this circuit comprises three transistors. Therefore, this design grieves from a long delay time in "0" to "1" transition. Another drawback of the ep-DCO architecture is that in every rising edge of the clock, the node X is discharged through MN1 and MN2 transistors, in [8] without considering the value of data signal. This is due to the fact that the input data must pass through MN1 and MN4 and the clock pulse must turn transistor MN3 ON to change the value of node Q [7]. This issue would result high power consumption for the ep-DCO architecture.

2.1.2 The Utilized Conditional- Discharge Flip-Flop Architecture:

In different method we have used to improve the design performance Fig. 2 shows an improved design, which solves

the periodic discharge problem taken in the previous model. This architecture is called Conditional-Discharge Flip-Flop architecture. In this architecture, a Conditional Discharge (CD) path is added to reduce the power consumption. By adding transistor MN3 to the input, [2] the conditional discharge path is created. The transistor MN3 of this architecture is connected to the Q-feedback and unless the value of the output changes, the node X is not going to be discharged. Moreover, in the CDFF architecture, to hold the value of node X, this design uses just one inverter and a P-MOS transistor, instead of using two inverters. This improvement simplified the design topology and it also decreased the power consumption. This design also suffers from a long delay when the output state transits from logic "0" to "1". This technique can be used in implicit type of flip-flop design. The semi-dynamic design of these flip-flops provides different internal power dissipation in [6] based on the input data distribution as compared to a fully static master slave flip-flop.

2.1.3 The Utilized Static Latch Conditional-Discharge Flip-Flop Architecture:

In this architecture it is very similar to CDFF architecture, but the only difference between these two designs is that SCDFF uses static latch [3]. Therefore, node X is not discharged periodically. This static latch reduces the power dissipation of the D-FF. However, it would result in a longer delay in data-to-Q feature is shown in Fig. 3.

2.1.4 The Utilized Modified Hybrid Latch Flip-Flop Architecture:

In this architecture the modified hybrid latch flip-flop is known as MHLFF and this is a type of implicit type flip-flop. MHLFF shown in Fig. 4 an improved P-FF design and it employs a static latch structure. The power consumption of this design is improved, [4] but this design suffers from a long delay in "0" to "1" transition. The special technique used in this design for reducing the power consumption of FFs is in the pull-up transistor, which is connected to the output (Q) to maintain node X value, but at the same time, [5] this would result in a longer delay in case of output transition from "0" to "1". It is because, node X is not pre-discharged.

2.2 Approach

The block diagrams of different flip-flop architectures are shown in figures.

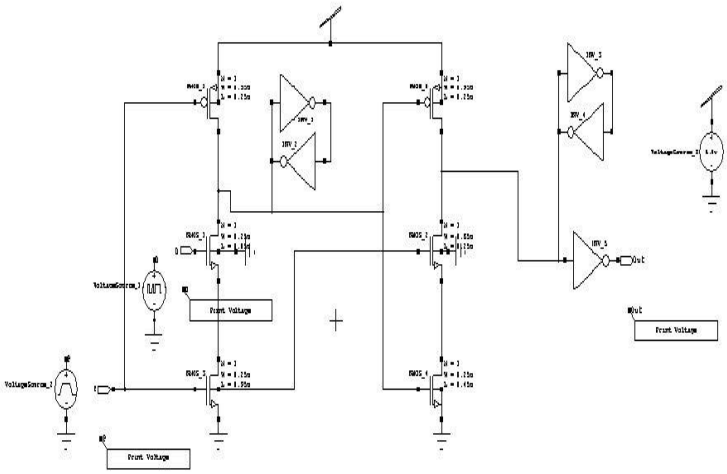

Fig. 1. The utilized ep-DCO Flip-Flop architecture.

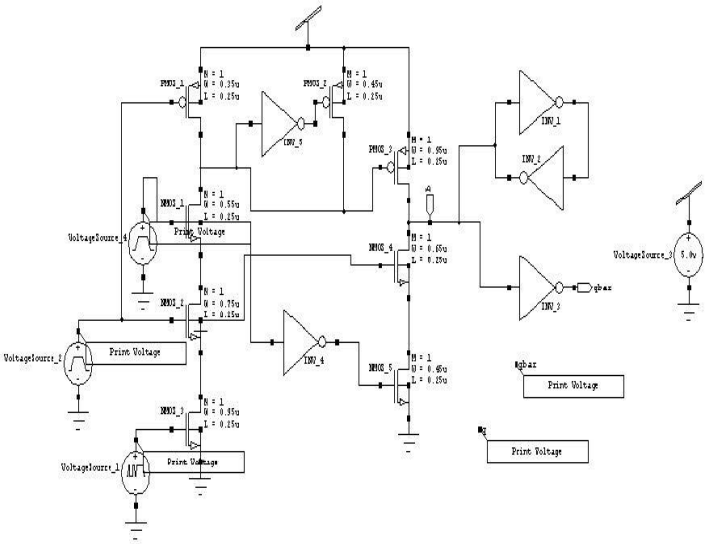

Fig. 2. The utilized CD-Flip-Flop architecture.

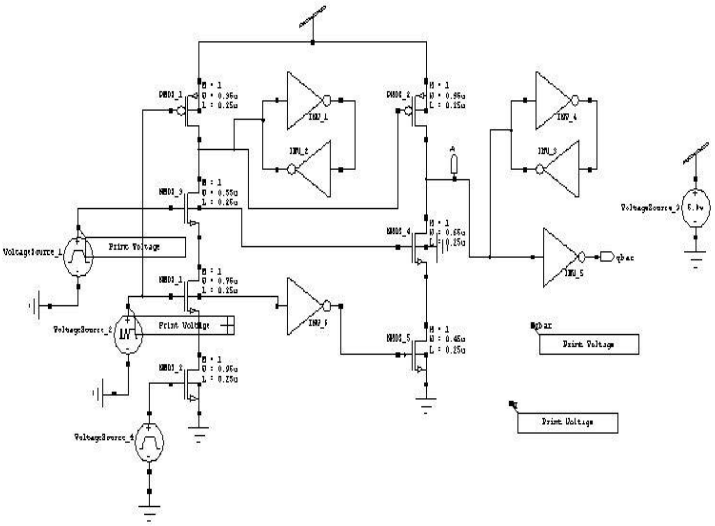

Fig. 3. The utilized SCD-Flip-Flop architecture.

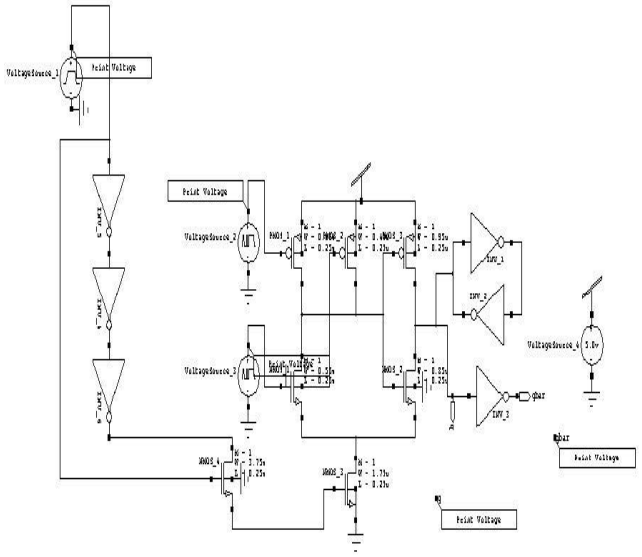

Fig. 4. The utilized MHL-Flip-Flop architecture.

III. SIMULATION RESULTS AND IMPLEMENTATION

This simulation is based on conditions and implemented in 250nm CMOS technology. A 20fF capacitor is placed in the output of the Flip-Flop, a 3fF capacitor is placed at the output of the clock buffer, the 500 MHz clock frequency and 5.0 V power supply is used as operating condition, which makes the proposed architecture suitable for low power applications.

The outputs waveforms are different architectures are shown in below figures1-8.

The simulation results of different architectures are shown in Table 1.

From the below architectures of these flip-flops we are reducing the power and delay. Based on the proposed architecture utilizes the lowest number of transistors and based on its architecture, the layout area required for this design is reduced. It should be noted that since this architecture requires a direct participation of input the drawn power from the input is also calculated.

The timing parameters of the proposed Flip-Flop are the real measurement of the performance of Flip-Flops based on power dissipation. The most important parameters are Setup time and Hold time. The power delay performances of these two parameters and C-to-Q delay an on power dissipation.

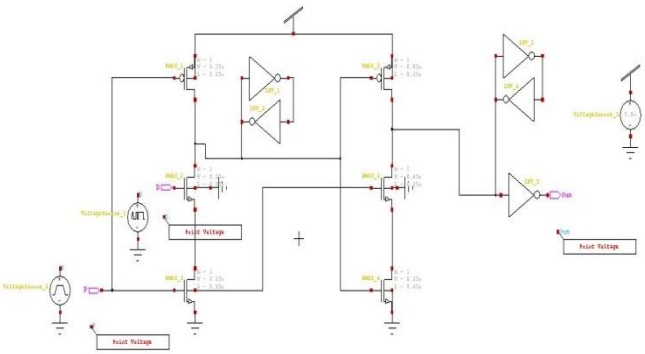

Fig. 1. Schematic diagram of DCO-FF architecture

Fig. 2. Waveform for DCO-FF architecture.

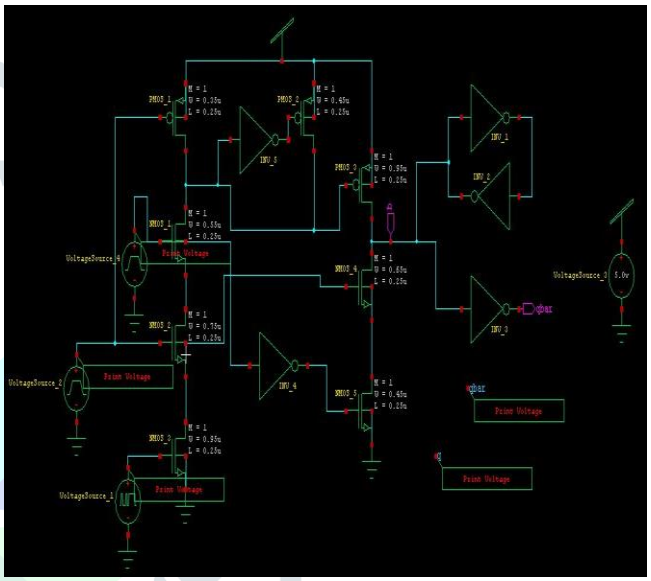

Fig. 3. Schematic diagram of CD-FF architecture.

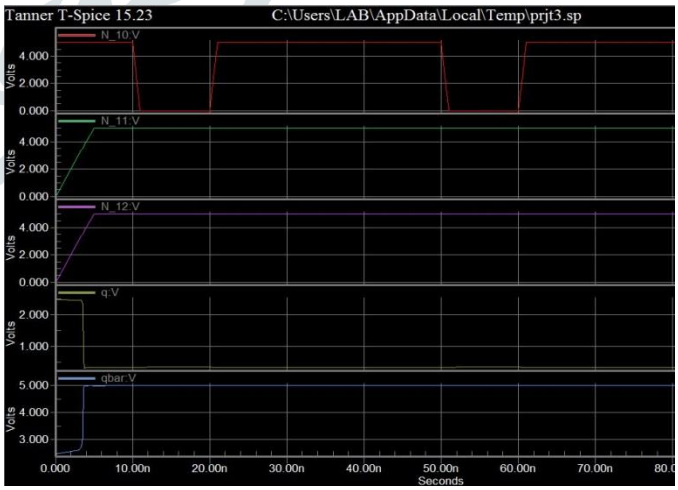

Fig. 4. Waveform for CD-FF architecture.

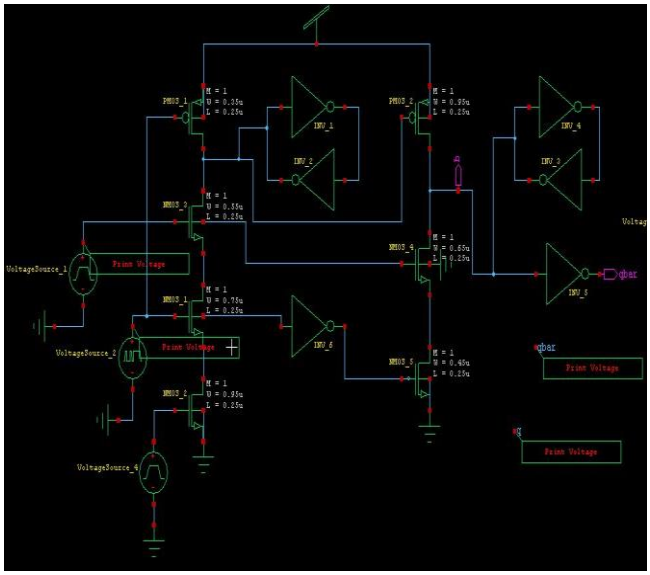

Fig. 5. Schematic diagram of SCD-FF architecture.

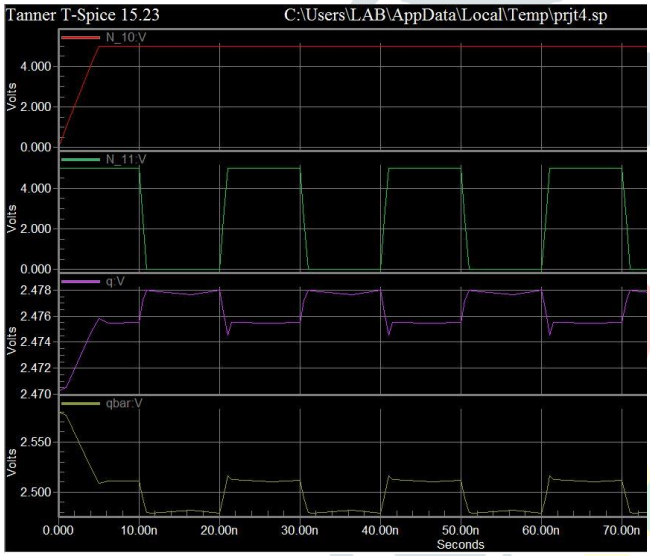

Fig. 6. Waveform for SCD-FF architecture.

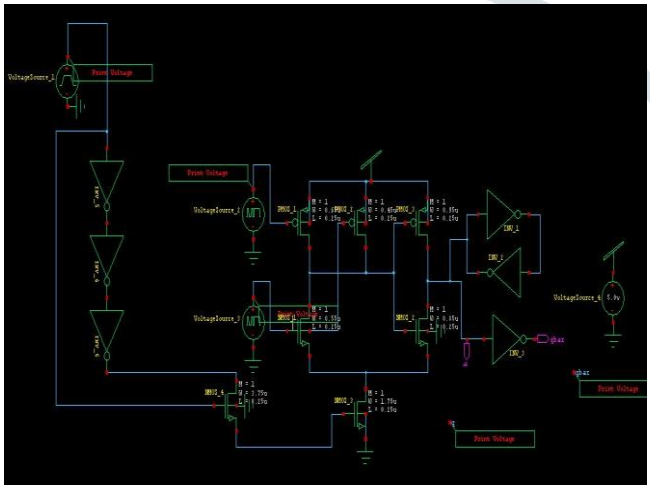

Fig. 7. Schematic diagram of MHL-FF architecture.

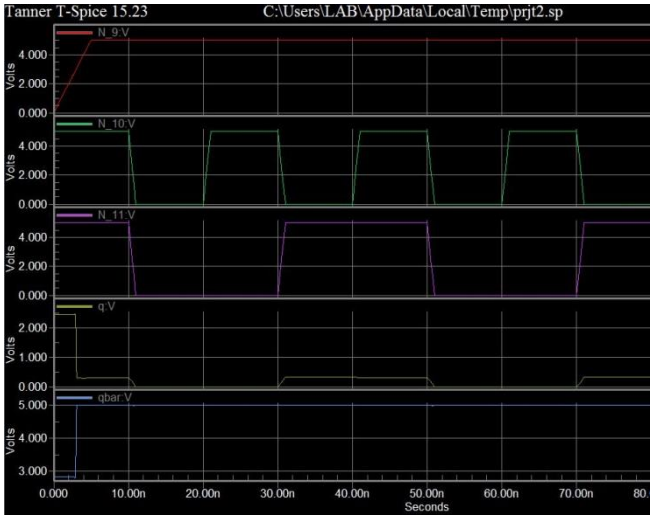

Fig. 8. Waveform for MHL-FF architecture.

The minimum amount of time a synchronous before the clock event data input should be held steady is known as Setup Time. It is done so that the data input is reliably sampled by the clock event.

Hold Time is the minimum amount of time after the clock event a synchronous data input should be held steady, so that the data input is reliably sampled by the clock event.

It should be noted that the optimal timing of this device rather than just D-to-Q, it is based on the optimization of PDP_{DQ} shows this device simulation results for PDP vs setup time curve. To measure hold time, a sufficient setup time should be applied. It should be noted that, the hold time is computed when the slop of clock–to-Q delay vs Hold time curve is equal to −1. All designs are further optimized subject to the tradeoff between power and delay i.e., minimizing the product of the two terms (Data to output delay and power).

Architectures	**DCO-FF**	**CD-FF**	**SCD-FF**	**MHL-FF**
Technology	250nm	250nm	250nm	250nm
Simulation	H-spice	H-spice	H-spice	H-spice
Supply voltage	5.0v	5.0v	5.0v	5.0v
No. of transistors	28	30	31	19
power	33.38 µW	34.82 µW	35.52 µW	31.72 µW

Table. 1. Comparison table of different architectures.

IV. CONCLUSION

Nowadays the power consumption reduction in different electronic devices is a rising concern. In this paper, a novel has been proposed to improve the performance of Flip-Flop, which can develop the memory cell and also the microprocessors performance. To reduce the power consumption and leakage power, a transmission gate was used to control the input data. Moreover, the P- MOS transistor creates a secondary discharging path for the node Q, and reduces the delay time required for "1" to "0" transition in transmission gate. This architecture is simulated using H-spice in 250 nm CMOS technology.

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