SYSTEM VERILOG MODEL DEVELOPMENT & VERIFICATION OF POR(POWER ON RESET) IN SENSOR CHIP

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Abstract : Simulation time, cost and test approaches are the major problems in the mixed-signal verification of a complex System-on-Chip (SoC). In this paper, an equivalent Power On Reset (POR) model has been created using the System Verilog language placed into a mixed-signal Sensor chip. Such a model can be simulate on a digital simulator, which is considerably faster as well as economical than the traditional method using an analog solver. Some verification approaches based on digital methods (Universal verification methodology) are also presented.

IndexTerms **– POR, Mixed-Signal Verification, System Verilog, UVM**

I. INTRODUCTION

Nowadays, with the increasing functionality at system level, the complexity as well as the number of Intellectual Properties (IPs) involved in a SoC is increasing. This leads to unavoidable interaction between Analog and digital IPs, creating an Analog and Mixed Signal (AMS) environment.

In addition, when AMS simulation to be part of SoC verification, it is eminent that speed of the simulation would be standing as a monster in between the strategical planning and the assurance for the first silicon pass.

Verification of such AMS environment involves a lot of simulations. Simulation for digital parts takes less time since they do not require high efficiency thus a large number of test patterns can be tested on it. While simulating analog part is time consuming process since it involves solving very complex differential equations for convergence[1][2]. This simulation time adds up to total verification time at the SoC level making verification a hindrance. Hence, we need some methodology where we can maintain accuracy of analog simulation while achieve speed of digital one.

It is possible to replace analog portions of SoC with their functionally equivalent digital models so that we do not require time taking analog engines for simulation. This indeed is achieved through modelling of analog blocks involved in AMS flow. The purpose of modelling is to provide simulation speedup where accuracy and speed trade-off must be taken into account. The classical approach to meet verification requirements was to use Verilog-AMS or have spice mixed simulation. Real value modelling is an add-on to these approaches. Real value modelling uses floating point numbers to represent data, like analog simulators while time is discrete like digital simulators[3].

In this paper, we demonstrate a mixed signal Sensor chip involving both digital and analog components which are to be verified. Key contributions to the implementation includes:

- Comparison between different modeling languages.
- Model-based design of analog signal of POR block by using System Verilog verification language.
- Completing the multi-level verification structure with reference of UVM verification methodology.

The remainder of this paper is organized as follows. Section 2 shows comparison between different modeling languages. Section 3 is an overview of mixed-signal Sensor chip. The software programming is described in section 4. Section 5 proposes the verification approaches. Section 6 covers experiment results and simulation waveforms and the conclusion in Section 7.

II. COMPARISION OF DIFFERENT MODELING LANGUAGES

One solution to model the POR block is Spice Modeling for Analog designs which helps create equivalent of Analog Circuit Design using simple passive elements resistor, capacitor, Dependent & Independent Sources along with Behavioral Modeling can limit the speed of Simulation giving the required accuracy.

Another solution is Verilog-AMS. With the advent of Verilog-AMS novel idea is used to merge existing digital and analog designs such that we do not require to rewrite individual designs.Without Verilog-AMS only single design domain can be developed that is either analog or digital designs.

However, to verify at SoC level both the mixed signal languages (Verilog-A and Verilog-AMS) have lots of limitation that reduces the simulation speed. With System Verilog only limitation is accuracy and that can also be evitable.

Table 1: comparison of simulation languages

Simulation Language	***Benefits***	***Limitation***
[1]SPICE	• Very Accurate • Able to Solve circuit equations • Use for Nonlinear DC Analysis	• Does not include effect of noise and interface • *Greater simulation time* • *Cross-talk is not taken into account*
[2]Verilog-AMS	• Faster than SPICE • Electrical signals are supported • Provide good platform for mixed signal design	• Required Analog solver • Convergence error are always present
[3]Verilog	• Faster than other languages • Digital solver only	• Real port are not available • Accuracy is poor
[4]System-Verilog	• Faster than SPICE and Verilog-AMS • Digital solver only • SV construct are useful in verification	• Accuracy is average

III. SYSTEM ARCHITECTURE

This research is based on a sensor chip including both digital and analog blocks. Figure 1 shows the overall structure of this circuit. External Vdd generator, which is external pad, is used to generate Vdd signal externally. Digital Vdd regulator, which converts Vdd into **dvdd**, is used by digital block. Master oscillator provides clock to digital block and also to POR block. It will provide clock to POR only when it is necessary. External reset provides **reset_bar** signal to POR externally.

A Sensor chip is generally divided into two parts. The first part contains Digital block e.g power management unit, sensor registers etc which are digital modules using Verilog HDL design. The second one is analog models which contain POR, Bias Regulator, and Master Oscillator in SPICE designs. The **reset_bar** (negative logic) and **clock_valid** of POR are generated whenever, the **Vdd** signal from External VDD generator and clock signal from Master Oscillator will be as per requirement. When **reset_bar** signal gets de-asserted, digital block can start its working. In our research paper, Digital Vdd regulator, Digital block and External reset are considered to be golden models or black boxes.

Some of the topics covered in the paper include, but are not limited to, the following:

- Check the function of POR block, that senses the analog **Vdd** signal, Digital Voltage regulator and Clock from Master Oscillator used for proper functioning.
- Verify mixed-signal sensor chip by digital verification techniques.

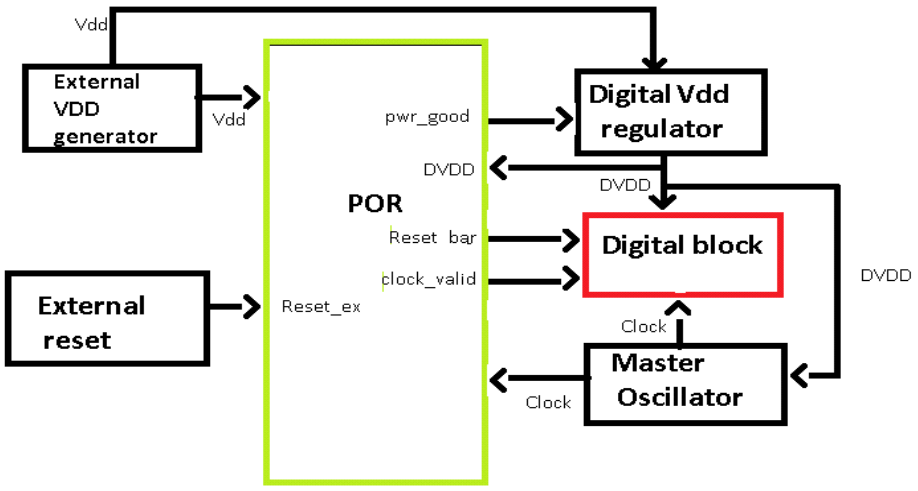

Figure 1: POR connection in sensor chip

IV. SOFTWARE PROGRAMMING

The **Vdd** generation process is a continuous function. It looks like ramp signal. External VDD generator generates it gradually. It will apply to POR, and checks whether **Vdd** signal value is beyond the threshold value. Threshold value is decided by the designer and that values will vary for different sensor chips. Here, it is 4.5V, where External VDD generator try to keep voltage to 5V. Figure 2 represents conversion of ramp signal into floating points.

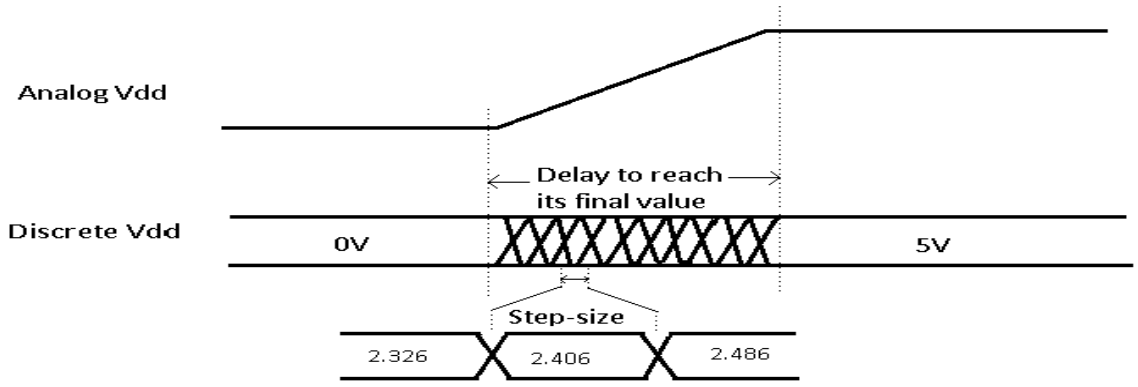

Figure 2 : analog data conversion into real data

V. SYSTEM LEVEL VERIFICATION

Leveraging pre-existing digital verification techniques and verification environment on mixed-signal sensor chip is the motivation in this research work. It will effectively mitigate the cost of mixed-signal sensor chip verification procedure.

A. Verification environment

We set up the verification environment with the object oriented programming (OOP) concept and multi-level hierarchical scheduling by System Verilog language, with reference to the universal verification methodology(UVM). The test bench structure is shown in Figure 3.

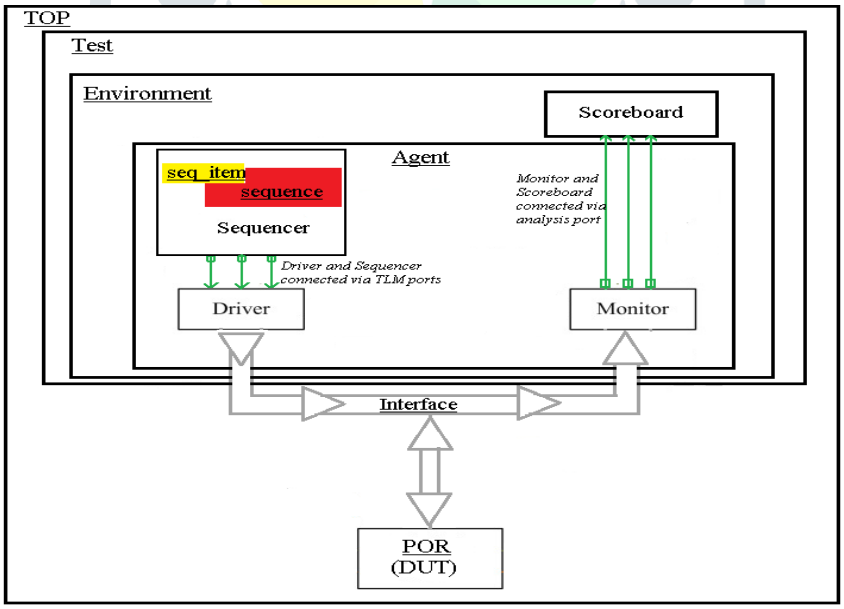

Figure 3: Test-bench architecture

We have developed the behavioral model of POR block using System Verilog language and this model is used as DUT in the SV-UVM test bench. POR model is dynamically controlled from UVM test bench, and it uses digital kernel in digital simulation environment. The stimulus generated by **sequence_item** and sequences shown in figure 3 interacts with the POR model by manipulating signals with logic and real data type.

Driver and Monitor connect the transaction data objects and activities, on interface of the POR module. Driver communicates with the sequences using sequencer. It gets input transactions as well as various sequences from input channels, manipulates those transactions in a user-defined manner according to function of different digital blocks and delivers one or more streams of transactions to interface. Test generates a stream of constrained random transactions and delivers them to a sequencer. TOP contains POR block (DUT) and test-bench components. The information e.g step size of Vdd ramp, which POR block and test-bench gets outside of interface is provided in TOP. As shown in Figure 2, delay and step-size values are inserted and applied it to test-bench to generate **Vdd** signal as per desired values. Values can be given at runtime with $value$plusargs switch that change the value of variable in TOP. We will discuss it more in section VI.

B. Constraint random value generation

Constrained random testing is more effective than directed testing approach. Using this approach, the ramp type behavior can be easily achieved. This UVM test bench uses constraint-driven test on top of an object-oriented data abstraction that models the data both on integral and real types to be randomized as objects that contain random variables and user-defined constraints. It's also an easier approach to find hard-to-reach corner cases in analog modules because in randomization seed is used to generate random numbers and by changing it, will have different sequence of random numbers. Figure 4 illustrates the constrained random analog data input process.

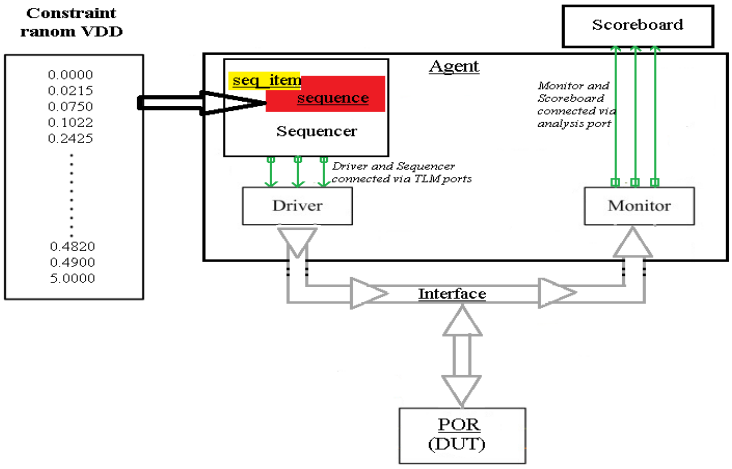

Figure 4: Vdd generation using constraint

VI. EXPERIMENTAL RESULTS

Using the test bench of Figure 3, this research covers conversion of analog nature signal into real type variable for POR block. A data sequence processed by POR block, is send to Driver by means of the Interface and Driver will drive the stimulus sequentially as per behavior of different blocks. The whole process is described by Figure 5:

1. Initially **Vdd** is zero. It is generated in steps by Driver. Once it reaches to its threshold value then POR block will assert **pwr_good** signal. In response to that, Driver makes **dvdd** signal low to high.

2. This **dvdd** indicates, that, now POR can go for verifying the clock. Based on clock's duty cycle of specific pules, **clock_valid** will either assert or remain low as a pulse.

3. **Reset_bar** signal gets de-asserted after clock has been asserted.

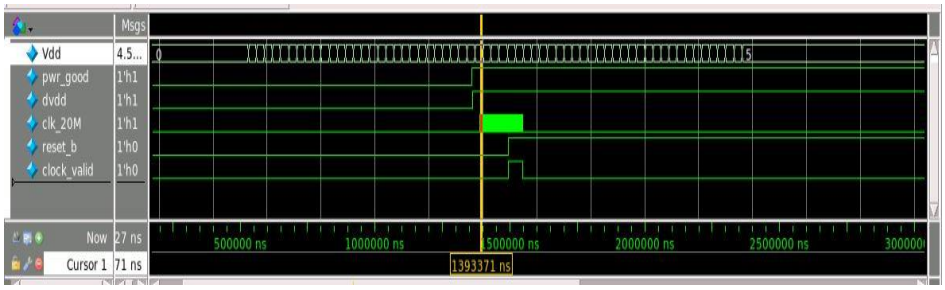

Figure 5 : simulation waveform of POR

In actuality, POR block is an analog block intended to provide timing reset to the digital block which is outside of POR block. It also provides **pwr_good** signal to the bias regulator. This can be seen in wave form (Figure 5).

Figure 5 illustrates the Vdd signal with its real data. As discussed above, it mainly depends on two factors step-size and delay to reach its final value. Figure 6 and 7 shows the waveforms, which are adjusted with step-size as well as delay set externally, thus the trade-off between speed and accuracy can be selected as per user requirement.

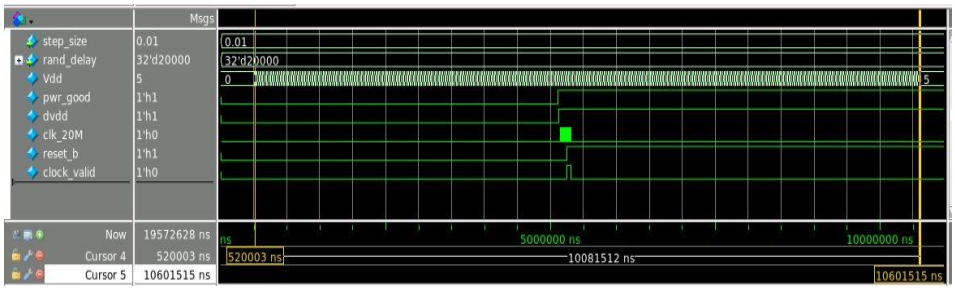

Figure 6: More accurate(step-size is less) and low speed speed compare to figure 7

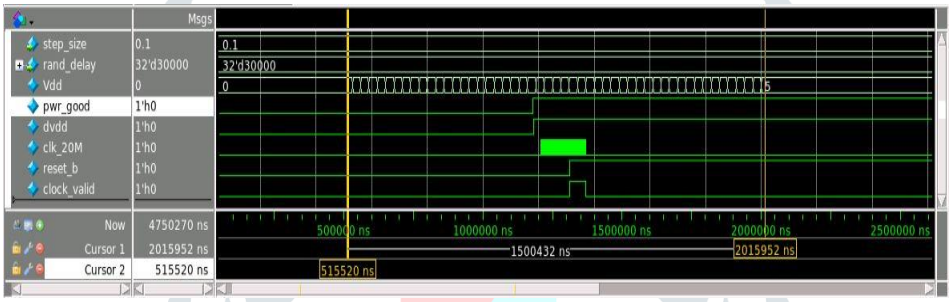

Figure 7: Less accurate(step-size is more) and high speed speed compare to figure 7

VII. CONCLUSION

This paper describes a verification process of a POR block in the mixed-signal Sensor-chip. Much has been done in the development of model, use of digital simulator e.g. Questasim and UVM methodology to address this verification complexity and minimize time consumption during simulation. Key advantages for this implementation include (i) real data in a digital-metric simulation tool and test bench, (ii) verification methodologies applicable to mixed-signal Sensor chip, (iii) a faster approach that can speed up the regression testing period,(iv) Constrained random input data verification. The results show that it is one of the best choices for mixed-signal Sensor chip level verification, because it does not only have faster simulation speed but also it is easier to migrate to the advanced digital verification techniques.

The drawbacks of such models tend to be less accurate and it is very difficult to write equivalent models for many classes of circuits. Applications of this type of modeling are better used for functional simulation. In brief, this paper links analog and digital circuits in a common verification environment to help the verification engineer to apply more verification methods than in traditional approaches. The future research will focus on improving the accuracy of analog models, thereby increasing the flexibility and reusability of the verification.

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