Analysis of Low Cost Scan Architectures

[1]Jinal Pathak,[2]HareshSuthar,[3]Yogesh Parmar, [4]Nirav Nanavati
[1]Student,[2]Head of Department,[3]Assistant Professor, [4]Delivery Manager
[1]Electronics and Communication,
[1]Parul University, Vadodara, India

Abstract: The current trends necessitate high performance DFT techniques to ensure testability of the manufactured SOC. Along with the benefits; the high performance DFT techniques are also accompanied by some costs. DFT Scan Architectures toll with power, pin, area and timing requirements, just to name a few. This paper aims at analyzing various existing Low cost DFT architectures. In addition, described are the various merits and demerits of the proposed methods. Finally the various performance parameters are compared for each of the architectures in tabular format.

IndexTerms **- Scan architecture, compressed scan, test wrapper, scan chain**

I. INTRODUCTION

With growing specialization, customization of scan architecture to the consumer needs has increased phenomenally. Specific chip designs die sizes and package requirements demand specific scan architecture modelling and reorganization. In general, scan architectures have the following pin requirements:

1. Scan Input
2. Scan Output
3. Scan Enable
4. Scan Clock
5. Scan Reset

Sharing of these inputs with functional inputs enables ease of stringent pin requirements, which test to be particularly of concern for small chips. In addition in cases like microphone and sensor chips, the pins available for scan may be as small as three to two top level pins. This calls for efficient and less expensive scan architectures.

The tradeoffs with reduction of pin count majorly include, increased area requirement for scan components and increased complexity.

The study aims at analyzing three existing low pin count scan control architectures. It provides a brief outline and gist of the scan control methods, the target application size and flop count.Later in the studya comparison of the merits and de merits of enlisted architectures is made. This comparison will be generalized and coarse as the target application of the architectures may vary. Based on the application requirement, a more detailed comparison based on implementation on a specific design (of specific flop count and area) can be made.

II. A THREE PIN ARCHITECTURE BASED ON FSM AND OMSR

Since the requirement of low pin DFT design is growing over the period of time, many designers have proposed various architectures. One such 3 pin architecture includes incorporating FSM and an OMSR (Operation mode shift register) . This architecture requires the use of TDI, TCK and TDO pins to control test procedures. Based on the sequence applied on the TDI various the state of the OMSR is initialized and triggered. This is followed by shifting of n bits into the OMSR, thus the configuration of testmode is accomplished. Also a multiplexer based technology is used to select between test data and functional data, selection of which is controlled by various controlled signals produce by the test control unit. This architecture involves use of a control bit to indicate the end of shift out operation and requires non overlapping scan operation.

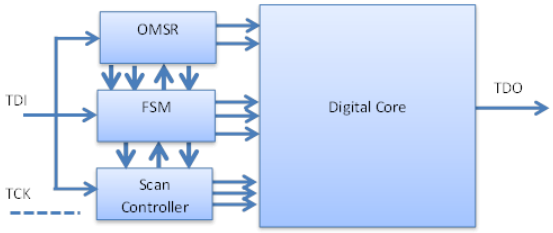

Figure 1 Three pin scan block diagram

FSM operation:

The state machine is first initialized to scan state, followed by a sequence of scan load, capture and scan unload. These loading and unloading procedures must be non- overlapping. Completion of loading is indicated by detection of bit 1, thus the FSM moves to the next state. The various states of the FSM are as follows:

- Scan-Out:In this state the scan chain must contain all zeros. When 1 is encountered the FSM moves to test init state.
- Test Init:Scan operation actually begins here. The value present at TDI defines the next state.
- Load SCR: It is a two bit register with three valid values, capture clock pulse, capture reset pulse, no capture pulse. The SCR is loaded through TDI during this state. After the number of cycles needed for SCR loading, the FSM moves back to Test Init state.
- Scan-In: This states allows shifting in data through TDI into the scan chains. When 1 is encountered at scan out, shift operation is completed.
- Capture Pulse: This state is one cycle long. The scan enable is kept low during this state.

Although this design proves to save the architectural requirements, this would result in increased area and complexity. Also compatibility to available vender ATPG tools is also a challenge, although some tools may be able to provide test support for this approach. Also one of the major drawbacks is the requirement of non overlapping scan operation which results in doubling of the test time. Also, since a single scan chain is supported, hence the power dissipation due to long chain lengths for designs having larger flop count may prove to be a major drawback of the design.

III. AN FSM AND LOW PIN COUNT CONTROLLER ARCHITECTURE

EDT (Embedded Deterministic Test) compression technique is used. Generally this requires eight signals, but a Test Controller Wrapper is used to allow DFT with three pins.This architecture basically consists of the following units:

Interface: Allows controller to interface with top level pins

FSM state machine block: determines and tracts between various scan states such as load, unload, shift and capture. It produces all the required scan control signals.

The counter block: It manages the number of shift
The EDT: It is a Mentor Graphics compression technique

Two possible configurations are:
1. Standard Scan Configuration which is the compressed scan mode.
2. Bypass mode. In this mode the compression is bypassed and all chains are configured to a single chain.

One main limitation is that the flow is not fully automated. Also the enabling of test configuration and EDT configuration tends to require complex circuitry. Around 1K gates are added with EDT.

IV. A SINGLE PIN DFT ARCHITECTURE

Another approach involves the use of OPMISR (On-Product Multiple Input Signature Register) based scan compression which use a MISR base comparator. The existing solutions for pin-count reduction include:

1. Scan compression with serializer and deserializer
2. LBIST based scan compression
3. OPMISR (On Product Multiple Inpt Shift Register).

Pattern Match Method: A pattern matching method is used to detect the beginning of the shift and capture procedures. This pattern matching is used to control the value of scan enable. In addition there are two sets of counters loaded to a predefined shift and capture cycle counts. This method reduces test application time by 10-15% in addition to reduction of pin requirement.

IEEE 1149.1 JTAG Based Architecture: For more complex scan compression, the number of control signals increases and hence the previously described architecture may be of little aide. A TAP controller is used to generated the control signals required for scan operations. A combination of specific JTAG states is used to generate specific scan control signals. This is advantageous to the previous method in terms of savings in test time as well as elimination of need of counter, although the toll in this case is increase in area. The transition sequences must be provided as inputs to the ATPG tool.

Table 1 TAP Controller State Decoding for Internal Scan Control Signals

Scan Control Pin	**TAP controller state/s**
Scan Enable	Shift_DR state and TMS=0
Capture Mode	Run_Test_Idle state and TMS=0
CMLE	Pause_DR state and TMS=0
Scan Reset	Select_DR>Capture_DR> Exit1_DR>Update_DR

MRE	Shift_DR> Exit-1_DR after first scan load only or subsequently after every assertion and de-assertion of MISR_OBS signal
MISR_OBS	Select_DR>Captur_DR> Exit1_DR>Pause_DRand TMS=0

Increasing Scan Channel Bandwidth by sharing JTAG pins:

This one pin architecture is based on sharing of the pins for the IEEE 1149.1 JTAG interface. This is achieved by configuring the TAP into run test idle state and asserting the internal TMS and TRSTN when the scan enable goes high. An important advantage of this method is that it is independent of any tool specific scan compression method.

A combination of the above mentioned techniques are used to generated the single pin solution. The Test designer may choose amounts the various techniques as per his requirement. The architecture proposed in the concept referred is as follows.

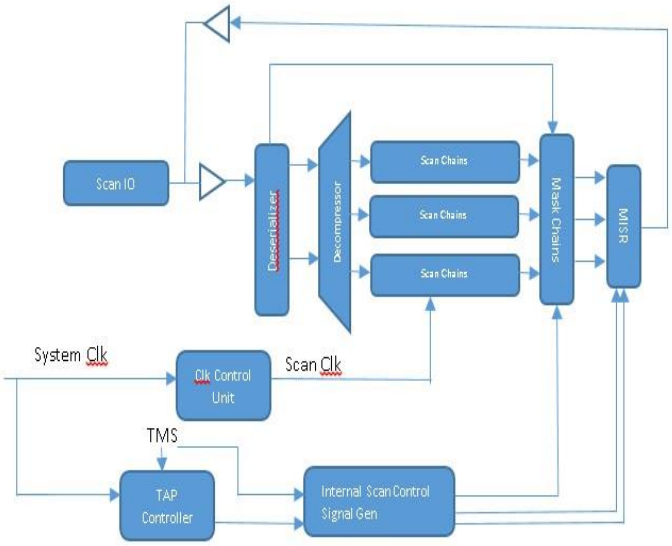

Figure 2 Single Pin Scan Architecture

This method is independent of any tool specific compression architecture. It proves to provide a single pin solution to scan. One significant demerit is the area and complexity increment introduced by TAP controller and internal scan control decoding.

V. A COMPARTIVE STUDY

Three low pin count scan architectures have been analysed in this study. Each method accomplishes scan test control generation and scan test executionby a range of techniques. To summaries the merits and demerits of the architecture discussed a coarse comparison of various parameters influenced is provide in the following table.

Table 2 Comparison of Cost Parameters

Architecture	**Pin Requirement**	**Area Increment**	**Complexity**	**Test Time**
A Three Pin Architecture based on FSM and OMSR	Three Pins (TDI,TDO,TCK)	High due to FSM and OMSR	High	Double due to requirement of non overlapping scan as compared to overlapping scan

A FSM and Low Pin Count Controller Architecture	Three Pins (Clock, Scan_in, Scan_out)	Not too high (as around 1K gates added due to scan logic)	Not too complex, but all logic is IP of Mentor Graphics	Low due to compression
A Single Pin DFT Architecture	Single Pin (TMS pin)	High Due to TAP and decoding logic	High	Comparatively less due to time saving schemes

VI. CONCLUSION

This study analyzed three methods of low pin scan architecture implementation. The basic operation of each architecture is described with illustration. Also, it enumerated the merits and demerits of each architecture. A comparative study is made for these three methods on the basis of pin requirement, area, complexity and test time.

VII. FUTURE WORK

As an enhancement to the existing schemes, we shall attempt to develop a low pin count scan architecture which aims at reduction of complexity and area increment due to scan insertion. Also, the coverage parameter will be measured in order to ensure no compromise in terms of testability.

VIII. ACKNOWLEDGMENT

The author would like to thank the reviewers for providing constructive feedback and comments.

REFERENCES

[1] Zhigang Jiang and Sandeep K.” A Test Generation Approach for Systems-on-Chip that use Intellectual Property Cores”, 12th Asian Test Symposium, 2003.

[2] Marcelo de Souza Moraes, Marcos BarcellosHerve, Marcelo SoaresLubaszewski; ” Zhigang Jiang and Sandeep K.”, IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems(DFT), 2012.

[3] Jocelyn Moreau, Thomas Droniou, Philippe Lebourg, Paul Armagnat; “Running scan test on three pins: yes we can!”, International Test Conference, 2009.

[4] Mudasir S. Kawoosa, Rajesh K. Mittal, MaheedharJalasuthram and Rubin A. Parekhji; Towards Single Pin Scan for Extremely Low Pin Count Test”, 31st International Conference on VLSI Design and 17th International Conference on Embedded Systems, 2018

[5] ZhikuangCai, Kai Huang, Jun Yang; “Low Cost Design-for-Testability Features for System-on-Chip: Case Study” 2nd International Conference on Computer Engineering and Technology, 2010

[6] Ms.Janki Chauhan, Mr.ChintanPanchal, Prof. HareshSuthar; “Scan Methodology and ATPG DFT Techniques at Lower Technology Node ”, International Conference on Computing Methodologies and Communication, 2017