Design and Simulation of 8-Bit ALU Integrated With 8x8 SRAM Memory Using Hybrid of GDI and SB Technique

Asif Iqbal Mulla[1], Nithin[2], and Abubakar Shameez[3]

Assistant Professors, Electronics and Communication Engineering Department, BIT, Mangalore, Karnataka, India.

Abstract— An 8-bit Arithmetic Logic Unit (ALU) and SRAM is designed by using the hybrid of two techniques i.e. gate diffusion input (GDI) technique and substrate biasing technique (SBT). In this work, ALU consists of multiplexer (4x1 and 2x1) and full adders used to perform logic operations such as OR, AND, XOR, XNOR and arithmetic operations such as Increment, Decrement, Addition and Subtraction. To design multiplexer GDI cells are used and substrate biasing technique is utilized. GDI is used to design full adder AND, OR, XOR, XNOR gates which are then associated to realize ALU. As compared to CMOS techniques this design consume less power, required less surface area, more efficient and faster. Cache memory of Microprocessor and ASICs used large SRAM array can occupy a large portion of the die area. The more than 90% area of SOC in next 10 years projected to occupy by the high density circuits such as SRAM. The large array of fast SRAM helps to raise the performance to optimize the performance of such chips. However, the cost of the chip becomes higher due to the area impact of incorporating SRAM arrays into a chip directly. Hence it is require to minimizing the footprints of SRAM cells. As an outcome, millions of minimum-size SRAM cells are tightly packed, which causes SRAM arrays are densest circuitry on a chip. This project aims to design an 8 bit ALU which is interfaced with the 64 bit SRAM where the inputs and results of ALU operations can be stored. The simulation is carried out using CADENCE VIRTUOSO with gpdk 180nm technology.

Keywords—**GDI Technique, ALU, Substrate biasing, cadence VIRTUOSO gpdk 180,6T cell, SRAM, Sense Amplifier, VLSI.**

I. Introduction

The ALU is core block of CPU. It performs several arithmetic and logical operations, where these arithmetic and logical operations are the key and basic functions in CPU. The three major constraints in VLSI Design are area, power, and time (delay). Here the ALU is designed with less complexity, low power and less delay using the idea of gate diffusion input and substrate biasing technique [1]. To design ALU the multiplexers and full adders are used.

With the advancing technology, there is always an increase in demand for large data storage capacity. This has driven towards higher data storage densities and towards more compact design in the process of memory development and fabrication technology. A variety of memories are available to store and access the information. According to the requirement one may design the memory to store the temporary data. The SRAM is very useful building block in many applications such as CPU cache memories, on-chip memories, buffers etc. SRAM is easily fabricated and is much faster than DRAM but require more space. Dynamic RAM unlike the Static RAM needs to be refreshed after equal intervals of time. SRAM's the standby power requirement is very low even though it has high density of transistors. Due to larger noise margins SRAM cells have noise immunity, and have ability to operate at low power supplies. In this work, we design an 8x8 SRAM and it consists of 6 transistors per cell[2,3].

The organization of the paper is as follows: Section II describes overview of literature survey. Section III given the information about Proposed Design. Design of Arithmatic and logical unit discussed in section IV. Design of SRAM is discussed in section V. Finally the Experimental results and conclusion of paper are given in section VI and VII.

II. Literature Survey

The author of paper [1] explained how the number of transistors can be reduced in the design of ALU by using hybrid of two techniques i.e. GDI and SBT techniques. The author of paper [2] explained about how to improving the efficiency of an 8x8 SRAM memory array by reducing the area and observing the variations in delay for variations in process parameters. The author of paper [3] explained about the design of 16x16 SRAM using GDI and SBT techniques. The author of book [4] explained the design of the single 6T SRAM such that during read operation it should not allow modification for the stored data and during write operation it should allow modification of the stored data. The author of paper [5] implemented 4-bit ALU using the concept of GDI and simulation is carried using mentor graphics 45nm technology and compared with pass transistor logic and CMOS logic realization. Optimization of devices with respect to speed and power is a significant issues in low voltage low power applications this which can be overcome by GDI technique [6].

A. Gate Diffusion Input

The standard GDI cell as shown in Fig. 3. The GDI technique is implemented using transistors for the complex logic functions. It reduces power consumption, propagation

delay and area circuits[8]. The source of the NMOS in GDI cell is not connected to ground and the source of PMOS in GDI cell is not connected to supply voltage. It uses source of both NMOS and PMOS to connect two input pins, which makes the GDI design more flexible than CMOS logic. Therefore, three inputs in a GDI cell G (input to the common gate of PMOS and NMOS). P (source /drain input of PMOS) or N (source/drain input of NMOS). Substrate terminal of PMOS is connected to P and substrate terminal of NMOS is connected N as shown in Fig. 1 and corresponding logic is given in the Table I.

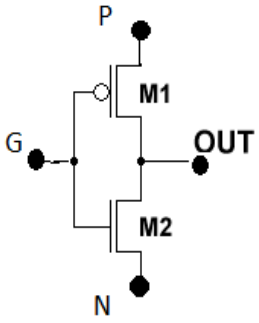

Fig. 1 Basic Gate Diffusion Input Cell

B. Substrate Biasing Technique

Substrate Biasing Technique (SBT): Substrate biasing in PMOS biases the body of the transistor to a voltage higher than applied V_{DD} and in NMOS, to a voltage lower than the applied Vss. Since leakage currents are the function of device substrate bias also known as back bias which can reduce leakage power and also raises the threshold voltage.

TABLE I
LOGIC FUNCTION FOR BASIC GDI CELL OPERATIONS OF ALU [1]

SN	Inputs			Output	Function
	N	P	G		
1	0	1	a	a’	Inverter
2	a	0	b	ab	AND
3	1	a	a	a+b	OR
4	a’	a	b	a’b+ab’	XOR
5	a	a’	b	ab+a’b’	XNOR
6	c	b	a	a’b+ac	MUX

IV. PROPOSED DESIGN

The proposed system aims at designing an 8 bit ALU using The design uses GDI technology and the substrate biasing. Where the PMOS substrate voltage is maintained greater than V_{dd} and NMOS substrate voltage is maintained less than Vss. This work also includes the design of 8x8 SRAM memory arrays, which is then integrated with the 8 bit ALU circuit and can be used to either read the data from memory to perform desired ALU operation or to store the outputs of the ALU operation that can be retrieved when required. The entire system is designed in CADENCE virtuoso gpdk180nm technology. The block diagram of proposed design shown in Fig. 2.

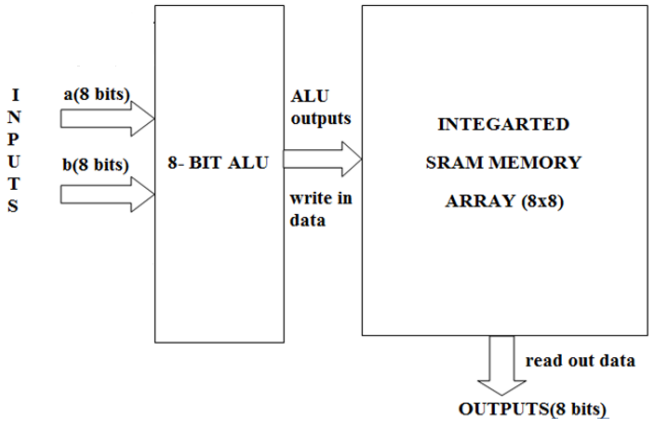

Fig. 2 Block diagram of ALU integrated with SRAM memory array

IV. ARITHMETIC AND LOGIC UNIT

Modern CPUs contain very powerful and complex ALUs and almost every microprocessors or microcontroller today contains at least one ALU. In our proposed design of ALU we used the idea of gate diffusion technique and substrate biasing. It contains 2x1,4x1 multiplexer and full adder as a sub blocks. Full adder is the main block in ALU, so both the techniques are utilized to implement full adder and multiplexer utilizes GDI technique. The 1-bit ALU is used as leaf cell for building 8 bit ALU. The schematic diagram for 1-bit and 8-bit ALU shown in Fig. 4 and Fig. 5 respectively.

The leaf cell of ALU consists of one full adders, two 4x1 multiplexers, one 2x1 multiplexer and a inverter as shown in Fig. 3. Increment operation performed by adding ‘1’ to the addend and decrement operation is performed by subtracting ‘1’ from the minuend. Subtraction operations is performed by using 2’s complement method. In 8-bit ALU the carries are interconnected between the leaf cells that is carry output of each full adder given as carry input to next bit full adder. The operations of ALU as shown Table II.

Where S0,S1 represents the select line for 4x1 multiplexer and S2 represents the select line for 2x1 multiplexer. The increment, decrement, addition and subtraction are the inputs to one of the 4x1 multiplexer and logical inputs are given to another 4x1 multiplexer. The 2x1 multiplexer is used to select either of the arithmetic or logical outputs.

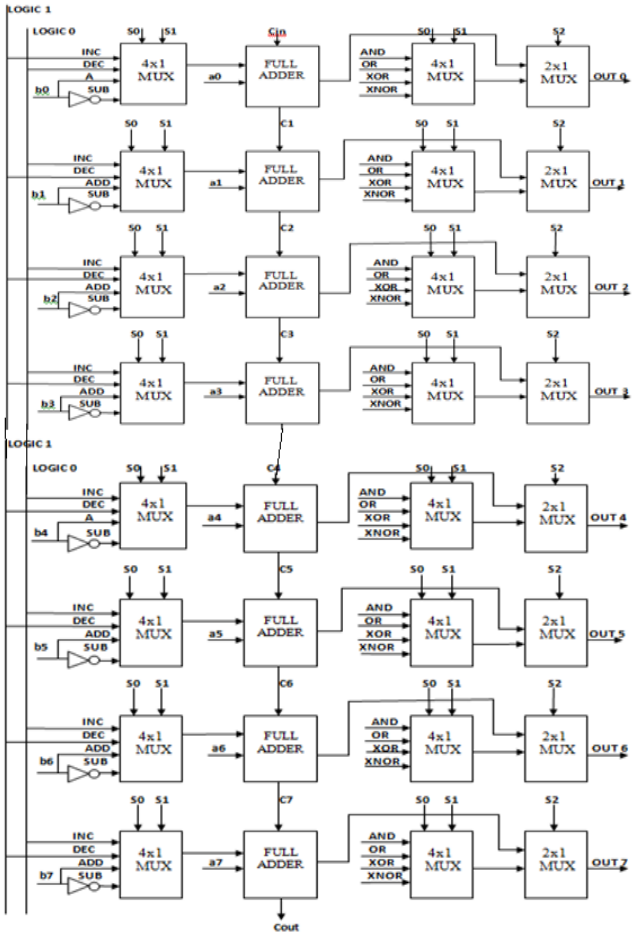

Fig. 3 Block Diagram of 8- bit ALU

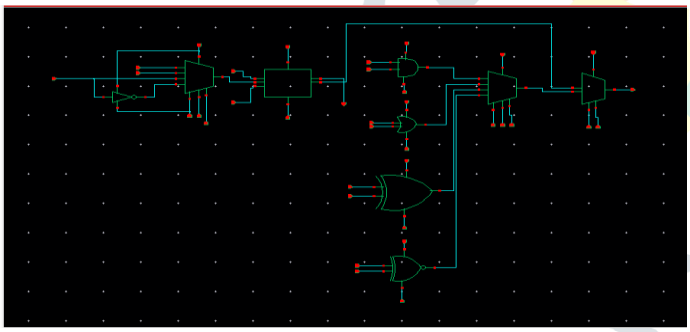

Fig. 4 Schematic Diagram of 1- bit ALU

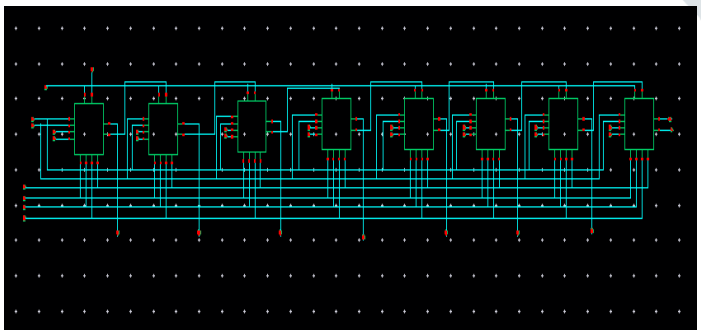

Fig. 5 Schematic Diagram of 8- bit ALU

V. Static Random Access Memory (SRAM)

SRAM is a type of semiconductor memory that uses bi stable latching circuitry (flip-flop) to store one bit. SRAM exhibits data reminiscence, in conventional sense SRAM is still volatile that eventually lost the data when the memory is not powered. An SRAM cell must be designed such that it provides a reliable write operation and a non-destructive read operation. The main building block of purposed SRAM blocks are as follows.

- SRAM cell
- Pre-Charge Circuit.
- Write Driver Circuit.
- Sense Amplifier
- Row decoder.

The Fig. 6, shows a typical SRAM block diagram. SRAMs can be organized as bit-oriented or word-oriented.. Bit-oriented SRAM every single bit in memory having separate address, whereas in a word-oriented SRAM each address accesses a word of n bits (where values of n include 8, 16, 32 or 64 etc). Memory Column decoders or column multiplexers addressed by Y address bits allow sharing of a single sense amplifier for each column.

TABLE II
Operations of ALU

Select lines			Operations
S2	**S1**	**S0**	
0	0	0	Increment
0	0	1	Decrement
0	1	0	Addition
0	1	1	Subtraction
1	0	0	AND
1	0	1	OR
1	1	0	XOR
1	1	1	XNOR

A. SRAM Operation

The operation of SRAM memory is classified into three modes i.e. standby mode, write mode and read mode. We use 6 transistors SRAM for the design as shown in the Fig. 7.

Standby mode: In this mode word line is deactivated, so both the bits access lines transistors M_1 and M_2 are disconnected from memory cell, hence in this mode memory cell retains its previous data as long as power supply is provided. The column capacitances are charges to supply voltage, through M_5 and M_6. In this mode memory cell consumes less power.

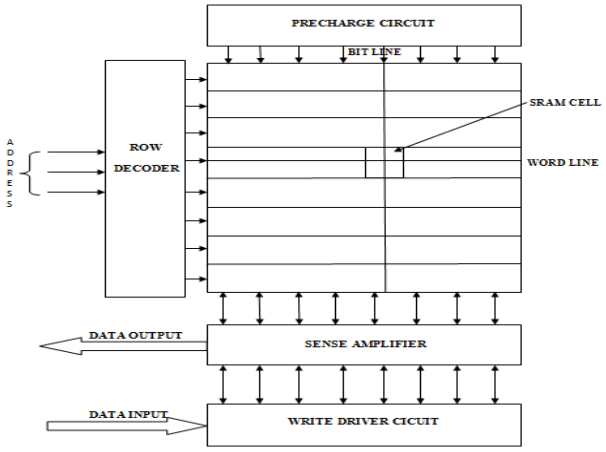

Fig. 6 SRAM Architecture

Write Mode: Suppose if we want to perform write zero operation by assuming initial stored data in memory cell as logic one, in the beginning of write operation the voltages present at two nodes A and B are V_{DD} and 0V respectively hence initially the two transistors M_3 and M_6 are operated in cut off mode whereas the transistors M_4 and M_5 are operated in linear region. Now by using write driver circuit the column voltage of bit line is forced to logic zero. Now the pass transistors M_1 and M_2 are activated by using word line whose address is given by row decoder.

Read Mode: Before the Read operation the two bit line voltages charge to supply voltage V_{DD}. During read mode, suppose if we want to perform read 0 operations, and then assume initial data stored in the memory cell is logic 0. and the initial voltages present at the storing nodes A and B is 0 and 1 respectively. Hence transistors M_4 and M_5 are operated in cut-off region whereas the transistors M_3 and M_6 are operated in linear region. The pass transistors M_1 and M_2 are activated by using word line which is controlled by row decoder circuit. Now there is no current flow through M_2 in transistor because the voltages at node B and bit line bar voltages are almost equal which is equal to V_{DD}. On the other hand, the transistors M1 and M_3 will exhibit a nonzero current and the bit line voltage is discharges to ground from V_{DD}. Now both the bit line voltages are given to the inputs of sense amplifier. The sense amplifier senses the input and it will produce logic 0 as output.

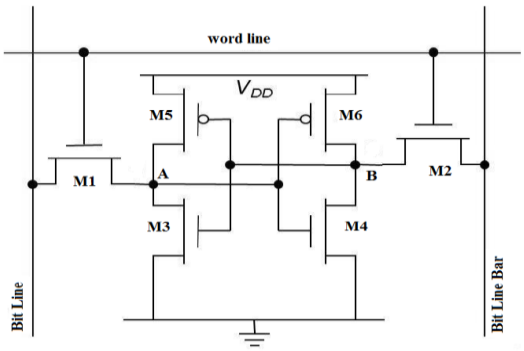

Fig. 7 Six transistors SRAM cell

The schematic diagram for Precharge circuit, write driver circuit, sense amplifier circuit, row decoder circuit and 8x8 SRAM memory are shown in Fig. 8, Fig. 9, Fig. 10, Fig. 11, Fig. 12 and Fig. 13 respectively.

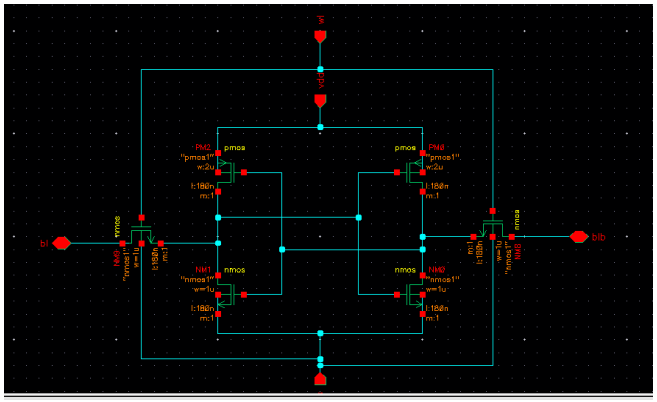

Fig 8. Schematic of SRAM Cell

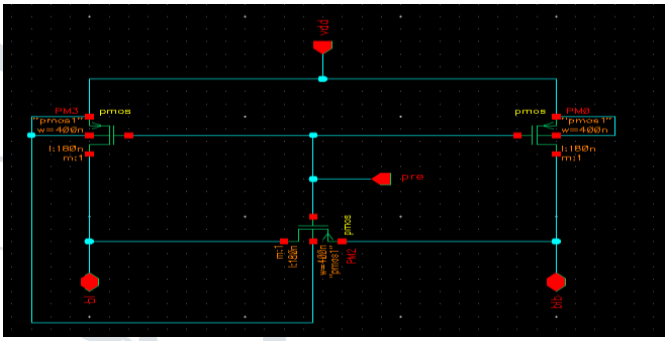

Fig. 9 Schematic of Precharge Circuit

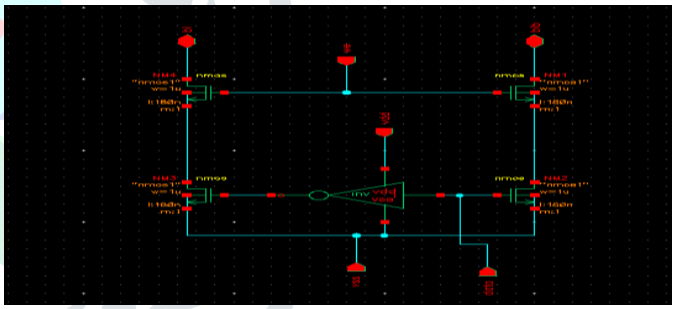

Fig. 10 Schematic of Write Driver Circuit

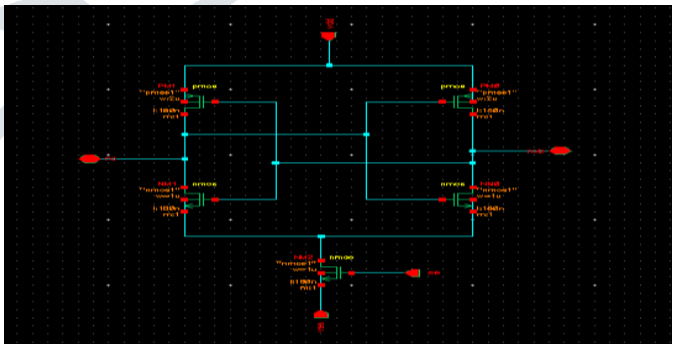

Fig. 11 Schematic of Sense Amplifier

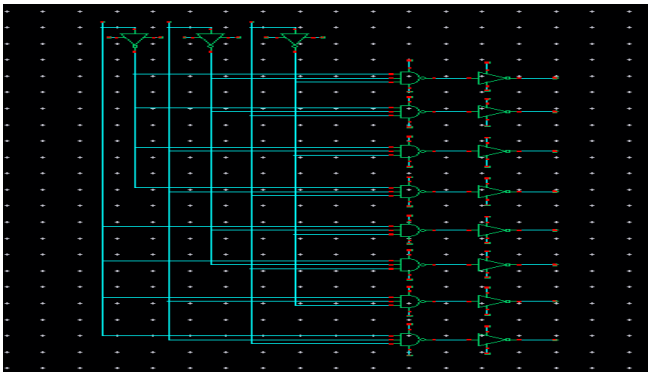

Fig. 12 Schematic of 3:8 Row Decoder

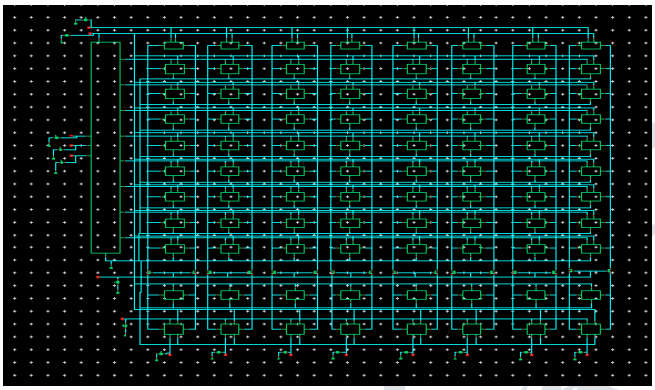

Fig. 13 Schematic of 8x8 SRAM Memory

VI. EXPERIMENTAL RESULTS

. The purposed design of 8 bit ALU integrated with 8x8 SRAM memory shown in Fig. 14. The complete SRAM array is designed, which include all peripherals components (Memory bit cell, Write driver circuit, Pre-charge circuit, Sense amplifier). The Design implemented using Cadence Virtuoso tool (gpdk180nm technology). The design is further verified using transient analysis. The transient response of 8 bit ALU, 8X8 SRAM and integrated design is shown in Fig. 15, Fig. 16 and Fig. 17 respectively.

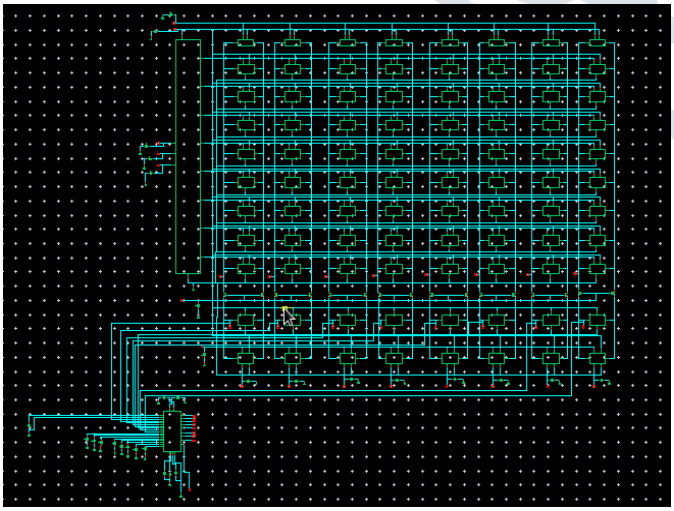

Fig.14 Schematic of ALU integrated with SRAM

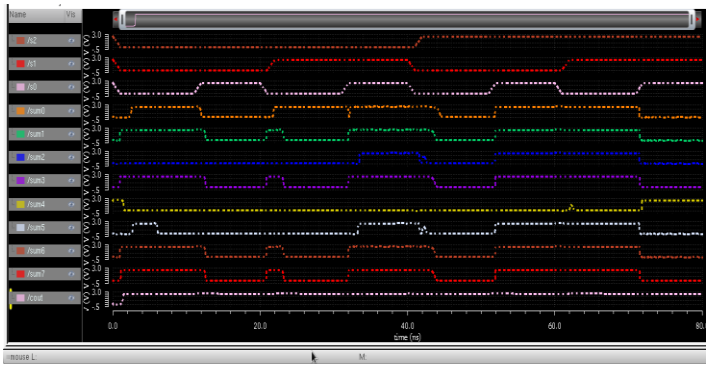

Fig. 15 Transient Response of 8 bit ALU

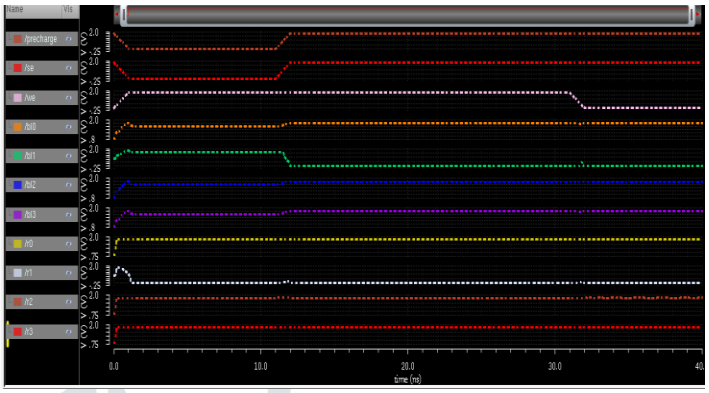

Fig. 16 Transient Response of 8x8 SRAM Memory Array

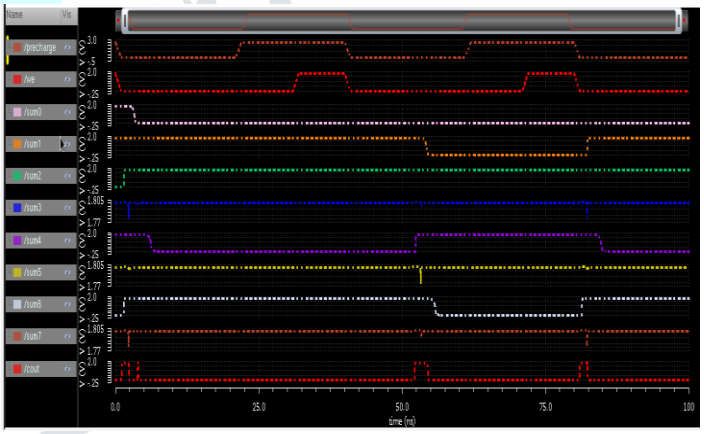

Fig 17 Transient response of integrated design

VII. CONCLUSION

The 8-bit ALU is successfully implemented using GDI cell and substrate biasing technique. Multiplexer designed using GDI cell and SB technique and other component in ALU used only GDI cell. The SRAM is designed for storage capacity of 64 bits i.e. 8x8 Memory array. Finally the 8 bit ALU and the SRAM memory array is integrated so as to store the output of the desired ALU operation. The complete integrated schematic is designed, implemented and verified using standard gpdk180nm technology using Cadence virtuoso tool for schematic.

REFERENCES

[1] Shreelakshmi, Sendamarai P "Enhancement of Design Quality for an 8-bit ALU" ABHIYANTRIKI an international journal of engineering and technology (AIJET) Vol. 3, No. 5 (May, 2016).

[2] Mansi S. Warde, V. Chandana S "Design and Analysis of 8x8 Static RAM", International Journal of Scientific & Engineering Research, Volume 6, Issue 7, July-2015.

[3] Preeti S Bellerimath and R. M Banakar, "Implementation of 16X16 SRAM Memory Array using 180nm Technology", International Journal of Current Engineering and Technology, a research article.

[4] Sung-Mo Kang and Yusuf Leblebici "CMOS Digital Integrated Circuits", TATA McGRAW-HILL EDITION 2003.

[5] M Kumar, MA Hussain, & LLK Singh. "Design of a low power high speed ALU in 45nm using GDI technique and its performance comparison". CNC 2011, CCIS 142, pp. 458–463.

[6] R Uma, & P Dhavachelvan. Modified Gate Diffusion Input Technique: a new technique for enhancing performance in full adder circuits. 2nd Inter. Conf. on Communication, Computing & Security, 2012.

[7] Anitesh Sharma, Ravi Tiwari, "Low power 8-bit ALU design using full adder and multiplexer" 2016 International Conference on Wireless Communications, Signal Processing and Networking, 23-25 March 2016.

.[8] Arkadiy Morgenshtein, Alexander Fish, Israel A Wagner," Gate-Diffusion Input (GDI) - A technique for low power design of digital circuits: Analysis and characterization" IEEE International Symposium on Circuits and Systems 1:I-477 - I-480 vol.1 · February 2002.

Asif Iqbal. M. Mulla: Born in 19th Feb 1979, Received his BE degree in Electronics and communication from Anjuman Institute of Technology Bhatkal, Karnataka, India and M.Tech Degree in Digital Electronics from B.V. Bhoomaraddi college of Engineering (BVBCET), Hubli, under VTU, India, in the 2007 and 2013, respectively. He has 9 years teaching and 3 Years Industrial experience. He published 2 conference and 6 journal papers. Presently he is working as Assistant Professor in the department of Electronics and Communication Engineering at Bearys Institute of Technology, Mangalore, India. His research areas include Embedded systems and VLSI design.

Nithin: Born in 19th July 1983, Received his BE degree in Electronics and communication from MVIT, Bangalore, Karnataka, India and M.Tech Degree in Digital Electronics and communication from MSRIT, Bangalore, Karnataka, India, under VTU, India, in the 2006 and 2010, respectively. He has 8 years teaching and 1 Years Industrial experience. He published 2 conference and 4 journal papers. Presently he is working as Assistant Professor in the department of Electronics and Communication Engineering at Bearys Institute of Technology, Mangalore, India. His research areas include Image Processing and VLSI design.

Abubakar Shameez: Born in 7th April 1988, Received his BE degree in Telecommunication Engineering from PACE, Mangalore, Karnataka, India and M.Tech Degree in VLSI & Embedded system from PACE, Mangalore, Karnataka, India, under VTU, India, in the 2010 and 2018, respectively. He has 7 years teaching experience. He published 2 journal papers. Presently he is working as Assistant Professor in the department of Electronics and Communication Engineering at Bearys Institute of Technology, Mangalore, India. His research areas include networking and VLSI design.