SAR ADC Using Low Power High Speed Comparator for Precise Applications

Neethu Prakash[1], Prof. Riyas K S[2]

[1]PG Scholar, [2]Associate Professor

Dept. of Electronics and communication Engg. Rajiv Gandhi Institute of Technology

Kottayam, India

Abstract—Now a days, low-power high-speed ADCs are integral parts of a variety of applications such as handheld devices. Comparators are the key building blocks of different types of ADCs. Several years ago, CMOS amplifiers were used as static comparators, although they suffer from very high power consumption (since they are always on) and inherent limited speed. In the proposed comparator, pMOS latch and pMOS preamplifier in addition to a small cross-coupled circuit are used with a special clocking pattern to adjust the preamplifier gain. The clocking pattern provides enough preamplifier gain; since pMOS transistors are used at the input of the latch, and the cross-coupled circuit is employed to keep the common mode voltage of the preamplifier outputs at a low level. It is shown that the proposed comparator reduces the power consumption by half while increasing the speed. Moreover, it operates at large input common-mode voltages close to VDD, although pMOS transistors are used at the input of the comparator. As another benefit, the preamplification delay can be set to its optimum value to have a better comparison speed and reduce excess power consumption. However, in the conventional and other comparators, this delay is fixed to a value which is far from its optimum point. As a result, the proposed comparator is a good candidate for precise low power high-speed applications. Deactivating the preamplifier after the optimum delay reduces the power consumption significantly. Therefore, it reduces the power consumption and improves the speed. The proposed structure can also be implemented using nMOS transistors, i.e., latch and preamplifier with input Nmos transistors. This will result in a higher speed because of the inherent superiority of nMOS transistors over pMOS ones. Using this comparator an SAR ADC is made. The tool used is Cadence.

Index Terms—Dynamic comparator, high speed, low power , two- stage comparator.

I. INTRODUCTION

Now a days, low-power high-speed ADCs are integral parts of a variety of applications such as handheld devices. Comparators are the key building blocks of different types of ADCs, such as SAR, pipeline, and flash ADCs. Comparators are the second most widely used device in electronic circuits after Opamp. Comparators are used in peak detectors, zero crossing detectors etc. Here a systematic methodology for designing a comparator is done. The circuits are optimized for power, speed and delay.

Using this comparator an energy efficient SAR ADC is made. The reason for using SAR ADC is that it implements a binary search algorithm, for an N bit SAR ADC it requires only N comparison periods, resolution ranges from 8 to 16 bits, low power consumption, physically small and has moderate circuit complexity. 2Associate Professor

The block diagram of SAR ADC is shown below. The successive approximation converter performs basically a binary search through all possible quantization levels before converging on the final digital answer. The timing of the conversion is controlled by an N-bit register, where N is the resolution of the ADC. Input V_{IN} is sampled and compared to the output of the DAC. The comparator output controls the direction of the binary search, and the output of the successive approximation register (SAR) is the actual digital conversion.
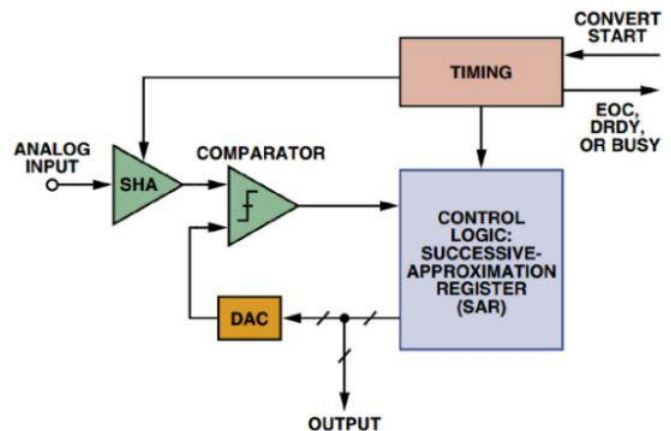

Fig. 1. Basic successive approximation register ADC architecture

In order to process rapidly changing signals, SAR ADCs have an input sample-and-hold (SHA) to keep the signal constant during the conversion cycle. The conversion starts

when the Digital to Analog Converter (DAC) output is set to midscale. The comparator determines whether the SHA output is greater or less than the DAC output, and the result (the most-significant bit (MSB) of the conversion) is stored in the successive-approximation register (SAR) as a one or a zero. The DAC is then set either to 1/4 scale or 3/4 scale (depending on the value of the MSB), and the comparator makes the decision for the second bit of the conversion. The result (one or zero) is stored in the register, and this process continues until all of the bit values have been determined. A logic signal (EOC, DRDY, BUSY, etc.) is asserted at the end of the conversion process. The acronym, SAR, which actually stands for successive-approximation register the logic block that controls the conversion process is universally understood as an abbreviated name for the entire architecture.

II. LITERATURE REVIEW

A. Design techniques for high-speed, high resolution comparators

In this paper the authors describe precision techniques for the design of comparators used in high-performance analog-to-digita1 converters employing parallel conversion stages. The design of fast precision comparators requires careful trade-offs among parameters such as speed, resolution, power dissipation, and input capacitance. The speed of a comparator is often limited by its preamplifier overdrive recovery, while the resolution is constrained by the input offset of its latch. Thus, if the latch offset is reduced in a reliable way, the preamplifier can be designed for lower gain and hence faster recovery.

A CMOS comparator which utilizes a new offset cancella-tion technique has also been introduced. To achieve a small residual offset, this comparator combines a preamplifier and a regenerative latch, both with offset cancellation. This topology significantly relaxes the preamplifier gain requirements, allow-ing high speed and low power dissipation. The comparator maintains an offset of less than 300 pV at conversion rates up to 10 MHz while dissipating 1.8 mW[1].

B. High-speed low-power comparator for analog to digital converters

In this paper authors proposed a high speed low power comparator. In this circuit, the voltage variation of the first stage is limited to Vdd=2. So that the power consumption of the first stage which is the main part of the total power consumption is reduced. Moreover, the speed of the circuit and maximum input common mode range is increased. That is because owing to the higher common mode voltage at the output of the first stage, the delay of the latch stage is reduced. In the proposed comparator, at the reset phase, the node voltages of the first stage are discharged to VS (Vdd/2) which is large enough to keep the second stage active. There is no delay time to change the output voltages of the first stage to the level of an NMOS voltage threshold to activate the latch stage[2].

C. Kickback noise reduction techniques for CMOS latched comparators

The building block of virtually all analog-to-digital con-verter architectures is latched comparator. It uses a positive feedback mechanism to regenerate the analog input signal into a full-scale digital level. The large voltage variations in the internal nodes are coupled to the input, disturbing the input voltagethis is usually called kickback noise. Two kickback noise reduction techniques are discussed here. The first technigue can be used in Class-AB comparator; the second technique can be used in any latched comparator. In first technique, minimize the voltage variations on the drains of the differential pair. Those nodes are isolated from the regeneration nodes using switches, which open during the regeneration phase. An alternative path for the current of the differential pair must be provided, in order to keep the drain voltages near the values found in the reset phase. Also it uses a neutralization technique. In the second technique, insert the sampling switches before the input differential pair, which are opened during the regeneration phase. Most power efficient comparators generate more kickback noise[3].

D. Low-power technique for dynamic comparators

Comparators are the key building blocks of the ADCs. The speed and the power consumption of the comparators play an important role in the characteristics of todays commonly used ADCs, such as successive approximation register (SAR) and flash ADCs. Static comparators have been used for years in the past. However, they suffer from high-power consumption and low speed. Dynamic comparators were proposed to reduce the power consumption and enhance the comparison speed. In the dynamic comparators, a pre-amplifier stage amplifies the input differential signal, and then a latch stage amplifies that voltage to the level of Vdd and Gnd. The positive feedback nature of the latch circuit provides a high speed comparison.

A low-power technique to reduce the power consumption of the dynamic comparators is presented. Using this technique, the pre-amplification phase of the comparator is stopped with-out any effect on the dynamic behaviour of the comparator. Therefore, the power consumption of the pre-amplifier stage which is the main part of the total power consumption is re-duced significantly. Simulation results in various comparators reveal that the proposed technique reduces the total power consumption by more than 50%[4].

E. A low-power low-offset dynamic comparator for analog to digital converters

A comparator comprises a cross coupled circuit which produces a positive feedback. The mismatch between the cross coupled circuits of conventional comparators, determines the trade-off between the speed, the power consumption and offset of the comparator. Here introduces a new low-power low-offset dynamic comparator for analog-to-digital converters. This comparator benefits from two operational phases and two stages to reduce the offset voltage caused by the mis-match effect inside the positive feedback circuit. The proposed

comparator works with a special three phase signalling. The structure benefits from two phase signalling to cancel the mismatch of the inner devices. The offset voltage was obtained using analytical derivations as a function of mismatch and delay[5].

F. A lownoise self-calibrating dynamic comparator for high-speed ADCs

A high-speed, low-offset, low-power consumption compara-tor is very attractive for many applications, such as memory sensing circuits, analog to digital converters and data receivers. A low-offset, low-noise dynamic latched comparator using a self-calibrating architecture that does not require a preamplifier and a DAC is proposed. At 1 GHz, the proposed comparator can compare 1.0 mV input voltage with a low power con-sumption of 40 W/GHz. The proposed calibration technique and comparator topology are very effective for achieving a small area and low offset voltage comparator using a deep sub-micron CMOS technology. Conventionally two phase clocks were required, but for the proposed comparator only one phase clock is required, which leads to relaxed clock. The proposed architecture consists of a comparator, offset com-pensation current sources and a charge pump. The proposed offset cancellation technique thus achieves low offset voltage and low power consumption. Compared with a conventional comparator, the proposed circuit topology can improve the comparator noise and reduce the clock driving requirement[6].

G. Excess power elimination in highresolution dynamic comparators

In this paper, a straightforward method to reduce the power consumption of the dynamic comparators is presented. This method is implemented in all kinds of the two-stage dynamic comparators simply by adding two transistors in series with the current source of the pre-amplifier stage. In the two-stage dynamic comparators, the first stage (pre-amplifier stage) amplifies the input differential voltage. Then the second stage (latch stage) is activated and finishes the comparison. When the comparison is about to finish, the balance of the positive feedback of the latch stage tends to tilt toward one of the outputs; after this, to the end of the comparison, the need for additional pre-amplification gain which causes excess power consumption is eliminated. While reducing the power consumption significantly, this method does not affect the dynamic behavior of the comparator such as offset voltage or speed. This method reduces the power consumption by 30% to 58%[7].

H. Comparator power minimization analysis for SAR ADC using multiple comparators

This paper analyzes the optimal comparators that need to be used to achieve a desired overall performance at minimum power levels. Here an analytically tractable model of the MSE error of the SAR ADC has been derived. Based on this model, it shows that the comparison power allocated to each bit step need not be the same, since the voltage

distribution at the comparator input is different for each bit cycle. An optimization problem is, therefore, constructed to identify the optimal distribution of the comparator power budget among all bit steps. To reduce the implementation complexity, comparator noise allocation problem is also solved when fewer than N comparators are employed in an N-bit SAR ADC[8].

I. A new ultra low power high speed dynamic comparator

Today very high speed, low voltage circuits are widely used, such as bio-implantable circuits and ADC's. Comparators are considered as base block for analog to digital converters. This kind of systems need high speed and low power consump-tion. The comparator with pre-amplifier increases the power dissipation. This is pushing toward dynamic regenerative com-parators to improve this problem. Here we use cross coupled mechanism to improve dynamic operation of the comparator. A comprehensive analysis of the delay time in the comparator is also proposed[9].

J. A lowpower high-speed comparator for analog to digital converters

Nowadays, low-power design is the main trend in the design of electronic circuits. ADCs are integral parts of a wide range of applications such as portable devices and radios. Employing low-power high-speed ADCs is essential to heighten the over-all system performance. Comparators play an important role in commonly used ADCs, such as flash and SAR ADCs. Static comparators have been used for years, however, they suffer from high power consumption and limited speed. Dynamic comparators were presented to improve the speed and reduce the power consumption of the static comparators.

In this paper, a two-stage dynamic comparator with PMOS transistors at the input of the pre-amplifier and latch stages is proposed. This structure in addition to a predefined clocking pattern reduces power consumption. Moreover, the offset and speed trade-off is controlled efficiently. The proposed circuit provides a low-power high-speed comparator in equal offset voltage budget compared to the conventional comparator. The PMOS latch-stage of the proposed comparator provides a lower offset voltage, since PMOS transistors offer a better matching compared to NMOS transistors in CMOS technol-ogy. PMOS latch with a predetermined delay is used to achieve a small amount of offset and improves the speed. Also, this delay limits the voltage variation at the output nodes of the pre-amplifier stage. Therefore, the power consumption of the proposed comparator is reduced by a factor of two while the speed is improved by 76:2% compared to the conventional comparator[10].

III. System Description

A. Comparator

The circuit of comparator is shown in Figure 2. In contrast to the conventional comparator, a pMOS latch (a latch with input pMOS transistors) is used in the latch which is activated with a predetermined delay during the evaluation phase [t_{amp},

as shown in Figure 2(b)]. This delay is supposed to be the optimum delay. At the reset phase, the clk, clkb1, and clkb2 hold a logic 1 to discharge the output voltages of both preamplifier and latch to GND. At the evaluation phase, first the clk and clkb1 are toggled to logic 0 to start preamplification (charging the parasitic capacitors of O1+ and O1 nodes differentially). During this phase, the cross-coupled circuit increases the differential voltage ($V_{idl} = [V_{O1+}-V_{O1}]$) slowly (since $M_{4;5}$ are mostly in subthreshold region) and reduces the commonmode voltage ($V_{cml} = 0.5 [V_{O1+} + V_{O1}]$) to provide a strong drive for the input pMOS latch stage. Increasing V_{idl} (means larger preamplifier gain) further eliminates the effect of the latch on the input referred offset voltage. Also, larger V_{idl} results in a smaller latch delay. Decreasing V_{cml} enhances the speed of the comparator, since pMOS transistors are used at the input of the latch ($M_{13;14}$). Finally, clkb2 is toggled to logic 0 to activate the latch. Simultaneously, clkb1 is changed to logic 1 to turn off the current source of the preamplifier in order to avoid excess power consumption. Amplification of V_{id} is kept going during this phase because the cross coupled circuit is still working independently of the current source (M8). Meanwhile, V_{cml} is kept reducing by M_{35}.

The control signals are implemented using a local clock generator as shown in Figure 2(b), which consumes a small amount of power. The black inverter is designed carefully to adjust the delay. Instructively, the proposed comparator is robust against overlapped control signals, since overlapped signals only slightly affect the power consumption and have no effect on the precision.

In the comparator circuit, the delay of the evaluation-phase is long enough to achieve the minimum required preamplifica-tion gain for a given speed and latch offset elimination. Thanks to the cross-coupled circuit ($M_{3\ 5}$), during the first step of the evaluation phase, the differential voltage at O1+ and O1-nodes increases; however, the common-mode voltage of those nodes is kept low. Therefore, for a sufficient evaluation phase delay, t_{amp}, V_{cml} (= $0.5 [V_{O1+} + V_{O1}]$) is pulled down to activate the pMOS latch strongly. Also, the larger V_{idl} boosts the latching process (speed). Consequently, the delay of the comparator will be small and almost flat over a wide range of the input V_{cm}. Transition of clkb1 to logic 1 limits the power consumption of the preamplifier which is the main part of the total power consumption. In the meanwhile, the cross-coupled circuit continues preamplification at no cost of power consumption.

As another benefit, the delay time from beginning of the evaluation phase to beginning of the latching process is simply controllable and can be tuned at its optimum value. However, in the conventional comparator, delay is inevitably fixed to the required time to charge the output parasitic capacitors of the preamplifier to the level of an nMOS voltage threshold.

This comparator structure can also be implemented using nMOS transistors, i.e., latch and preamplifier with input nMOS transistors. This will result in a higher speed because of the inherent superiority of nMOS transistors over pMOS ones. The size of $M_{4;5}$ is chosen large enough to keep the output
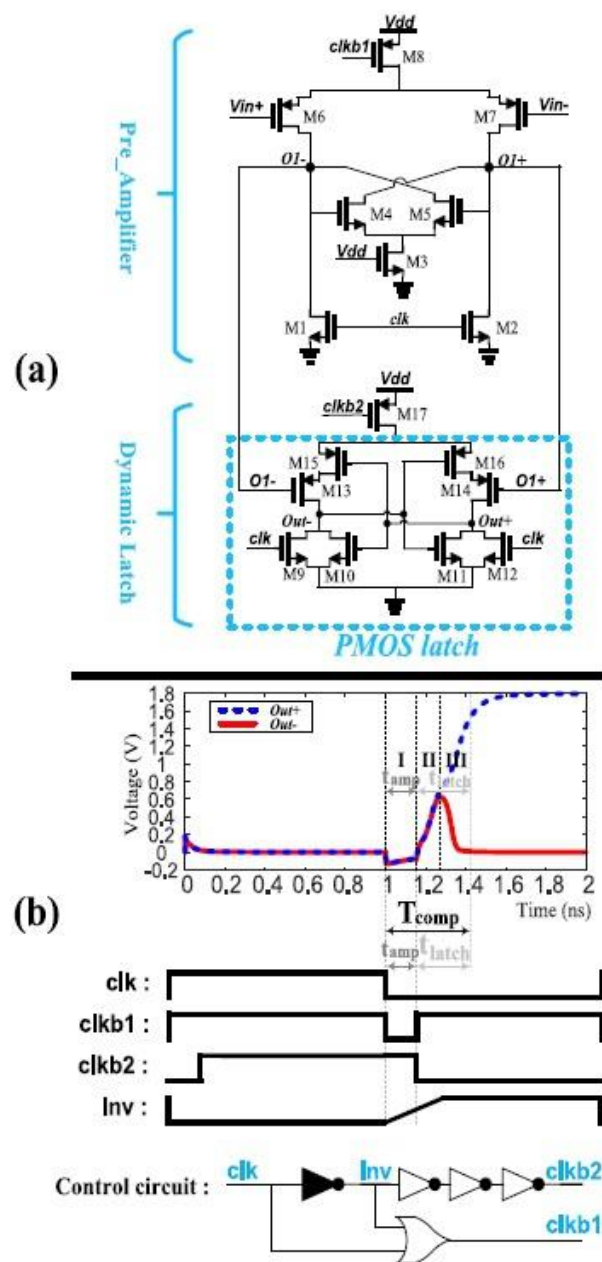

Fig. 2. (a) Proposed two-stage dynamic. (b) Its typical output waveform and clock signal.

common-mode voltage of the preamplifier small enough and increase the preamplifier differential gain.

B. DAC

The overall accuracy and linearity of the SAR ADC are determined primarily by the internal DACs characteristics. To achieve the desired accuracy and linearity, early precision SAR ADCs, such as the industry-standard AD574 uses DACs with laser-trimmed thin-film resistors. However, the process of depositing and trimming thin-film resistors adds cost, and

the thin-film resistor values may be affected after the device is subjected to the mechanical stresses of packaging. For these reasons, switched-capacitor (or charge-redistribution) DACs have become popular in newer CMOS-based SAR ADCs. In the switched-capacitor DAC, the accuracy and linearity are determined by high accuracy photo lithography, that es-tablishes the capacitor plate area, hence the capacitance and the degree of matching. In addition, small capacitors can be placed in parallel with the main capacitors to be switched in and out under control of autocalibration routines to achieve high accuracy and linearity without the need for thinfilm laser trimming.

The charge scaling DAC is the very popular DAC architecture used in CMOS technology. Figure 3 shows a parallel array of binary-weighted capacitors, totaling 2N C, is connected to an op-amp. The value, C, is a unit capacitance of any value. After initially being discharged, the digital signal switches each capacitor to either VREF or ground, causing the output voltage, v_{OUT} to be a function of the voltage division between the capacitors.
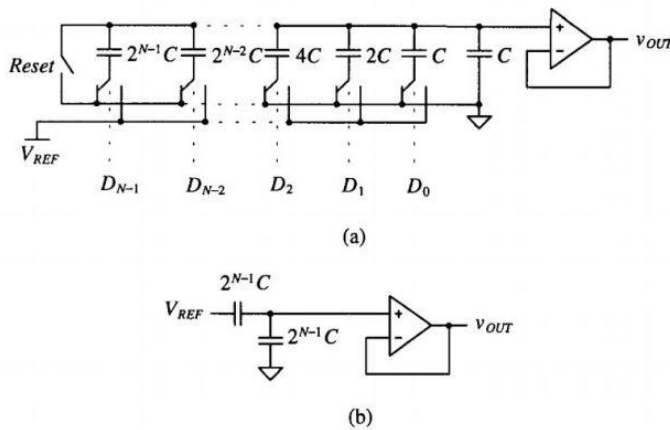

Fig. 3. (a) A charge scaling DAC, (b) the equivalent circuit with MSB = one, and all other bits set to zero

C. SAR Logic using Ring counter and Registers

The successive approximation register logic is the schedul-ing block that supplies circuit control signals and guarantees the operation accuracy of DAC and comparator. Using SAR control logic, successive approximation register ADC imple-ments the binary search algorithm.

As shown in Figure 4, this block has two register rows, which involves the cyclic shift register in the top row and the DAC driving registers in the bottom row. Based on the result of the comparator SAR control logic determines the value of bits sequentially. SAR architecture shown here is commonly used in SAR ADCs due to its straightforward design technique.

For each conversion, in clock cycle zero, the EOC signal is high and all Flip Flops outputs are reset to zero, and for the rest of cycles EOC is low. In the next clock cycle, the
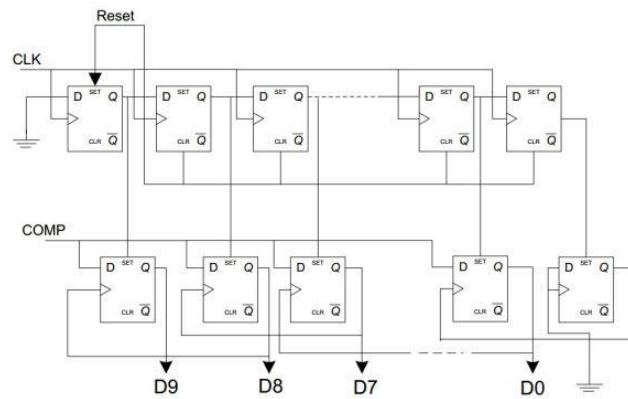

Fig. 4. SAR Logic using Ring Counter and Registers

most significant Flip Flop is set to one which corresponds to MSB of the digital word to the DAC. Then the counter shifts 1 through the Flip Flops from MSB to LSB. The Flip Flops which are used in this structure are set-reset D-FFs. For each clock cycle, one of the outputs in the ring counter sets a Flip Flop in the code register. The clock signal for the previous Flip Flop is used from the output of this Flip Flop which is set by the ring counter. This Flip Flop loads the result from the comparator at the rising edge of the clock. EOC signal turns to high, at the end of each conversion.

IV. RESULTS & ANALYSIS

This section presents the test setup and simulation results of the 8 bit SAR ADC designed using gpdk 180 nm. The internal modules SAR Logic, DAC and Comparator which are individually tested and characterized are interfaced to operate as a Successive Approximation Register ADC.

Figure 5 and Figure 6 shows the schematic diagram of conventional comparator and modified comparator used for SAR ADC.

Figure 7 shows the test circuit of SAR ADC with PWL input for 0V, 1V and 2v.

Figure 8,9 and 10 shows the test simulation results of * bit SAR ADC with PWL input for 0V, 1V and 2v.

Comparison of power consumed by conventional comarators and Modified comparator is shown in table 1.

TABLE I
COMPARISON ON POWER

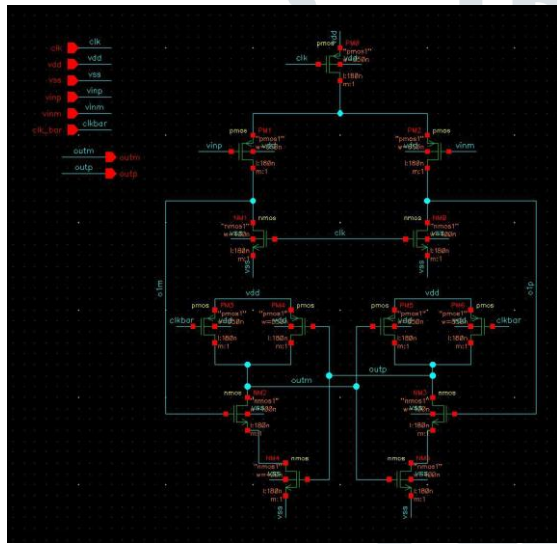| Case	Comparator	Average Power
1	Reference Comparator 1	65 w
2	Reference Comparator 2	34.4 w
3	Reference Comparator 3	29 w
4	Conventional Comparator	23.2 w
5	Modified Comparator	12.98 w
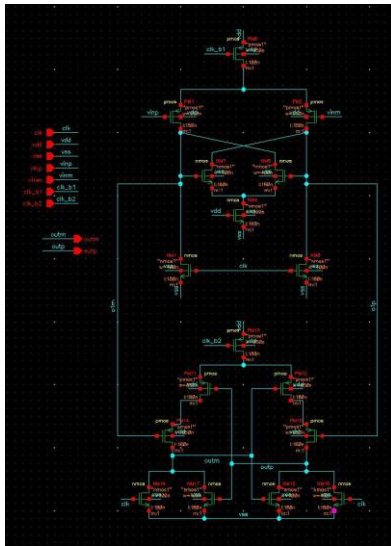
Fig. 5. Schematic of Modified Comparator

Fig. 6. Schematic of Conventional Comparator

Fig. 7. Test circuit of SAR ADc

Fig. 8. Output for v_{in}= 0v

CONCLUSION

Here an 8 bit SAR ADC is designed and simulated in 180 nm CMOS Technology at transistor level. Comparator being the crucial component of the architecture in maximizing speed and power efficiency, a comprehensive power analysis is presented. Designers can obtain an idea about the main contributors to the comparator power, delay from the analytical expressions, and fully explore the tradeoffs in dynamic com-parator design. The SAR Logic module was designed using ring counter and registers.

REFERENCES

[1] B. Razavi and B. A. Wooley, "Design techniques for high-speed, highresolution comparators", IEEE J. Solid-State Circuits, vol. 27, no. 12, pp. 19161926, Dec. 1992.
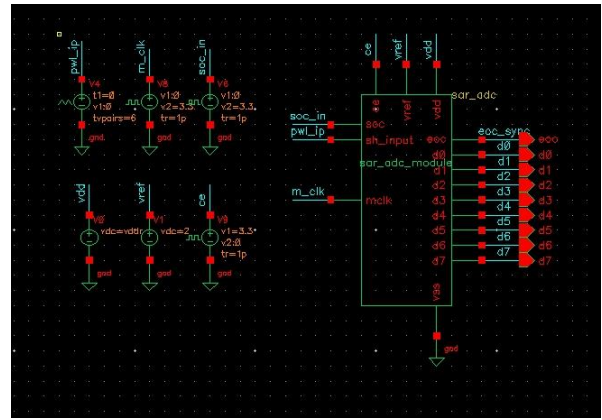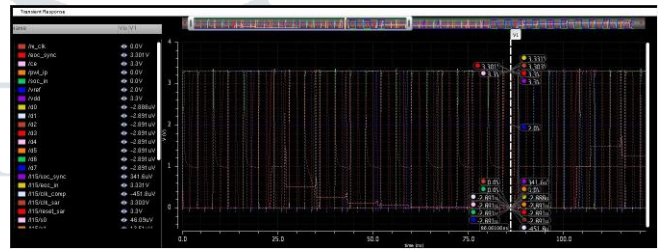
[2] A. Khorami and M. Sharifkhani, "High-speed low-power comparator for analog to digital converters," AEUInt. J. Electron. Commun., vol. 70, no. 7, pp. 886894, 2016.

[3] P. M. Figueiredo and J. C. Vital,"Kickback noise reduction techniques for CMOS latched comparators," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 53, no. 7, pp. 541545, Jul. 2006.

[4] A. Khorami and M. Sharifkhani, "Low-power technique for dynamic comparators," Electron. Lett., vol. 52, no. 7, pp. 509511, Apr. 2016.

[5] M. Hassanpourghadi, M. Zamani, and M. Sharifkhani, "A low-power low-offset dynamic comparator for analog to digital converters," Micro-electron. J., vol. 45, no. 2, pp. 256262, 2014.

[6] M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A lownoise self-calibrating dynamic comparator for high-speed ADCs," in Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC), Nov. 2008, pp. 269272.

[7] A. Khorami and M. Sharifkhani, "Excess power elimination in highres-olution dynamic comparators," Microelectron. J., vol. 64, pp. 4552, Jun. 2017.

[8] M. Ahmadi and W. Namgoong, "Comparator power minimization anal-ysis for SAR ADC using multiple comparators," IEEE Trans. Circuits Syst. I, Fundam. Theory Appl., vol. 62, no. 10, pp. 23692379, Oct. 2015.

[9] A. Rabiei, A. Najafizadeh, A. Khalafi, and S. M. Ahmadi, "A new ultra low power high speed dynamic comparator," in Proc. IEEE 23rd Iranian Conf. Elect. Eng. (ICEE), May 2015, pp. 12661270.

[10] A. Khorami, M. B. Dastjerdi, and A. F. Ahmadi, "A lowpower high-speed comparator for analog to digital converters," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), May 2016, pp. 20102013.

[11] S. Babayan-Mashhadi and R. Lotfi, "Analysis and design of a low-voltage low-power double-tail comparator" , IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 22, no. 2, pp. 343352, Feb. 2014.