Design of LDO Regulator in CMOS 45nm Technology

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Abstract: The transistor model is designed for outline of two different LDO Regulators having a differential stage stacked by current amplifier and the voltage feedback. The principal LDO has a consistent bias current. The LDOs were analysed to verify the transistors operations from weak inversion to strong inversion. It is demonstrated that in these LDOs the output voltage might be higher than the input reference voltage at minimum load current, and both the circuits begin "to follow" to achieve desired voltage with respect to load current depending on bias voltage. This paper additionally concentrates on outlining a particular LDO Regulator to fulfill the given requirements. The circuits were intended for 45 nm gpdk CMOS Technology and simulated in CADENCE Spectre tool.

Index Terms **- LDO, Weak inversion, Moderate inversion, Strong Inversion, regulator.**

INTRODUCTION

By the year 2020 it is expected that corresponding to every human being there would be seven connected devices. These connected devices will usher in the Internet of Things (IoTs) and would percolate every aspect of human life, changing the human experience at a fundamental level [8].LDO Regulator is one of the main block of power management system which is used in portable battery power system because of its various properties such as consistent and stable output voltage free of load impedance, input voltage variety, temperature and time requires to discharge battery. This leads to essential stability improvement and noise reduction for other sub circuits. Since the technology forces in compelling creators to configuration circuits working at bring down supply voltages, the LDOs are perfect for furnishing various voltage levels and work with a fairly low dropout voltage. LDOs are likewise fit for limiting current utilization down to microamperes, which is significant for current utilization of the sub-blocks in rest mode. This LDO regulator used to drop the DC-DC voltage. The cadence tool kit consists of several programs for different applications such as schematic drawing, layout, verification and simulation. Analog circuits are designed in Cadence Virtuoso and simulation is done on Spectre platform. This work focuses on designing an LDO voltage regulator in 45 nm process with gpdk45 process design kit. Specified output voltage is 1.8 V under all load conditions. In international scenario, the proposed LDO can operate from a supply voltage of 3.3–3.5 V with a minimum dropout voltage of 0.5 V worked at University of Missouri-Kansas City, US[8]. And also paper presented on “A Transient-Enhanced Fully-Integrated LDO Regulator for SoC Application”, in which the LDO is designed in a 130 nm CMOS process with 1.2 V regulated output and 200 mV dropout voltage[9].

II. SIMPLE LDO REGULATOR

The simple LDO Regulator circuit is shown in fig.1.

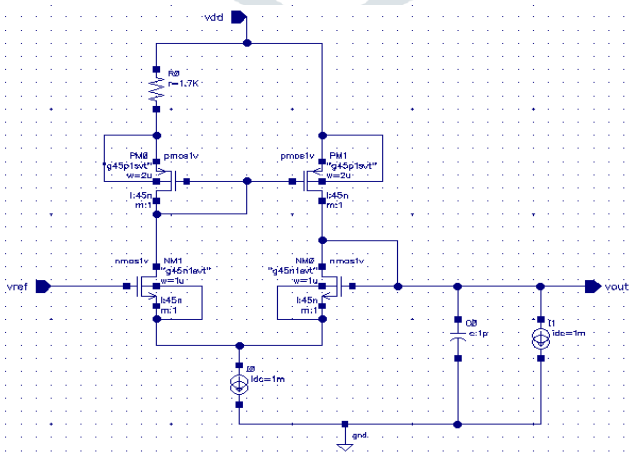

Fig.1 Simple LDO Regulator[1].

One can see that the right estimation of the circuit load characteristic requires the transistor model (in any event, for PM1 transistor in fig.1) which plainly portrays the progress from weak to strong inversion. This paper depicts such a model, and demonstrates the LDO voltage characteristics. It is additionally appeared as the most effective method to do estimations if there is transistor biasing.

To increase LDO efficiency, the proper small bias current to be picked, and the current gain is picked up A_W as large as would be prudent. To increase gain it includes a resistor R (Fig. 1) in the source circuit of MP0.

Assuming that for all values of $I1$ and I 2 one has approximately equal gate-source voltages of NM0 and NM1 transistors, the output voltage V_{out} should be approximately equal to the input voltage V_{ref} [1].

Effective answers for outlining power delivery networks for Internet of things (IoT) are clarified underneath. However, the longing to increase their efficiency may come about, as demonstrated as follows.

When the load is absent, the transistors in both circuits are operating in weak inversion; when the load is increasing the pass transistors in both circuits are moving to strong inversion [1].

The LDO Regulator can be analysed in two Cases as follows:

Case (1): Designing the circuit of Fig.1 with R=1.7KΩ in CADENCE Tool for following parameters.

L=45nm, W_n=1um, W_p=2um, V_{ref}=1.8V, V_{dd}=3V, I_0=1mA, I_1=1mA, V_{out}=1.78V.

Case (2): Designing the circuit of Fig.1 for R=0 in CADENCE Tool for following parameters.

V_{dd}=3.6V, V_{ref}=1.8V, L=45 nm for all mosfets, W_n=5um, W_p=10um, V_{bias}=1.15V, I_1=0.85mA, V_{out}=1.7825V.

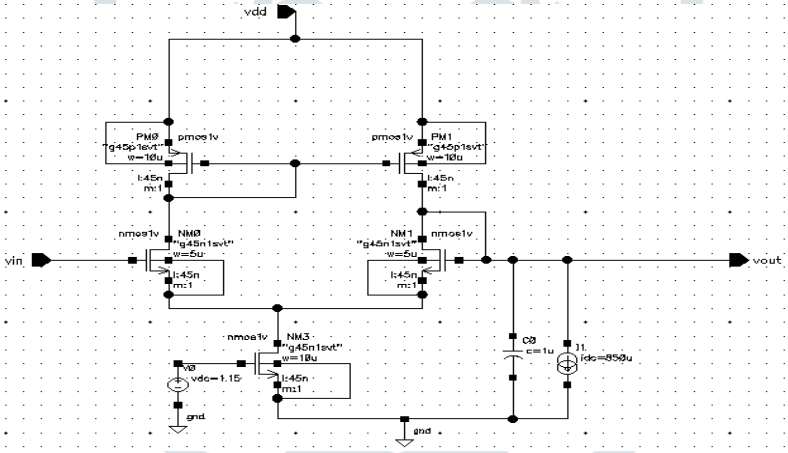

Fig.2 LDO Regulator with Transistor Bias[1].

III. COMPLETE LDO REGULATOR

With the help of the Fig.1 which is reference Circuit, complete LDO Regulator circuit is designed and simulated for specific input and reference voltage to get required output voltage.

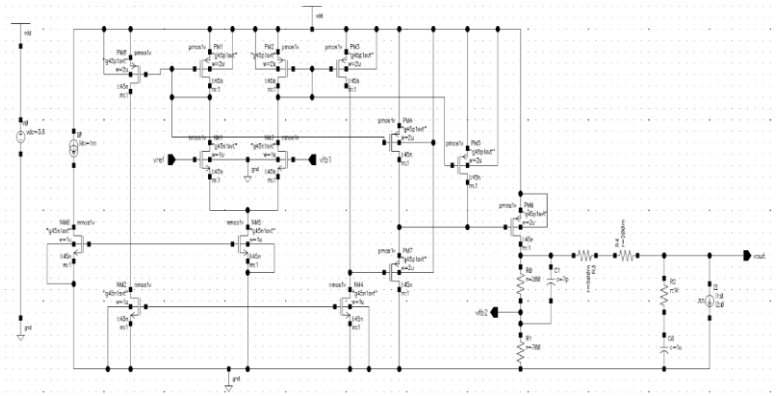

Fig.3 LDO Regulator Circuit [7].

Complete LDO Regulator designing has various components including error amplifier, pass element, feedback circuit, voltage divider circuit, load circuit.

a. Voltage reference circuit:

Voltage reference sets the working purpose of the error amplifier, in this manner it is the beginning stage of all regulators. By and large this voltage reference is of the band-gap compose, in light of the fact that it gives capacity to work at low supply voltages, and its precision and its steadiness under fluctuating temperature is adequate for design of linear regulators. The transistors of voltage reference circuits are PM0, PM1, NM1, and NM3.

b. Error amplifier design:

Error amplifier design must be kept as basic as could be expected under the circumstances, so it doesn't draw excessive current. The less current branches it has, the less current it draws from the input. Error amplifier takes the voltage scaled down by the voltage divider composed of resistors R1 and R2. $V_p = V_{out}R_1/ (R_1 + R_2)$, compares it with the reference voltage and adjusts the resistance of the pass element to drive the error signal ($V_{err} = V_p - V_{ref}$) as close to zero as possible[7]. The transistors of error amplifier are PM0, PM1, PM2, PM3, NM1, NM2, NM3, NM4.

c. Feedback network:

Resistive feedback network scales the output voltage V_{out} for the examination against the reference voltage V_{ref} by the error amplifier. Due to the fixed V_{ref} the best way to change the output voltage is through ratio of R2/R1[7].

d. Series-Pass element:

Pass element is exchanging large currents from input to the load and is driven by the error amplifier in a feedback loop. There are different topologies of pass components yet since this works is concentrating on outline of a LDO in a CMOS technology; just MOSFET pass components will be depicted.

In the event that the load current builds, the load capacitor supplies the current to the stack, this progresses the output voltage which is the detected by the resistive divider and fed back to the amplifier which regenerates the adjustment in the output voltage by enabling more current to move through the pass transistor.

Technology Parameters:

Parameters	Range
Input voltage	3.6V
Load Current	0.85mA-1mA
Bias current	1uA
Gate length	45nm
Output Capacitor	1uF

IV. RESULTS

The LDO circuits of both cases are simulated in CADENCE spectre tool. The below graphs shows the results of the circuits.

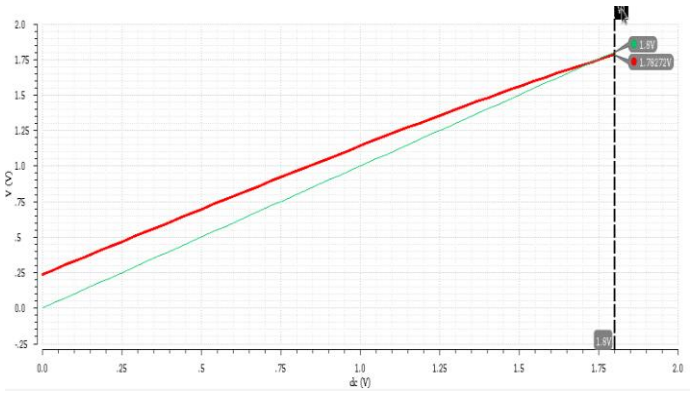

Fig.4 DC Analysis in CADENCE Spectre for V_{ref}=1.8V

The Fig.4 graph shows the simulated result of parameters mentioned in the case(1). When the load is present in the circuit and the gate voltages in NM0 and NM1 transistors are equal the output voltage is close to the input voltage V_{ref} which can be noticed in

above graph.

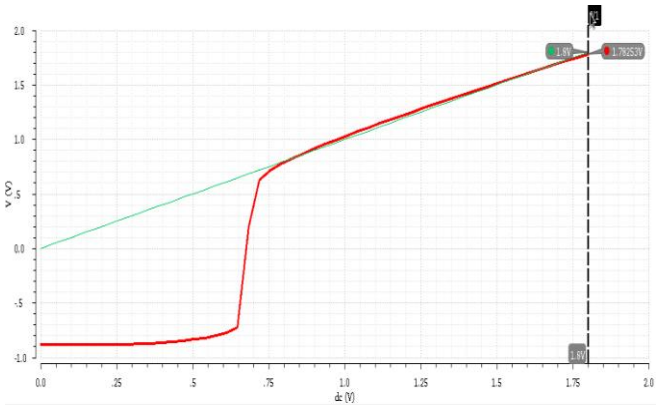

Fig.5 DC Analysis of Circuit in Case(2) for Vref=1.8V

The Fig.5 shows the simulated result of Fig.2 with case (2) parameters. The Bias current is replaced with transistor voltage, device parameters are also varied and R=0 to get the same output voltage 1.8V. Since, the gate voltages of NM0 & NM1 are equal so the output voltage is near to input voltage V_{ref}.

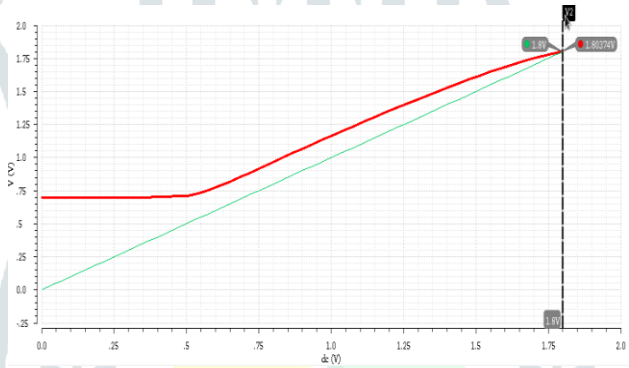

Fig. 6 DC Analysis of complete LDO Regulator.

Fig.3 is simulated to get the above graph. Here V_{ref} =1.8V and V_{in}=3.6V .We got the output voltage of 1.8037V. The pass element passes the dropped voltage to feedback circuit which is compared with error amplifier and the desired output is generates according to reference voltage which is shown in above graph. Here only V_{ref} and V_{out} graph is shown.

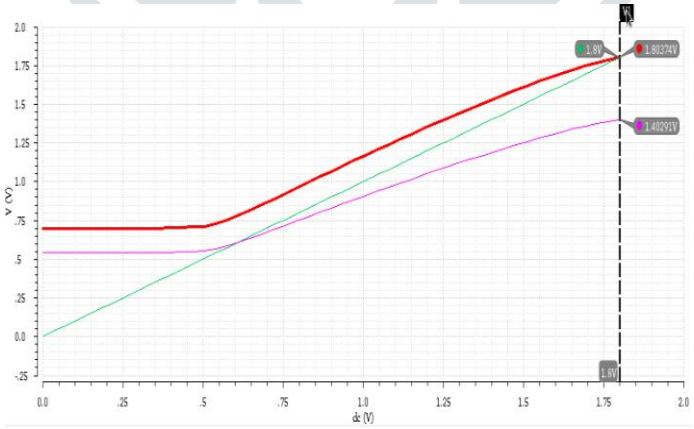

Fig.7 DC analysis with feedback graph of the complete LDO Regulator.

The pass element passes the voltage to feedback circuit, if the voltage is less than the reference voltage the error amplifier detects and amplifies to required output voltage. The fig.7 shows the feedback voltage value and also amplified final output voltage.

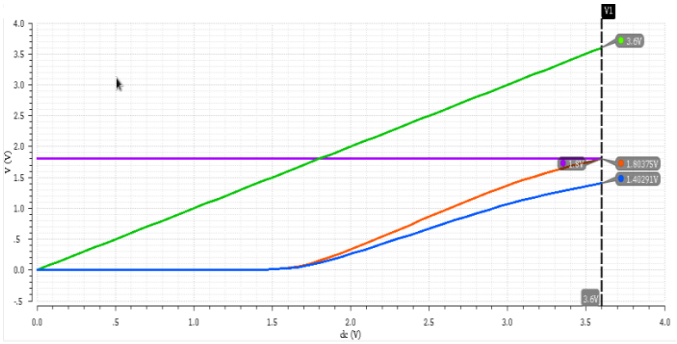

Fig.8 DC analysis for V_{in}=3.6V.

Fig.8 shows the complete graph with all parameters such as input voltage is 3.6V, reference voltage is 1.8V, feedback voltage is 1.40291 shown in above graph and the output voltage got is 1.80375V. Here the different lines indicates different input and outputs, as the voltage flows through different components of the circuits the output voltages are shown in graphs with voltage values.

V. CONCLUSION

A simple transistor model for IoT circuits where transistors are operating in wide range (from weak via moderate to strong) of inversion is proposed. The results of calculations and simulations, for such simple model, are analysed. Both cases gave same output value. Instead of bias current we have used bias voltage in second case to provide biasing for the circuit It finds its application in the power delivery circuits for IoT.

Complete LDO Regulator circuit is designed and simulated. The desired output for the LDO regulator is achieved.

VI. FUTURE SCOPE

We can simulate the fig.3 further to calculate the total power for the LDO Regulator in CADENCE Spectre. Also the circuits can be scaled down for 16nm technology and simulation is done in different simulation tools according to the design variations.

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