# Pefformance and Electrical Charactrization of of Ge-Nanowire Field Effect Transistor

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*Abstract:- In Nanoscale regime some disadvantages are associated with the existing MOSFETs, n***anowire FET devices are one of the alternative semiconductor devices which have potential to replace the existing MOSFET technology in future. In this paper a simulation study is reported that how Ge nanowire FET devices can replace the MOSFETs. In devices metallic contacts are considered as source and drain as well as Ge nanowire is considered as a channel between source and drain. Different simulations are performed in nanoHUB with different channel length to analyze the impact of different factors on electronic transport inside the nanowire FETs. Analysis are observed with the scaling the channel length of the nanowire FETs. It is observed through simulation results that at low gate voltage, drain current and the sub-threshold swing increases.**

**Keywords:** MOSFET, NW-FET, Threshold-voltage, Ge-Nanowire FET.

## I. INTRODUCTION

The bulk process of manufacturing the MOSFET is relatively simple and is widely adopted by the semiconductor industries. According to ITRS device scaling is important factor to achieve the goal of semiconductor industry, but scaling beyond 20 nm is quite complicated to maintain all the device parameter further [1]-[4]. Many efforts are going on parallel to replace the existing MOSFET technology worldwide. In scaling functionality and reliability of the device has to maintain at small dimension, because of this activity short channel length comes into the pictures along with some other parameters. Effect of this causes the reduced sub-threshold swing which further causes to difficulty in turn on the device. In MOSFET (metal oxide semiconductor field effect transistor) technology, generally two device structures are studied widely, the first one is bulk structure and second one is silicon on insulator[5]-12]. In bulk structure any transistor is fabricated directly on the substrate of semiconductor whereas in SOI transistor is fabricated on thin layer of silicon and it is separated with a layer of insulator from the substrate.

## II. GERMANIUM STRUCTURE

In nano-regime many devices has capability to replace the existing MOSFET technology but still research are going on for mass production. Ge-Nanowire FET has immerges as a potential candidate for future semiconductor devices. Silicon and Ge are widely available material in the Earth, whereas the crystal of silicon structure is highly stable. Because of good electrical and mechanical properties of Si material it is best suitable for semiconductor industry [13]-18]. SiO2 is a native oxide of Si which is widely used as insulator in the in semiconductor devices.

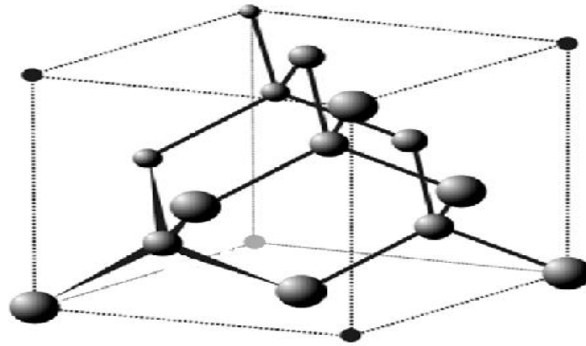

Fig. 1. Cross view of Ge structure

## III. RESULT ANALYSIS

For simulation of Ge nanowire FET device, the length of source and drain are fixed to 10nm and the channel length is in range of 12 to 4 nm. Other parameter like oxide-thickness of the device as well as the diameter of the nanowire are considered as 2.5nm and 1 nm respectively. Doping concentration of 2e+20/cm$^3$ is considered for donor,source and drain doping concentartion, whereas 1e+06/cm$^3$is fixed for acceptor, source and donor concentration.

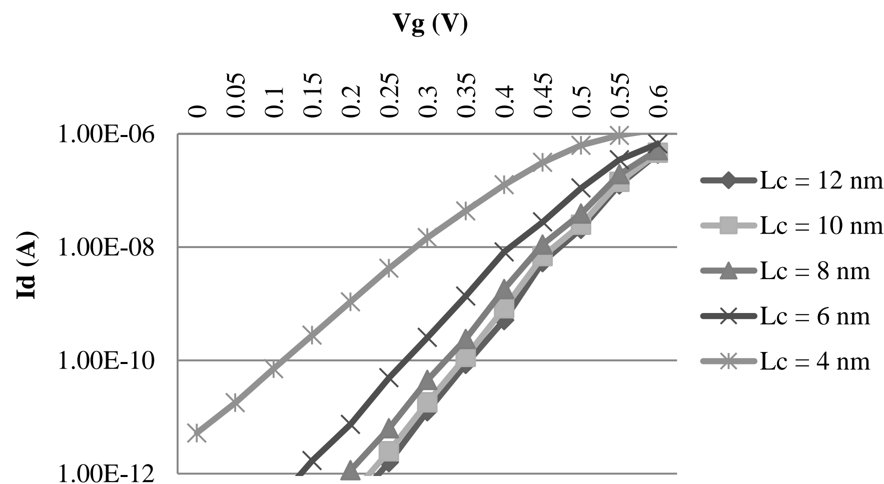


Fig.2. I-V plot for Ge-nanowire FET device

## IV. CONCLUSION

In nanometer regime nanowire FET devices have some promising characteristics which will lead a potential candidate for future semiconductor device. A new class of devices is represented by nanowire FET. This paper is focused to the electronic-transport of Ge nanowire FET with variable channel length. The simulation results shows that while reducing the channel length of the nanowire FET device, a substantial increment in sub-threshold swing and drain current is observed at low gate voltage, which on is very important for nanometer devices.

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