JETIR.ORG ISSN: 2349-5162 | ESTD Year : 2014 | Monthly Issue
JOURNAL OF EMERGING TECHNOLOGIES AND INNOVATIVE RESEARCH (JETIR)
An International Scholarly Open Access, Peer-reviewed, Refereed Journal

PROGRAMMABLE ARRAY LOGIC(PAL) AND PROGRAMMABLE LOGIC ARRAY(PLA) USING REVERSIBLE LOGIC GATES

Vanaparthi Poornima, Mr. Kalyan Raghu
M.Tech Student, Professor
Department of Electronics & Communication Engineering
International School of Technology & Sciences (Approved by AICTE & Affiliated to JNTUK Kakinada), Rajahmundry, India

Abstract: Reversible logic is currently a new research area. The goal of this white paper is to design and synthesize programmable array logic (PAL) and programmable logic array (PLA) using reversible logic with minimal quantum cost. A PAL is a programmable logic device consisting of an array of programmable AND gates and fixed OR gates. A PLA is a PLD that contains programmable AND arrays and programmable OR arrays. PLDs are combinational circuits primarily used to implement Boolean functions of interest. Reversible Logic has its applications in various fields such as Quantum Computing, Optical Computing, Nanotechnology, Computer Graphics, and low power VLSI etc., Reversible logic has gained importance in recent years, mainly due to its low power consumption and low heat dissipation characteristics. This article proposes PAL and PLA designs with low heat dissipation and low power consumption. The designed circuits are analyzed in terms of quantum cost, garbage outputs and number of gates. The Circuit was designed and simulated using Xilinx software.

Index Terms – PAL, PLA, PLDS, Quantum Cost, Reversible Gates, Garbage Outputs, Number of Gates**.**

INTRODUCTION

With today's VLSI technology, power consumption has become a very important factor to consider. Power consumption and heat dissipation can be minimized by using reversible logic. Reversible logic circuits consume much less power than nonreversible logic circuits. Reversible logic finds unique applications in quantum computing, nanotechnology, optical computing, computer graphics, and low-power VLSI.

Reversible logic involves using reversible gates with the same number of inputs and outputs. H. There should be a one-to-one mapping between input vector lines and output vector lines. In reversible computation, reversible gates are executed both forward and backward. A device satisfies the second law of thermodynamics if it satisfies the above two conditions. This ensures that bits of information are retained without being erased and heat is not dissipated

Quantum cost plays an important role in logical reversibility. A high quantum cost increases the area of the circuit, thereby increasing the propagation delay. However, the quantum cost does not affect heat dissipation. Latency is one of the most important cost metrics. A switchable circuit design can be modeled as a series of discrete time slices. Depth is the sum of total time slices. In digital electronics, a binary decoder is a combinatorial logic circuit that converts binary integer values into associated output patterns. Ongoing research has produced various proposals for the design of combinational and sequential circuits. In this article, we propose programmable array logic (PAL) and programmable logic array (PLA) designs that use reversible logic with minimal quantum cost

PROGRAMMABLE LOGIC DEVICES

The need to complete designs quickly drives the development and evolution of programmable logic devices. The idea started with read-only memory (ROM), an array of organized gates, and evolved into system-on-programmable chip (SOPC), which uses programmable devices, memory, and configurable logic on the chip. This chapter presents the evolution from basic array structures like ROMs to complex CPLDs (Complex Programmable Logic Devices) and FPGAs (Field Programmable Gate Arrays). This topic can be looked at from different angles: logical structure, physical design, programming techniques, transistor level, software tools, as well as historical and commercial aspects. However, the treatment of this topic is at a more structural level. Describes gate-level structures for ROM, PLA, PAL, CPLD, and FPGA. This material is the level you need to understand how to configure and use CPLDs and FPGAs in your digital designs.

PROGRAMMABLE LOGIC ARRAYS

The cost of a ROM's high degree of flexibility is the large area occupied by the AND planes that form each min term of the ROM's input. Programmable Logic Arrays (PLAs) present a less flexible and less silicon-consuming alternative. In this discussion, we consider ROMs as logic circuits.

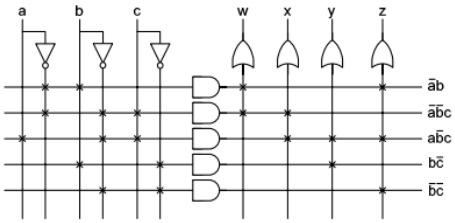

Fig : PLA Implementation

PROGRAMABLE ARRAY LOGIC

This circuit uses the equations for w, x, y, and z shown in Figure Recall that these expressions are a minimal implementation for the output of the example circuit and follow the k-map in Figure. The PAL structure in Figure 2.5 has a programmable AND plane and a fixed OR plane. Product terms are formed in the AND plane and three terms are used as OR gate inputs in the OR plane. This structure allows up to three product terms per output

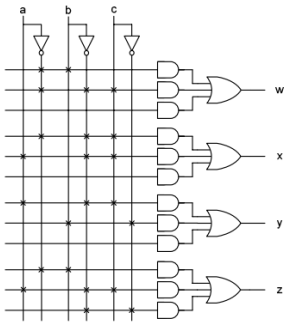

Fig: PAL implementation

Consider for example, PAL implementation of expression w shown below:

$w = a \cdot b \cdot c + a \cdot b \cdot c + a \cdot b + a \cdot b \cdot c$. Let us assume that this function is to be implemented in a 3-input PAL with three product terms per output and with outputs feeding back into the AND plane, as shown in Figure

ADVANTAGES OF USING PLDS

Advantages of using PLDs are less board space, faster, lower power requirements (i.e., smaller power supplies), less costly assembly processes, higher reliability (fewer ICs and circuit connections means easier troubleshooting), and availability of design software. There are three fundamental types of standard PLDs *PROM, PAL, and PLA*

THREE FUNDAMENTAL TYPES OF PLDS

The three fundamental types of PLDs differ in the placement of programmable connections in the AND-OR arrays. Figure shows the locations of the programmable connections for the three types

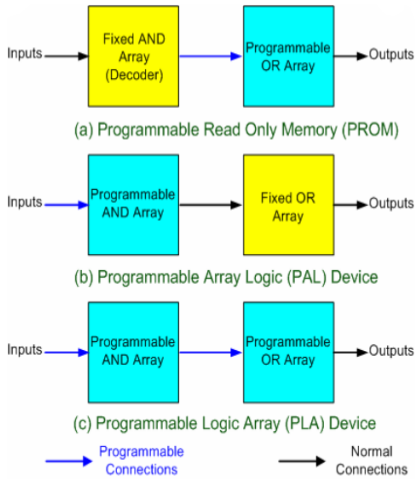

Fig: Three Types of PLD S

REVESIBLE GATE

Reversible logic is widely used in low power VLSI. Reversible circuits are capable of back-computation and reduction in dissipated power, as there is no loss of information [1]. Basic reversible gates are employed to achieve the required functionality of a reversible circuit. The uniqueness of reversible logic is that, there is no loss of information since there is one-to-one correspondence between inputs and outputs

REVERSIBLE LOGIC

Boolean logic is said to be reversible if the set of inputs mapped have an equal number of outputs mapped i.e. they have one-to-one correspondence. This is realized employing reversible gates in the designs. Any circuit having only reversible gates is capable of dissipating no power.

GOALS OF REVERSIBLE LOGIC:

Quantum Cost:

Quantum cost of a circuit is the measure of implementation cost of quantum circuits. More precisely, quantum cost is defined as the number of elementary quantum operations needed to realize a gate.

Speed of Computation:

The time delay of the circuits should be as low as possible as there are numerous computations that have to be done in a system involving a quantum processor; hence speed of computation is a very important parameter while examining such systems.

- **Garbage Outputs:**

Garbage outputs are those output signals which do not contribute in driving further blocks in the design. These outputs become redundant as they are not required for computation at a later stage. The garbage outputs make the system slower; hence for better Efficiency it is necessary to minimize the number of garbage outputs.

- **Feedback:**

Looping is strictly prohibited when designing reversible circuits.

- **Fan-out:**

The output of a certain block in the design can only drive at most one block in the design. Hence it can be said that the Fan-out is restricted to 1.

REVERSIBLE GATES :

There are many reversible gates such as Feynman, Toffoli, TSG, Fredkin, Peres, etc [3]. As the universal gates in boolean logic are Nand and Nor, for reversible logic, the universal gates are Feynman and Toffoli gates.

FEYNMAN GATE:

Feynman gate is a universal gate which is used for signal copying purposes or to obtain the complement of the input signal. The block diagram of Feynman gate is shown in fig.1:

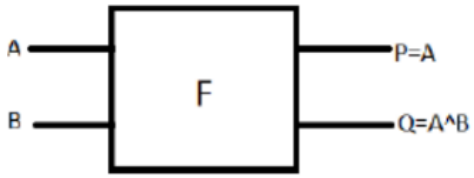

Fig: feynman gate

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Truth table

FREDKIN GATE

It is a basic reversible 3- bit gate used for swapping last two bits depending on the control bit. The control bit here is A, depending on the value of A, bits B and C are selected at outputs Q and R. When A=0, (Q=B, R=C) whereas when A=1, (Q=C, R=B). Its block diagram is as shown in fig. 2

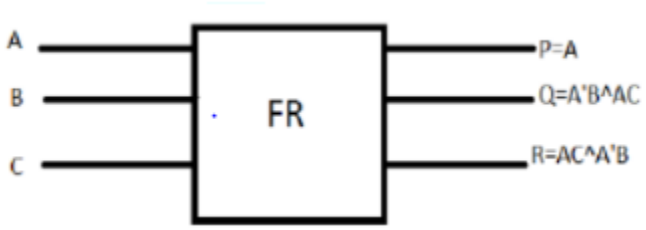

Fig: fredkin gate

INTRODUCTION TO VLSI

Very Large Scale Integration (VLSI) is the process of creating integrated circuits by combining thousands of transistor based circuits into a single chip. VLSI began in 1970s when complex semiconductor and communication technologies were being developed. the microprocessor is a VLSI device. the term is no longer common as it once was,as chips have increased in complexity into hundreds of millions of transistors

WHAT IS VLSI?

VLSI stands for "very large scale integration". This is the field which involves packaging more and more logic devices into smaller and smaller areas.

- Simply we say integrated circuit is many transistors on one chip.
- Design/ manufacturing of extremely small, complex circuitry using modified semiconductor material.
- Integrated circuit (IC) may contain millions of transistors each a few mm in size.
- Application wide ranging : most electronic logic devices

VLSI AND SYSTEMS

These advantages of integrated circuits translate into advantages at the system level:

- Smaller physical size
- Reducing power consumption has a ripple effect on the rest of the system
- Reduced cost

APPLICATIONS OF VLSI:

Electronic systems now provide a variety of tasks in daily life. electronic systems in some cases have replaced mechanisms that operated mechanically, hydraulically, or by other means; electronics are usually smaller ,more flexible, and easier to service .in other cases, electronic systems have created totally new applications. Electronic systems perform a variety of tasks, some of them visible, some are hidden:

- Personal entertainment systems such as portable MP3 players and DVD players perform sophisticated algorithms with remarkably little energy.
- Electronic systems in cars operate stereo systems and displays; they also control fuel injection systems, adjust suspensions to varying terrain, and perform the control functions required for anti-lock breaking systems.
- Transaction processing system, ATM.
- Medical electronic systems.
- Low cost terminals for web browsing still require sophisticated electronics, despite their dedicated function.

VERILOG

verilog synthesis tools can create logic circuit structures directly from verilog behavioral description and target them to a selected technology for realization. Using verilog, we can design ,simulate and synthesis anything from a simple combinational circuit to complete microprocessor on chip

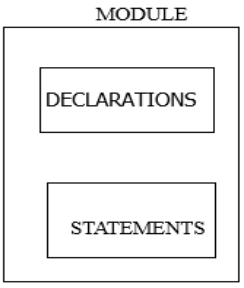

Fig: Program structure

SYNTAX:

Module Module_Name (port_name……..port_name);

Input declaration

Output declaration

Net declaration

Variable declaration

Parameter declaration

Function declaration

Task declaration

Concurrent_ statements

Endmodule

Module-signifies the beginning of a module definition.

Endmodule-signifies the end of a module definition.

EXISTING SYSTEM

NOT GATE:

Reversible logic gate's simplest example is the NOT gate. It simply inverts the bit value it handles. Not gate is 1-input/1-output gate.

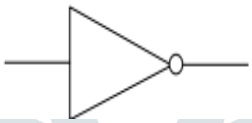

Fig: Not gate

CNOT GATE:

A reversible gate of considerable importance in quantum computing is the 2-bit controlled-NOT gate (CNOT). The effect of the "controlled" NOT gate is to flip the bit value of the second bit if and only if the first bit is set to-1

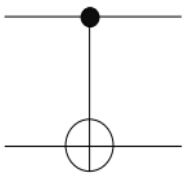

Fig: CNOT gate

REVERSIBLE DECODER:

In order to reduce the power dissipation in the decoder circuit, concept of reversible logic has been used. 2 to 4 decoder has been proposed using fredkin gates. Figure 8 shows the reversible 2 to 4 decoder.

Fig: Reversible 2 to 4 decoder

In fig IN1, IN2, E are three input signals and OUT0, OUT1, OUT2, OUT3 are four outputs. For decoder to operate E signal should be at logic „1". Three constant inputs that is logic 0 is provided to the circuit and GO1, GO2 are two garbage outputs. Since in all three Fredkin gates same number of inputs and outputs are there resulting in less power dissipation as compared to conventional logic gates. by making use of fredkin gates in similar manner any n to 2n decoder can be designed. Here n represents the number of inputs. In this paper a 4 to 16 decoder has been designed based on the same above said logic.

PROPOSED SYSTEM

In reversible PLDs structure, the fuses are replaced with a reversible fuse which is made of reversible Feynman gate and fredkin gate as shown in the below figure. The Feynman reversible gate acts as a duplicating circuit. It duplicates the output line into two output lines out of which one output line drives the next circuit and the other drives the second input of2×1 reversible multiplexer. The first input of reversible multiplexer is grounded so that when the enable signal 'E' is low it acts as an 'off' switch. The reversible multiplexer is made of Fredkin gate as shown in the below figure

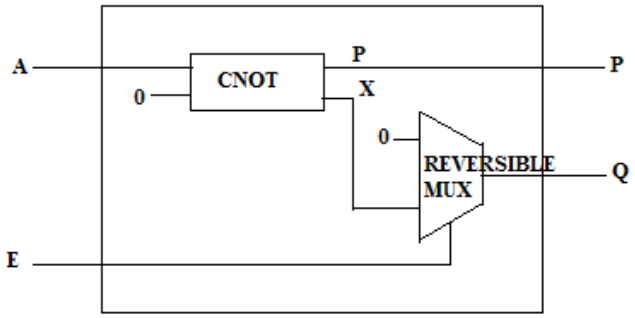

Fig: Reversible fuse

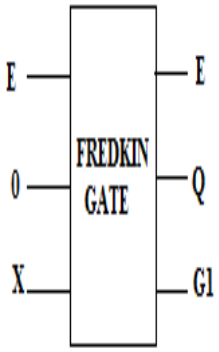

Fig: Reversible Mux

The fixed connections are replaced by CNOT gates in which the second input is set to '0' always. The CNOT gates solution for two remedies. It overcomes the feedback limitation and it acts as a fixed connection. The Design of PAL made of reversible logic which is programmed to perform the operation of the below Boolean algebraic equations is shown in the below figure11. The PAL consists of fixed OR gates array and programmable AND gate array.

F1 = I[1]I[2] + I[1]I[3]' + I[1]'I[2]'I[3] …… Eqn (1)
F2 = I[1]I[2] + I[1]'I[2]'I[3] + I[1]I[3] ……..Eqn (2)
F3 = I[1]I[3]' + I[1]I[2]I[3] …… Eqn (3)

Contemporary to irreversible PAL, the fuses are replaced with programmable reversible fuses and the fixed connections are replaced with the CNOT gates as shown in the figure11. The 'P' output of fuse drives the subsequent fuse and the 'Q' output of fuse drives the input of AND gate as shown in figure13. The output of AND gate drives the fixed connections i.e., CNOT gate. The 'P' output of CNOT gate drives the next fixed connection and the 'Q' output of CNOT drives the input of OR gate

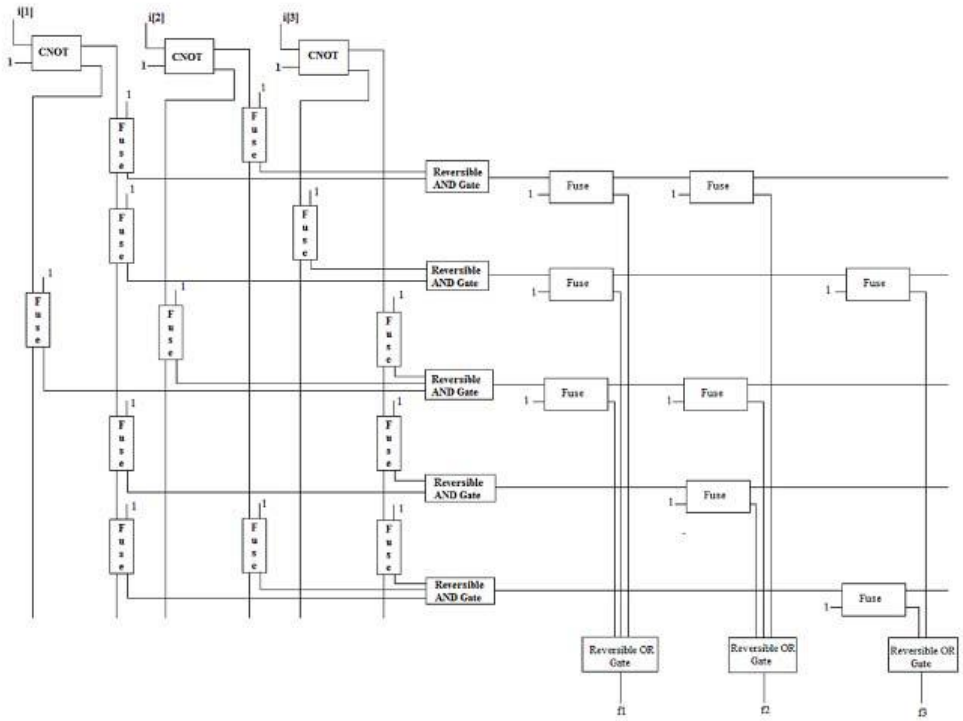

FIG : Circuit Diagram of Reversible PAL to Perform Boolean algebric equations operation

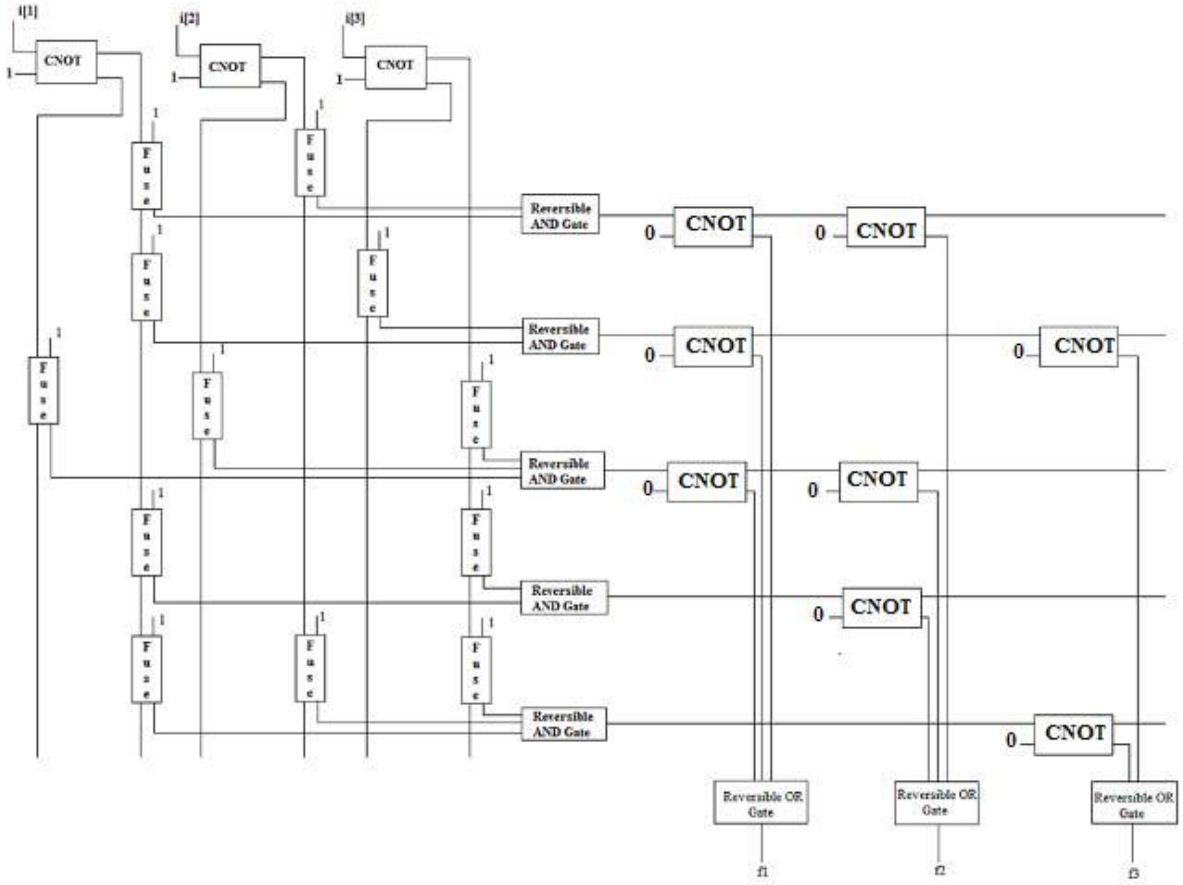

FIG : Circuit Diagram of Reversible PLA to Perform Boolean algebric equations operation

SOFTWARE TOOLS USED

XILINX SOFTWARE:

Xilinx Tools is a suite of software tools used for the design of digital circuits implemented using Xilinx Field Programmable Gate Array (FPGA) or Complex Programmable Logic Device (CPLD).

- Create Verilog design input file(s) using template driveneditor.
- Compile and implement the Verilog designfile(s).
- Create the test-vectors and simulate the design (functional simulation) without using a PLD (FPGA orCPLD).
- Assign input/output pins to implement the design on a targetdevice.
- Download bitstream to an FPGA or CPLDdevice.
- Test design on FPGA/CPLDdevice

A Verilog input file in the Xilinx software environment consists of the following segments:

- **Header:** module name, list of input and output ports.
- **Declarations:** input and output ports, registers and wires.
- **Logic Descriptions:** equations, state machines and logic functions.

End: end module

SIMULATION RESULTS OF PROPOSED CIRCUITS

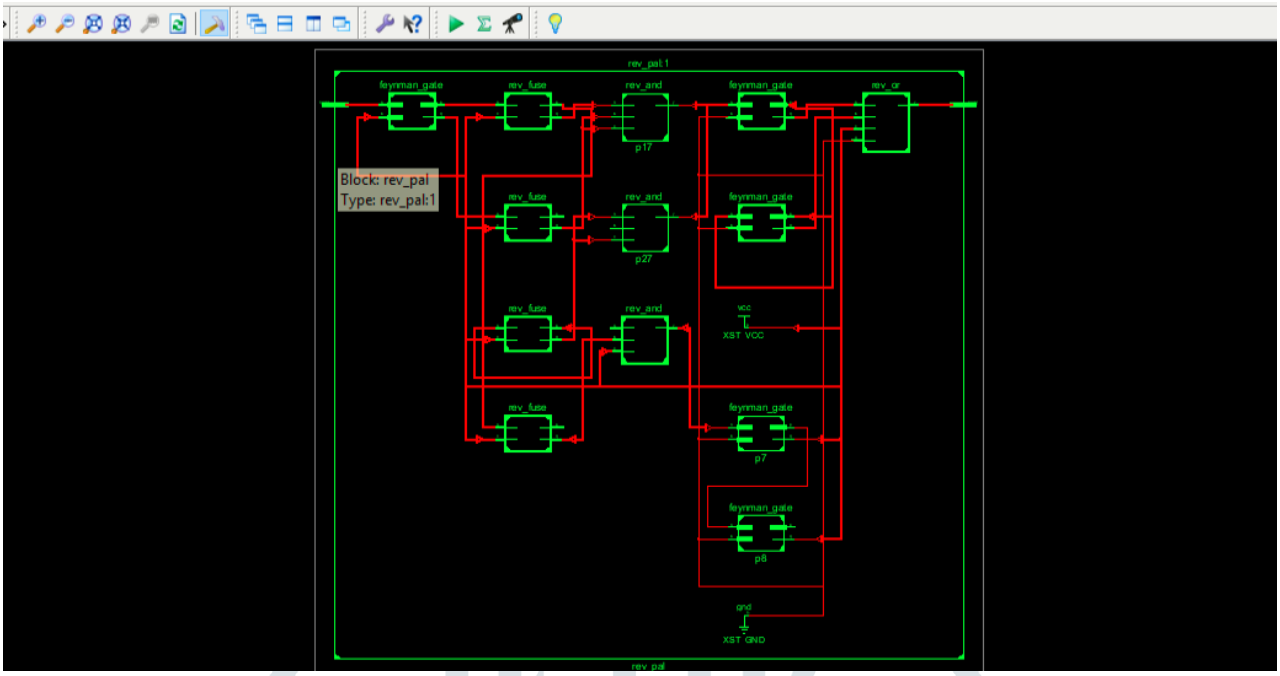

Fig: RTL Schematic of PAL implementing Boolean algebraic equations Eqn(1) to Eqn(3)

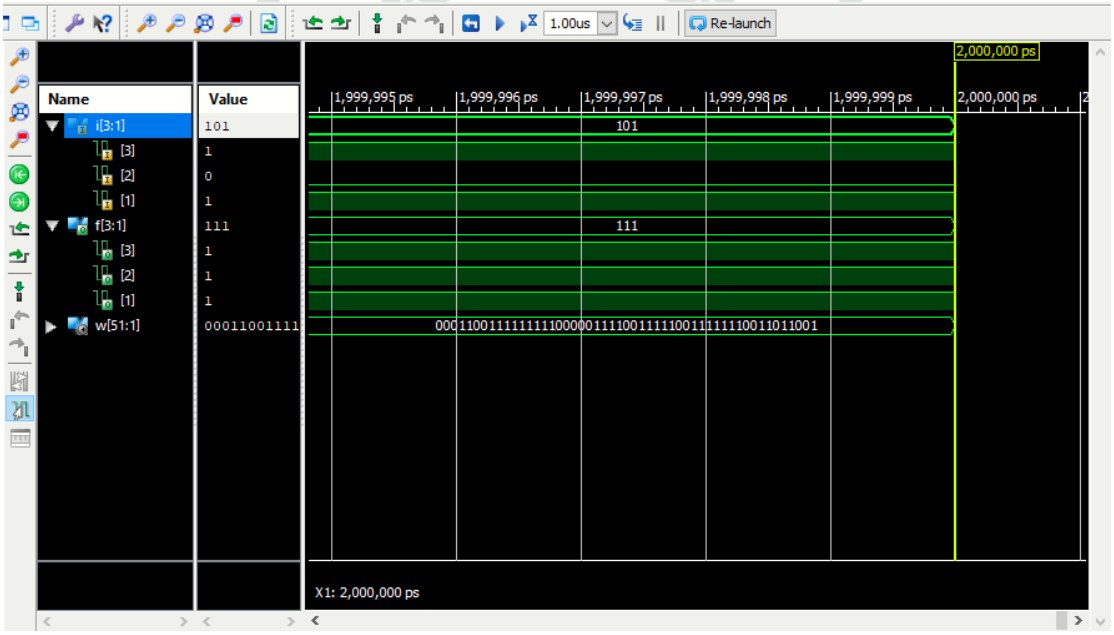

fig: simulated outputs for implementing Boolean algebraic equations using PAL

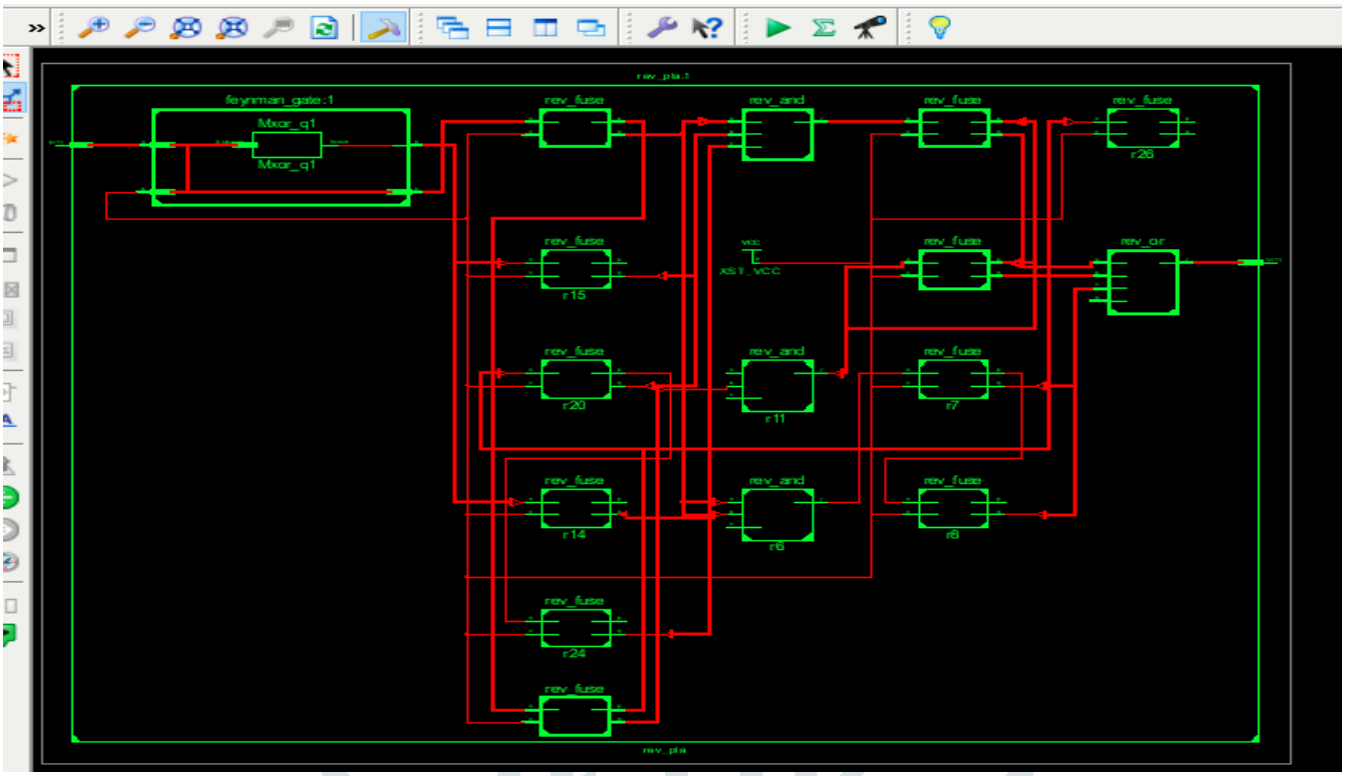

Fig: RTL Schematic of PLA implementing Boolean algebraic equations Eqn (1) to Eqn (3)

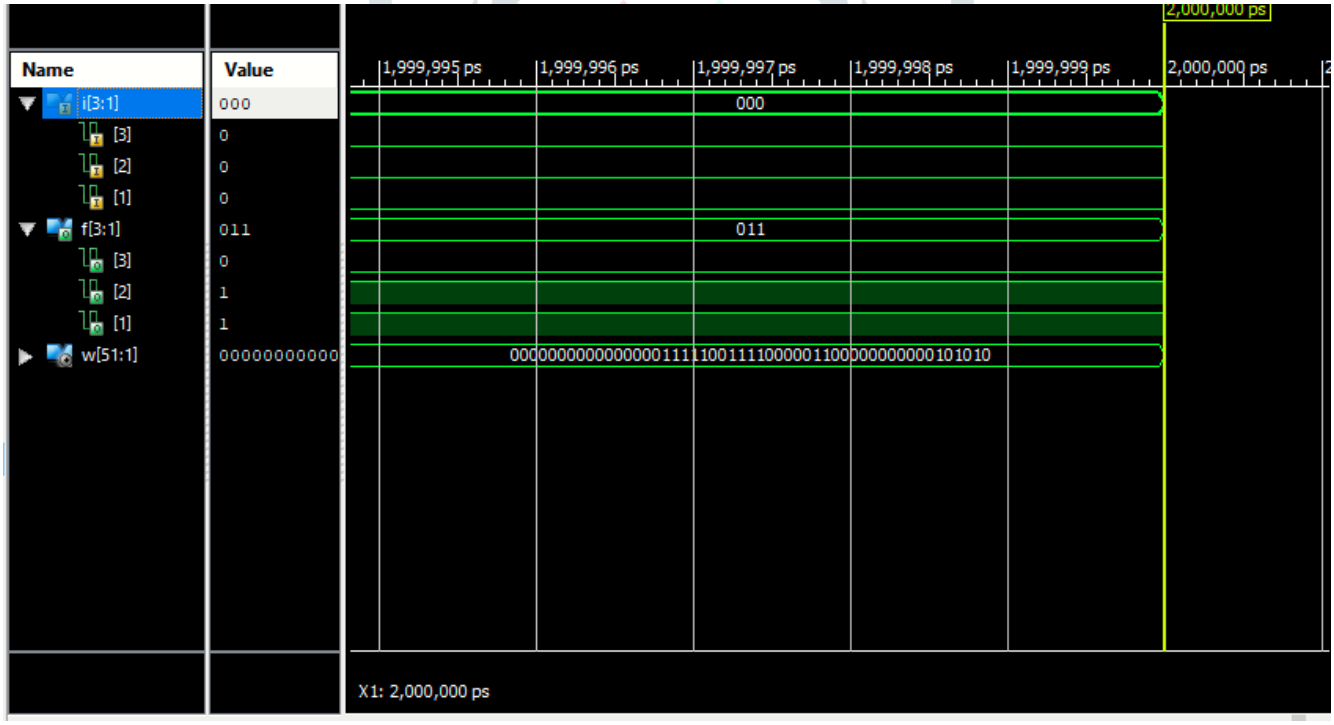

Fig: simulated outputs for implementing Boolean algebraic equations using PLA

ADVANTAGES & APPLICATIONS

11.1 ADVANTAGES:

1. The power dissipation will be zero if a network contains only reversible logic gates.
2. Minimum quantum cost.
3. Low power consumption.

11.2 APPLICATIONS:

1. Quantum computing.
2. Nano technology.
3. Optical computing.

CONCLUSION

In this paper, the method of realizing different Boolean functions using reversible PLDs like reversible PAL, reversible PLA, reversible GAL are explained. These circuits are designed for minimum quantum cost and minimum garbage outputs. To overcome the fan-out limitation in reversible logic circuits the concept of duplicating the single output to required number of output lines is implemented by using additional reversible combinational circuits. The reversible PLDs are implemented using a reversible fuse and Feynman gate. The reversible fuse is made of CNOT gate and fredkin gate which is used for programmable connections. Feynman gate with second input made zero is used for fixed connections. The reversible circuits used for designing programmable connections and fixed connections give minimum heat dissipation. By using this reversible PLDs eighty percentage of efficiency can be acquired in terms o heat dissipation. The time delay increases a little when compared to irreversible PLDs which can be termed as a disadvantage but it is negligible. The time delays for reversible PAL, PLA and GAL are 5.847nsec, 5.847nsec and 5.847nsec respectively. The time delay depends upon then Boolean expressions considered to program on the device.

The time delay is the function of quantum cost. The quantum cost increases with increase in length of Boolean function, because the number of programmable reversible fuses and Feynman gates (fixed connectors) increases with increase in length of Boolean function. If quantum cost increases, the time delay also increases. The reversible PAL, GAL finds more advantages when compared to the reversible PAL and PROM, since both OR array and AND array are programmable. Because of using reversible decoder in PROM the quantum cost becomes less when compared to the remaining PLDs. The propagation delay can be reduced if the quantum cost of the circuit is reduced further more. This can be termed as future scope for this project

REFERENCES:

1. R. Landauer, “Irreversibility and Heat Generation in the Computational Process”, IBM Journal of Research and Development, 5, pp. 183- 191, 1961.

2. C.H. Bennett, “Logical Reversibility of Computation”, IBM J.Research and Development, pp. 525-532, November 1973.

3. C H Bennett, "Notes on the History of Reversible Computation", IBM Journal of Research and Development,vol. 32, pp. 16-23, 1998.

4. R. Feynman,”quantum mechanical computers:, Optic News, vol. 11,pp 11-20, 1985.

5. A. Peres, “Reversible logic and quantum computers”, phys.rev.A,Gen.Phys., vol. 32, no. 6, pp. 32663276, Dec. 1985.

6. H.G Rangaraju, U. Venugopal, K.N. Muralidhara, K. B. Raja,”Low power reversible parallel binary adder/subtractor” arXiv.org/1009.6218,2010.

7. J.M. Rabaey and M. Pedram, “Low Power Design Methodologies,” Kluwer Academic Publisher, 1997.

8. T. Toffoli., “Reversible Computing”, Tech memo MIT/LCS/TM-151, MIT Lab for Computer Science 1980.

9. Y. Syamala, and A. V. N. Tilak, “Reversible Arithmetic Logic Unit”, Electronics Computer Technology (ICECT), 2011 3rd International, vol. 5, pp.207-211,07 july 2011.