Designing Of Modified Area Efficient Square Root Carry Select Adder(SQRT CSLA)

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***Abstract*—In the design of Integrated Circuits, The necessity of portable systems is increasing an area occupancy plays a vital role. Square Root Carry Select Adder (SQRT CSLA) is one of the fastest adders which is used in this data-processing processor to perform fast arithmetic functions. In this paper, an area-efficient square root carry select adder(SQRT CSLA design) by sharing Common Boolean logic term (CBL) is proposed The modified architecture has been developed using Binary to Excess-1 converter (BEC). Based on this modification 8-, 16-, 32-, and 64-b square-root CSLA (SQRT CSLA) architecture have been developed by using CBl. The proposed design has reduced area as well as power,but in this we study only for area with a slight increase in the delay.**

***INDEXTERMS*—-SQUARE-ROOT CSLA (SQRT CSLA), COMMON BOOLEAN LOGIC (CBL), BINARY TO EXCESS-1 CONVERTER(BEC).**

I. INTRODUCTION.

In digital adders, the speed of addition is controlled by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is produced sequentially only after the previous bit position has been summed and a carry forwarded into the next position . In electronic applications adders are most widely used As we know millions of instructions per second are performed in microprocessors. So, speed of operation is the most important constraint to be considered while designing adder. Carry select Adder (CSLA) is one of the fastest adder used in many data processing processors to perform fast arithmetic operations. This paper present a simple and efficient gate-level modification to significantly reduce the area and power of the CSLA. Based on this modification 16-, 32-, and 64-b square-root CSLA (SQRT CSLA) architecture will be developed and compared with the regular and modified SQRT CSLA architecture. The basic idea of this work is to use Common Boolean Logic (CBL) instead of BEC with Cin=1 in the modified CSLA to achieve lower area and power consumption .This is one of the most substantial areas of research in VLSI system design.

The previous bit position has been summed and a carry propagated into the next position only when the sum for each bit position in an elementary adder is generated sequentially. The CSLA can be used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum . Whereas, the Regular CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry The ripple carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder

As a result Delay and Area of ripple carry adder is more. The solution of problem is instead of parallel RCA with Cin=1 is replaced with Bin**a**ry-Excess 1 converter(BEC).But after this modification, number of gate used in a design is more .Hence it requires large area. speed is also reduce due to this it provides more number of gate which result increase in delay. T.he main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure. The basic idea in this designing is to use Common Boolean Logic(CBL) instead of BEC with Cin=1 in the modified CSLA to achieve lower area and power consumption.

II. RELATED WORK

A simple approach is proposed by B. Ramkumar and Harish M Kittur to reduce the area and power of SQRT CSLA architecture. The reduced number of gates of this work offers the great advantage in the reduction of area and also the total power. The compared results show that the modified SQRT CSLA has a slightly larger delay (only 3.76%), but the area and power of the 64-b modified SQRT CSLA are significantly reduced by 17.4% and 15.4% respectively. The power-delay product and also the area-delay product of the proposed design show a decrease for 16-, 32-, and 64-b sizes which indicates the success of the method and not a mere tradeoff of delay for power and area. The modified CSLA architecture is therefore, low area, low power, simple and efficient for VLSI hardware implementation. [1]

HEMIMA.R, CHRISJIN GNANA SUJI.C proposed work uses a simple and efficient transistor level modification to significantly reduce the area and power of the CSLA. Based on this modification 4-bit CSLA architecture have been developed and compared with the regular CSLA architecture. In this proposed architecture RCA was designed using four bit 8T full adder. The multiplexer used in this block was designed with 2T.By reducing the number of transistors used the performance parameters, area and power reduces with slight increase in delay.[2]

Due to importance of adders in signal processing Authors Habib Ghasemizadeh Tamar, Akbar Ghasemizadeh Tamar designed a High Speed Area Reduced 64-bit Static Hybrid Carry-Lookahead/Carry-Select Adder. Combination of logic styles is an attractive approach for improvement of digital circuits. In this design we used combination of conventional CMOS (C-CMOS) and

transmission gate (TG) logic to decrease critical path delay of adder. So with small hardware this adder can operate in very high speed.[3]

Shivani Parmar, Kirat Pal Singh proposed the efficient modified Carry Select Adder (CSA) of 8-bit, 16-bit, 32-bit by using a single Ripple Carry Adder (RCA). The selection of ripple carry adder gives the specifications by accurate resource estimation. The high speed carry select adder performs binary addition pervasive in FPGA applications. Modified carry select adder shows performance and resource improvements as compared with conventional carry select adder. The frequency of conventional CSA is better than modified CSA. This paper proposes a scheme which reduces the delay, area and power than conventional CSA. The overall improvement in Modified SQRT CSLA shows better results in terms of area power and delay. Hence, proposed modified SQRT CSLA is being used for power and area efficient devices.[4]

To achieve more speed CSLA is replaces by SQRT CSLA. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum [5]-[6]. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry input Cin=0 and Cin=1, the final sum and carry are selected by the multiplexers(mux) [7]-[8] .Therefore in steadof Ripple Carry Adder Binary Excess-1 Converter(BEC) with sharing common Boolean Logic(CBL) concept is used.

III. PROPOSED WORK

The modified 16-bit SQRT CSLA using BEC is shown in Fig.1. The structure is again divided into five groups with different sizes of Ripple carry adder and BEC. The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed. The proposed 16-bit SQRT CSLA are shown in Fig.2. The parallel Ripple carry adder with Cin=1 with BEC. One input to the multiplexer goes from the RCA with Cin=0 and other input from BEC. Comparing the individual groups of both modified and proposed SQRT CSLA, it is clear that the BEC structure reduces delay. But the disadvantage of BEC method is that the area is increasing than the regular SQRT CSLA once the carry-in signal is ready, then select the correct carry-out output according to the logic state of carry-in signal.

This method replaces the BEC add one circuit by Common Boolean Logic. The proposed 16-bit SQRT CSLA architecture is shown in Fig.2. The summation and carry signal for full adder which has Cin=1, generate by INV and OR gate. Through the multiplexer, the correct output result is selected according to the logic state of carry-in signal. The internal structure of the group3 of proposed CSLA is shown in Fig.2.

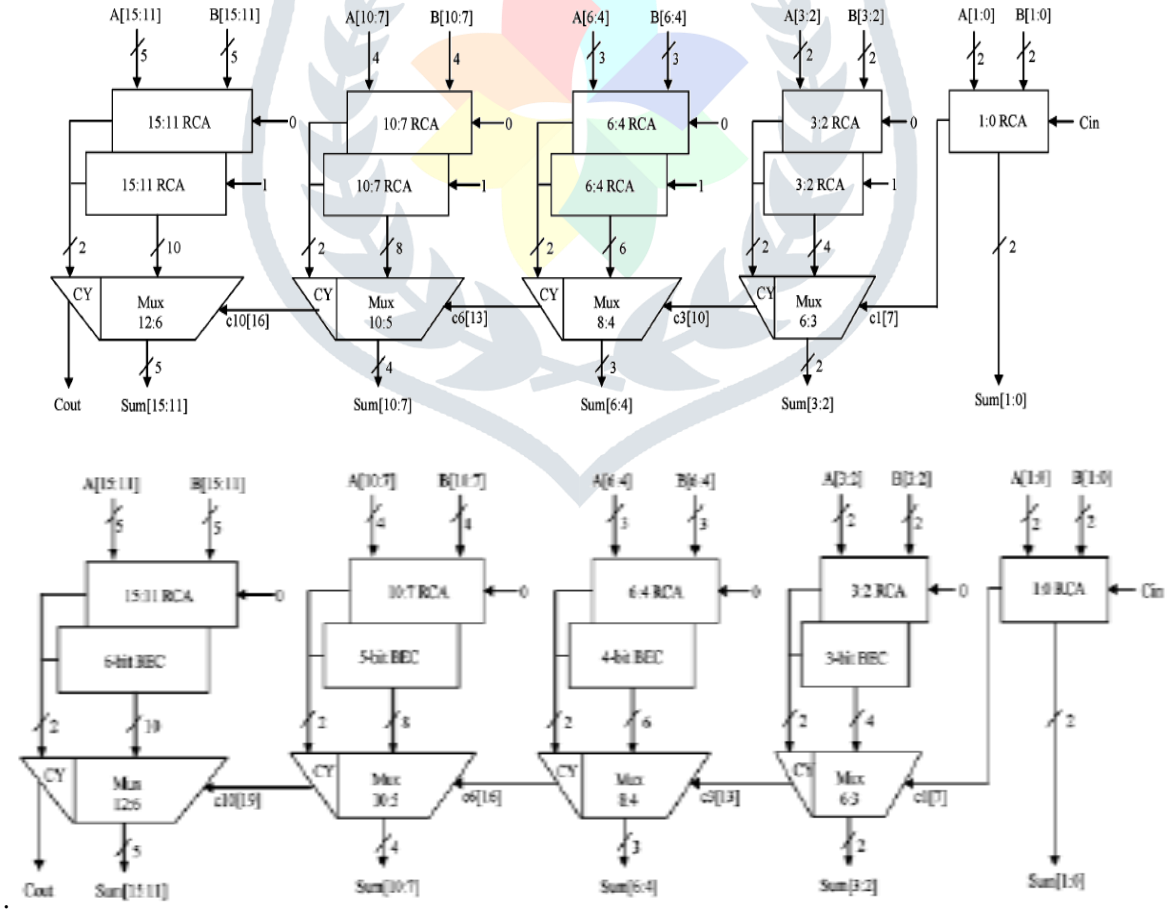

Fig.1 Regular and Modified 16 Bit SQRT CSLA

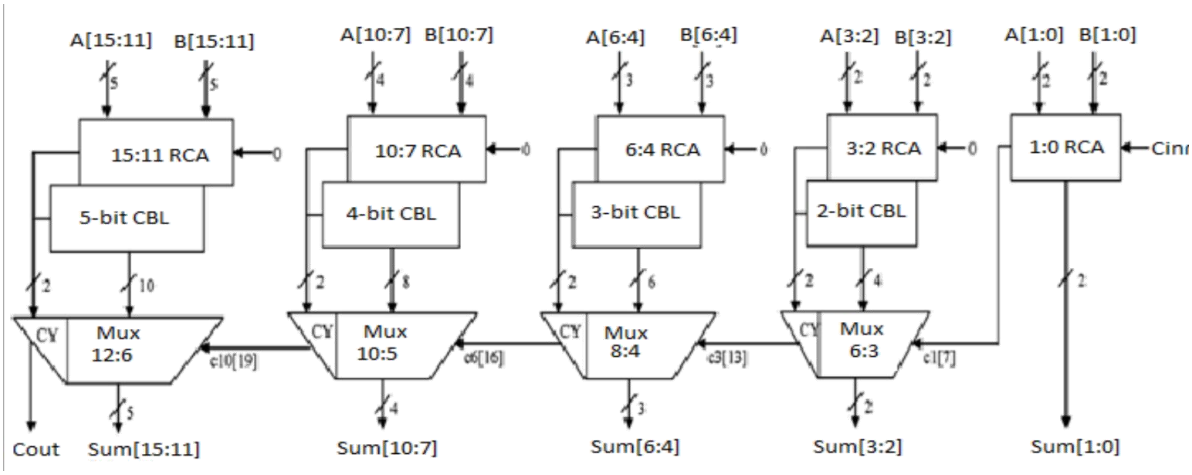

Fig.2 Proposed 16 Bit SQRT CSLA

IV. OBJECTIVES

The primary objectives of this study can be summarized as follows:

The 8-bit SQRT CSLA is done by the structure of 16-bit SQRT CSLA except group4 and group5. The 8-bit inputs are given to the full adder to complete the 8-bit sum and carry. The 32-bit SQRT CSLA is done by combining the two 16-bit SQRT CSLA. Simulation is carried out using Tanner simulation tool as the target device. The major disadvantage of modified architecture using BEC is increasing area. This disadvantage is overcome by using Common Boolean Logic which is shown in Fig.3 term in the proposed architecture which reduces area than the regular and modified Square-root Carry select adder in proposed archtectures.

The proposed work is planned to be carried out in the following manner,in this paper, an area efficient square-root carry select adder is proposed by sharing the common Boolean logic (CBL) term, the duplicated adder cells in the conventional carry select adder is removed this architecture will be designed by Taneer EDA 13.1 simulatiuon. This work offers the great advantage in the reduction of area. The regular SQRT CSLA has the disadvantage of occupying more chip area. This paper proposes a scheme which reduces the area as well as power in SQRT CSLA. It would be interesting to test the design of the 32 and 64 bit SQRT CSLA using this CBL concept shown in Fig.3.

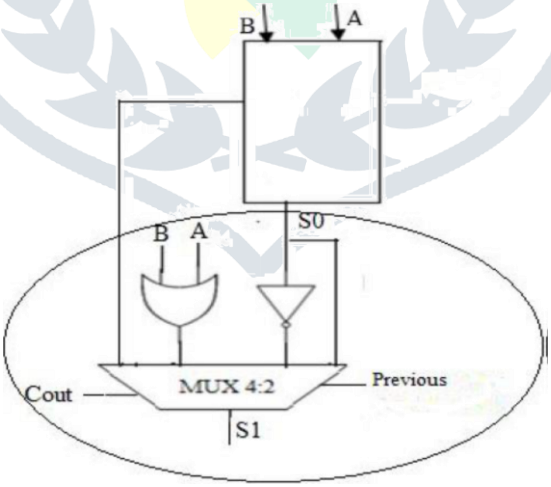

Fig.3 Single Bit CBL Full Adder

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V. ADVANTAGES

From all the reference paper, most recent methods for the carry select adder are discussed. The proposed work is planned to be carried out in the following manner. The reduced number of gates of this work offers the great advantage in the reduction of area as well as power The regular SQRT CSLA has the disadvantage of occupying more chip area. This paper proposes a scheme which

reduces the area than the regular and modified SQRT CSLA. It would be interesting to test the design of the 32 and 64 bit SQRT CSLA.The reduced number of gates of this work offers the great advantage in the reduction of area by using CBL concept.

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