

Memory Efficient Scalable Video Encoder Architecture

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Abstract— Memory efficient scalable video encoder architecture is proposed in this aspect that the quality of the video to be good even though it is scaled down. Apart from that also see that the memory utilized by it to be as less as possible. Here a low complexity and memory efficient architecture is being used for scalable video encoder. The proposed very-large-scale integration architecture of the scalable video encoder is implemented on Field Programmable Gate Array (FPGA). The hardware synthesized using Xilinx ISE (Integrated Software Environment). In this architecture a lossless compression, quality driven bit plane sequencer, size scalability and SNR scalability is done.

Index terms — Lossless compression; discrete wavelet transform; size scalability; SNR scalability; image compression;

I. INTRODUCTION

Nowadays wireless digital home environment is a trend to remove the unnecessary wires between different entertainment devices, such as the DVD player, television, computers, mobile devices. The traditional approaches, including the Wireless HD [1] and WHDI [2], did not consider the transmission issue with multiple devices at the same time. Thus, a multiple source scalable video encoder with high definition real-time video processing capability is required and the hardware realization of the encoder is needed.

H.264/AVC is the new video coding standard. It can save 25%-45% and 50%-70% of bitrates when compared with MPEG-4 Advanced Simple Profile (ASP) and MPEG-2, respectively. Although motion compensated transform coding is still adopted, many new features are used to achieve much better compression performance and subjective quality, such as quarter-pixel Motion Estimation (ME) with Multiple Reference Frames (MRF) and Variable Block Sizes (VBS), intra prediction, Context-based Adaptive Variable Length Coding (CAVLC), and in-loop de-blocking filter. The rate distortion optimized mode decision is also included in reference software to improve rate-distortion efficiency. There are many potential applications of H.264/AVC. Ongoing applications range from High Definition Digital Video Disc (HD-DVD) or BluRay for living room entertainment with large screens to Digital Video Broadcasting for Handheld terminals (DVB-H) with small screens. However, the H.264/AVC coding performance comes at the price of computation complexity. According to the instruction profiling with HDTV1024P (2048×1024, 30fps) specification, H.264/AVC decoding process requires 83 Giga-Instructions Per Second (GIPS) computation and 70 Giga-Bytes Per Second (GBPS) memory access. As for H.264/AVC encoder, up to 3600 GIPS and 5570 GBPS are required for HDTV720P (1280×720, 30fps) specification. For real-time applications, accelerating by the dedicated hardware is a must. However, it is difficult to design an system architecture for the H.264/AVC codec. The design for the significant modules are also very challenging.

Besides high computation complexity and memory access, the coding path is very long, which includes prediction, reconstruction, and entropy coding. The reference software adopts many sequential processing of each block in the Macro Block (MB), which restricts the parallel processing. The block-level reconstruction loop caused by intra prediction induces the bubble cycles and decreases the hardware utilization and throughput. The coding tools involve with many data dependencies to enhance the coding performance, but the considerable storage space is the penalty. There are functionalities that have multiplex modes, and the re-configurable engine is essential to achieve resource sharing.

A well-known scalable video codec is provided by AVC (MPEG-4) video coding standard. The intent of the H.264/AVC project was to create a standard capable of providing good video quality at substantially lower bit rates than previous standards (i.e., half or less the bit rate of MPEG-2, H.263, or MPEG-4 Part 2), without increasing the complexity of design so much that it would be impractical or excessively expensive to implement. An additional goal was to provide enough flexibility to allow the standard to be applied to a wide variety of applications on a wide variety of networks and systems, including low and high bit rates, low and high resolution video, broadcast, DVD storage, RTP/IP packet networks, and ITU-T multimedia telephony systems.

The H.264 standard can be viewed as a "family of standards". A specific decoder decodes at least one, but not necessarily all profiles. The decoder specification describes which profiles can be decoded. The H.264 name follows the ITU-T naming convention, where the standard is a member of the H.26x line of VCEG video coding standards; the MPEG-4 AVC name relates to the naming convention in ISO/IEC MPEG, where the standard is part 10 of ISO/IEC 14496, which is the suite of standards known as MPEG-4. However it involves high complexity on computation and implementation.

We have proposed a low complexity scalable video encoder, named as size and SNR scalable image-video compression codec (SS-SIVC), for wireless high definition video interface. In our scalable video encoder, three main modules are included: discrete wavelet transform (DWT), the bit plane sequencer and the fast adaptive binary arithmetic coding (M-Coder). For discrete wavelet transform (DWT), there are several architectures, including [3]- [6]. In this, a memory-efficient pipelined architecture with parallel scanning method is used for 2-D lifting-based DWT in scalable video encoder applications. For the bit plane sequencer, we

consider the improvement on the run-time performance and avoid the computational complexities. Comparing the arithmetic coder on AVC video coding standard, CABAC (Context-based Adaptive Binary Arithmetic Coder) is adopted as one of the most efficient entropy coders. CABAC realizes high compression efficiency close to theoretical limit by utilizing context-adaptive probability estimation of binary symbol (bin). During adaptive binary arithmetic coder (M-coder), CABAC adopts 398 contexts, while proposed bit plane sequencer reduces original 398 contexts to only 3 contexts. Accordingly, a low-complexity pipelined fast adaptive binary arithmetic coding (M-Coder) is proposed. In this , the architecture and VLSI design of scalable video encoder is proposed. The design is based on a new lossless compression codec with size and SNR scalable image-video compression codec.

II. RELATED WORKS

[1] A high performance and memory-efficient pipelined architecture with parallel scanning method for 2-D lifting-based DWT in JPEG2000 applications. The Proposed 2-D DWT architecture are composed of two 1-D DWT cores and a 2×2 transposing register array. The proposed 1-D DWT core consumes two input data and produces two output coefficients per cycle, and its critical path takes one multiplier delay only. Moreover, we utilize the parallel scanning method to reduce the internal buffer size instead of the line-based scanning method. For the $N \times N$ tile image with one-level 2-D DWT decomposition, only $4N$ temporal memory and the 2×2 register array are required for $9/7$ filter to store the intermediate coefficients in the column 1-D DWT core. And the column-processed data can be rearranged in the transposing array. According to the comparison results, the hardware cost of the 1-D DWT core and the internal memory requirements of proposed 2-D DWT architecture are smaller than other familiar architectures based on the same throughput rate. The implementation results show that the proposed 2-D DWT architecture can process 1080p HDTV pictures with five-level decomposition at 30 frames/sec.

[2] Context-Based Adaptive Binary Arithmetic Coding (CABAC) is a normative part of the new ITU-T/ISO/IEC standard AVC/AVC for video compression. By combining an adaptive binary arithmetic coding technique with context modeling, a high degree of adaptation and redundancy reduction is achieved. The CABAC framework also includes a novel low-complexity method for binary arithmetic coding and probability estimation that is well suited for efficient hardware and software implementations. CABAC significantly outperforms the baseline entropy coding method of AVC/AVC for the typical area of envisaged target applications. For a set of test sequences representing typical material used in broadcast applications and for a range of acceptable video quality of about 30 to 38 dB, average bit-rate savings of 9%–14% are achieved.

[3] Design of Architecture and FPGA Implementation of a Video Encoder proposes a novel VLSI architecture for Video Encoder, which processes high resolution video sequences at real time rates. The architecture has been realized using Verilog and implemented on an Xilinx XUPVP30 FPGA. The gate count of the implementation is approximately 800,000 including an output FIFO of size 128 K bits. It can process 1600×1200 pixels color motion pictures in 4:2:0 format at 30 frames per second as per MPEG-2 standard. The compression effected is typically 20 to 40 and the reconstructed picture is of good quality with a PSNR values of 32 db or more. The main advantage of the architecture proposed is that it improves the throughput by over 30% compared to the earlier Encoder developed by one of the present authors. The proposed architecture of Video Encoder consists of Discrete Cosine Transform and Quantization Processor, Run Length Encoder, Variable Length Coder, Header Generator, Serializer, FIFOs and a Master Controller that co-ordinates all the activities of the encoder. The Video Encoder has also been coded in Matlab in order to validate the Verilog realization. The drawback was that it used FIFO and needed a serializer.

[4] Hardware Architecture Design of an H.264/AVC Video Codec. H.264/AVC is the latest video coding standard. It significantly outperforms the previous video coding standards, but the extraordinary huge computation complexity and memory access requirement make the hardwired codec solution a tough job. This paper describes the design methodology for H.264/AVC video codec. The system architecture and scheduling will be addressed. The design consideration and optimization for its significant modules including bandwidth optimized motion compensation engine, reconfigurable intra predictor generator, low bandwidth parallel integer motion estimation will be mentioned. Due to the complex, sequential, and highly data-depended characteristics of all essential algorithms in H.264/AVC, not only the pipeline structure but also efficient memory hierarchy is required. The design case with a hybrid task pipelining scheme, a balanced schedule with block-level, MB-level, and frame-level pipelining, will be presented. By combining with many bandwidth reduction techniques and data reused schemes, very efficient architecture and implementation for plate-form based system is proved by the prototype chips. A hybrid task pipelining scheme, a balanced schedule with block-level, MB-level, and frame-level pipelining, is used for decoder to greatly reduce the internal memory size. Combined with many bandwidth reduction techniques and DR schemes, these two system architectures are all characterized by high throughput and low system bandwidth requirement. Moreover, efficient modules are designed to support the new H.264/AVC functionalities. A parallel IME architecture comprising eight PE arrays and adder trees is applied to dramatically reduce the memory bandwidth by three-level memory hierarchy and DR scheme. A reconfigurable intra predictor generator was designed to achieve resource sharing for all intra prediction modes. A bandwidth optimized MC engine highly exploits DR between interpolation windows of neighboring blocks.

[5] Distributed Video Coding (DVC) is a new coding paradigm for video compression, based on Slepian- Wolf (lossless coding) and Wyner-Ziv (lossy coding) information theoretic results. DVC is useful for emerging applications such as wireless video cameras, wireless low-power surveillance networks and disposable video cameras for medical applications etc. The primary objective of DVC is low-complexity video encoding, where bulk of computation is shifted to the decoder, as opposed to low-complexity decoder in conventional video compression standards such as H.264 and MPEG etc. Primarily there are two types of DVC techniques namely

pixel domain and transform domain based. Transform domain design will have better rate-distortion (RD) performance as it exploits spatial correlation between neighbouring samples and compacts the block energy into as few transform coefficients as possible (aka energy compaction). It has been proven that DVC resulted in better RD performance than that of H.264 intra for low to medium motion activity sequences. For high motion sequences, the RD performance of DVC and H.264 intra are comparable. Whereas, DVC RD performance of very high motion sequences are lower than that of H.264 intra. Drawbacks were: Need of Feedback channel from decoder to encoder, lack of procedure for chroma components coding, lack of compressed video transport bit-stream definition, inconsistencies in RD performance compared to H.264 intra with different video Streams, No standardization, flicker.

[6] Low cost architecture for JPEG2000 encoder without code block memory tries to unify the output scanning order of the 2D-DWT and the processing order of the EBCOT and further to eliminate the code-block memory completely eliminated. A new architecture for embedded block coding (EBC), code-block switch adaptive embedded block coding (CS-AEBC), which can skip the insignificant bit-planes to reduce the computation time and save power consumption. Besides, a new dynamic rate distortion optimization (RDO) approach is proposed to reduce the computation time when the EBC processes lossy compression operation. The total memory required for the proposed JPEG2000 is only 2KB of internal memory, and the bandwidth required for the external memory is 2.1 B/cycle.

[7] VLSI architecture of line-based lifting wavelet transform for motion JPEG2000 is a architecture of lifting processor for JPEG2000 and implemented it with both FPGA and ASIC. It includes a new cell structure that executes a unit of lifting calculation to satisfy the requirements of the lifting process of a repetitive arithmetic. After analyzing the operational sequence of lifting arithmetic in detail and imposing the causality to implement in hardware, the unit cell was optimized. A new simple lifting kernel was organized by repeatedly arranging the unit cells and a lifting processor was realized for Motion JPEG2000 with the kernel. The proposed processor can handle any size of tiles and support both lossy and lossless operation with (9,7) filter and (5,3) filter, respectively. Also, it has the same throughput rate as the input, and can continuously output the wavelet coefficients of the four types (LL, LH, HL, HH) simultaneously. The lifting processor was implemented in a 0.35 μm CMOS fabrication process. The operation speeds of the ASIC and FPGA were 150 MHz and 115 MHz, which correspond to the data rates of 1.2 Gb/s (219 frames/s) and 0.92 Gb/s (166 frames/s), respectively. These speeds are more than enough for real-time process even for high-definition images. The result from comparing to the existing architectures showed that the proposed uses less hardware resources and simple complexity in compensation to the larger memory requirement and also stably operated.

III PROPOSED METHODOLOGY

We propose the architecture for the SS-SIVC encoder. Fig.1 shows the block diagram. It contains a 3-level DWT module, three two pass quality driven bit-plane sequencer based on M-coder modules (BPS), and a bitstream buffer (BSB).

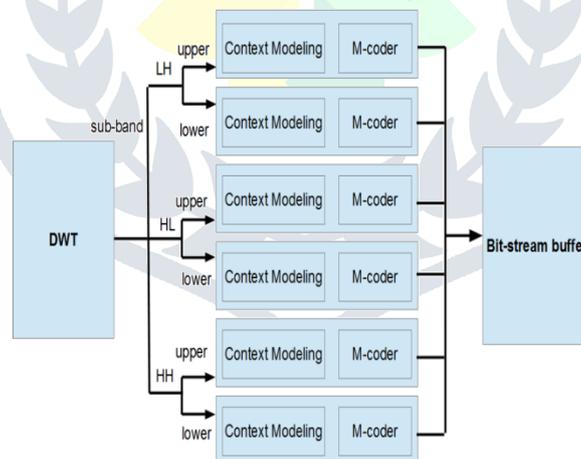


Fig. 1Block diagram of the SS-SIVC codec system.

The block diagram of the proposed lifting based 2-D DWT architecture Fig. 2. We present a high speed and memory-efficient pipelined architecture with parallel scanning method for 2-D lifting-based DWT in SS-SIVC applications. The proposed architecture contains two 1-D processors, a temporal buffer, and a transposing buffer. The LL Memory stores the LL-band coefficients of lower levels for the decomposition of higher level. To reduce the critical path of the 1-D processor, the proposed 1-D processors have one multiplier delay via the proposed 5/3 filter lifting scheme. According to the 5/3 lifting-based equation, the equation is applied in designing the 1-D DWT processing unit for our design. Based on the signal processing design methodology, the detailed data flow graph (DFG) of the proposed two-inputs/two-outputs 1-D processing element as illustrated. Two input samples are fetched each cycle, and then each input is multiplied by the corresponding coefficient next cycle. After each input data is multiplied, it only requires several addition operations for the rest of the calculation. According to the structure of DFG, corresponding hardware architecture is presented. The transpose buffer is designed with the consideration on the scan order. According to the 2-input/2-output characteristics, the parallel scan is adopted by combining the line scan methodology and two-output characteristic, as illustrated. Based on the scan order, only four registers are required for the transpose buffer, resulting in the optimal condition for transpose buffer design.

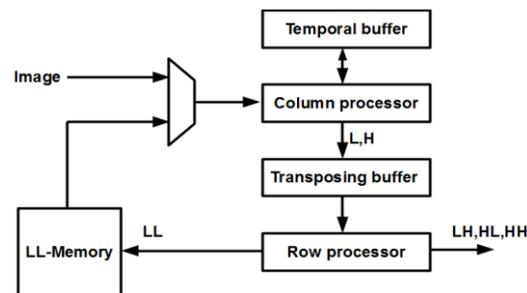


Fig.2 Block diagram of the proposed 2-D DWT architecture.

IV RESULTS

Initially the image is taken as input and DWT is performed on it. The result is as shown in the below figures



Fig 3.Original image

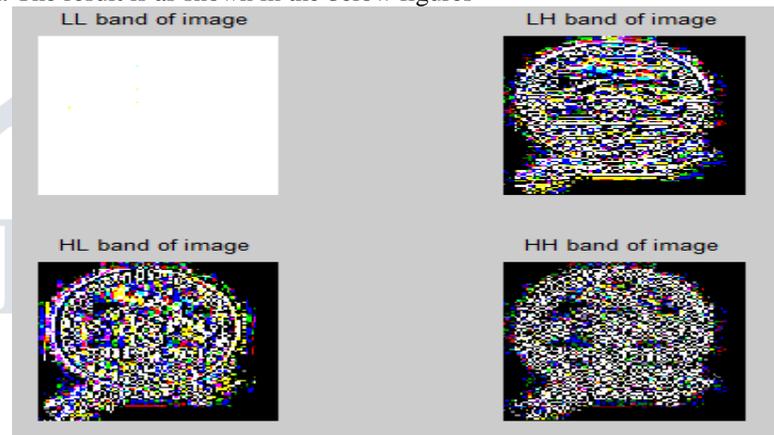


Fig 4. Sub bands LL,LH, HL &HH after applying DWT

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