Dual-V_{DD}, Single-Frequency Clocking Methodology for System on Chip

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***Abstract*—** Clock distribution networks synchronize the flow of data signals among synchronous data paths. The design of these networks can dramatically affect system-wide performance and reliability. A theoretical background of clock skew is provided in order to better understand how clock distribution networks interact with data paths. Minimum and maximum timing constraints are developed from the relative timing between the localized clock skew and the data paths.

Two new clocking methodologies based on supply voltage and frequency scaling are proposed for lowering the power consumption and the temperature-fluctuation-induced skew without degrading the clock frequency. The clock signal is distributed globally at a scaled supply voltage with a single clock frequency with the first clocking methodology. Alternatively, dual supply voltages and dual signal frequencies are employed with the second methodology that provides enhanced power savings. Novel multi-threshold voltage level converters and frequency multipliers are employed at the leaves of the clock trees in order to maintain the synchronous system performance. The temperature-fluctuation-induced skew and the power consumption are reduced by up to 80% and 76%, respectively, with the proposed dual supply voltage and dual frequency clock distribution networks as compared to a standard clock tree operating at the nominal supply voltage with a single clock frequency [1].

In this paper, design of a Dual-Vdd and Single Clocking methodology is analyzed with respect its operation then building and testing using Cadence Tools. In realization, first discuss the architecture and the implementation issues. Then, the coding process is simulated and verified by Cadence Tools.

Tools used: Cadence Tools (Virtuoso, ADEL, Spectre Simulator, Assura

***Index Terms*—Clock distribution networks, clock skew, De-skew buffers, H-trees, wireless clock distribution.**

I. INTRODUCTION

Clock signals are important in synchronous circuits to synchronize different data signals arriving from different parts of the integrated circuit, such that the correct data is available for computation. Due to impedances present in interconnects there are mismatches in the clock arrival time due to spatial distances between two clocks.

These mismatches in time are known as clock skews. Due noises caused by other interconnect lines running in parallel with the clock signals, clock signals arriving at two different registers with the same clock input experience a phase noise, commonly known as clock jitter [1].

Clock distribution networks ensure that these constraints regarding clock skew and jitters are minimized. Design of clock distribution network is however a cumbersome task and a designer must decide the clock distribution before the circuit is designed because the difficulty in designing an efficient clock distribution network increases in the latter stages of design [1].

Different techniques such as H-tree, buffered clock trees and meshed clock network are used in the design of the clock networks. Since the interconnects do not scale proportionally to the rapidly scaling transistor feature sizes that operate at high clock frequencies, sets a difficulty in designing an efficient clock distribution networks.

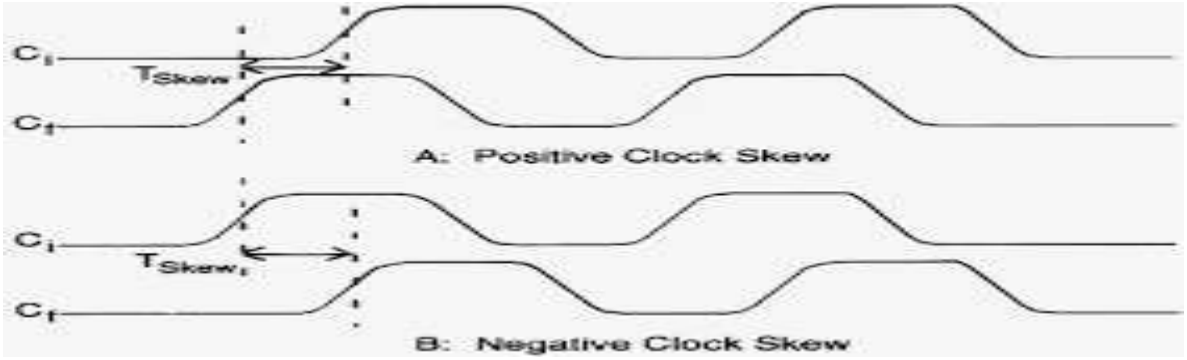

Fig.1. Positive & Negative Skew

II. CLOCK DISTRIBUTION NETWORKS

The Design methodology and structural topology of the clock distribution network should be considered in the development of a system for distributing the clock signals.The system speed,Physical die area,and power dissipation are greatly affected by the clock distribution network.

Requirements:-

1.clock waveforms must be particularly clean and sharp
2.No Skew.

Methodologies:-

Clock distribution strategies:- The relative phase between two clcoking element is important
Achieve zero skew routing:- Route clock to destinations such that cloc k edges appear at the same toime.

H-TREE:-

The primary goal in clock distribution design has traditionally been to transmit the clock signal to every register in the system at precisely the same time. Many routing algorithms exist for attaining zero clock skew, some more effective than others. In all cases, routing for zero clock skew results in a larger clock distribution network. The necessity to match delays forces increased route lengths, and often increases complexity.

A common zero skew routing strategy is the symmetric H-tree clock distribution network. This method aims to produce zero skew clock routing by matching the length of every path from clock source to register load. This is accomplished by creating a series of H-shaped routes from the center of the chip as illustrated by Fig.2. At the corners of each "H" the nearly identical clock signals provide the inputs to the next level of smaller "H" routes. At each junction the impedance of the interconnect is scaled to minimize reflections.

For an H-tree network, each conductor leaving a junction must have twice the impedance of the source conductor. This is accomplished by decreasing the interconnect width of each successive level.

This continues until the final points of the H-tree structure are used to drive either the register loads, or local buffers which drive the register loads. Thus, the path length from the clock source to each register is practically identical in an H-tree distribution. A variant of H-tree is X-tree clock distribution network illustrated in Fig.

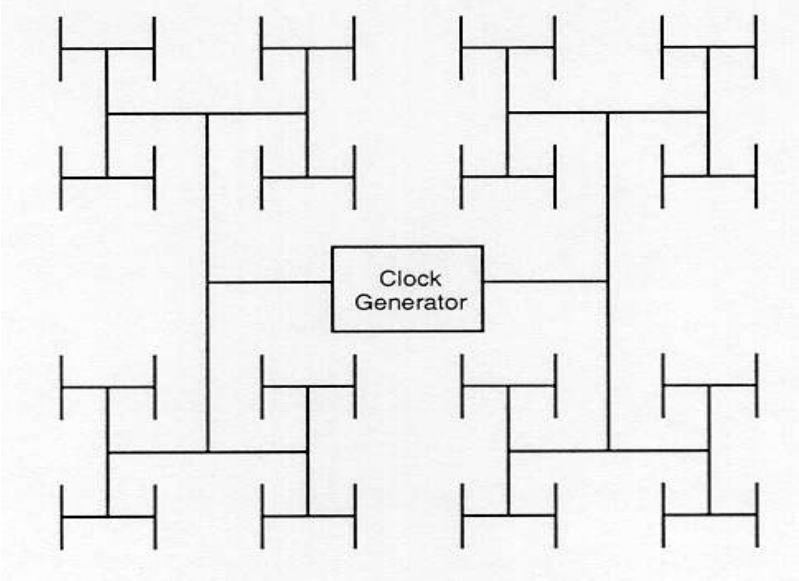

Fig.2 H-tree Clock distribution network

The major component of the total power dissipation is the power that is used to charge and discharge the load capacitance in the circuits.

$$P = \square CLVddVs$$

where f is the clock frequency, C_L is the load capacitance, Vdd the supply voltage, and Vs the output swing of the buffer. For the case where the output of the buffer swings from 0 to Vdd, Vs = Vdd and the formula reduces to

$$P = f\,CL\,Vdd^2.$$

Since f is a fundamental parameter for the circuit, it cannot be changed and its effects can only be reduced by techniques such as clock gating..

Therefore, the power dissipation of the clock network can only be reduced by
(a) reducing the total load capacitance, which is consistent with attempting to achieve the minimal wire length and the minimal buffer power dissipation; techniques for minimal wire length .
(b) reducing Vdd, which creates a quadratic reduction if Vs is also simultaneous reduced by the same factor (for example, when Vdd = k Vs for some value of k)
(c) reducing Vs without reducing Vdd, which corresponds to a linear reduction in the power dissipation.

I. LEVEL CONVERTER CIRCUITS

The structure of the HLconverter is relatively straightforward. To convert the clock swing from a higher voltage range of gnd to VddH to a lower voltage range of gnd to VddL, a conventional buffer driven by a supply voltage of VddL will be adequate.

We note that the use of feedback in the part driven by VddH serves to speed up the transition and therefore ensures that the transient current is not significant;
our simulations show that it is, in fact, less than the transient current for a single inverter driven by VddH.

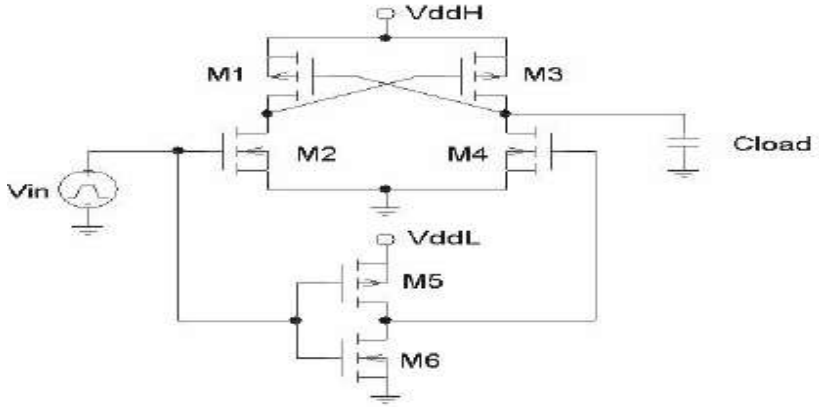

Fig.3 LH Converter Circuit.

II .MULTI –V_{TH} LEVEL CONVERTER

For a dual-Vdd FPGA fabric, the interface between a VddL device and a VddH device must be designed carefully to avoid the excessive leakage power. If a VddL device drives a VddH device and the VddL device output is logic '1', both PMOS and NMOS transistors in the VddH device will be at least partially "on", dissipating unacceptable amount of leakage power due to short circuit current.

A level converter should be inserted to block the short circuit current. The level converter converts VddL signal swing to VddH signal swing 1.

Different level converter circuits have been used in dual-Vdd ASIC designs. These level converters use both VddH and VddL as its supply voltages and create extra constraints for power/ground routing. As shown in Figure, when the input signal is logic '1', the threshold voltage drop across NMOS transistor 'n1' can provide a virtual low supply voltage to the first-stage inverter (p2,n2) so that p2 and n2 will not be partially "on". When the input signal is logic '0', the feedback path from node 'OUT' to PMOS transistor 'p1' pulls up the virtual supply voltage to VddH and inverter (p2,n2) generates a VddH signal to the second inverter so that no DC short circuit current exists.

For a particular VddH/VddL combination, we decide the transistor size in the level converter as follows. We start from a level converter with minimum transistor sizes. We size up the transistors to limit the level converter delay within 30% of a single LUT delay or 7% of a logic cluster delay.

For transistor sizes that meet the delay bound, we choose the sizing with the lowest power consumption. This is because the threshold voltage drop cannot provide a proper virtual low-supply as the gap between VddH and VddL is large. Therefore, the VddH/VddL ratio cannot be too large considering the leakage overhead of level converters.

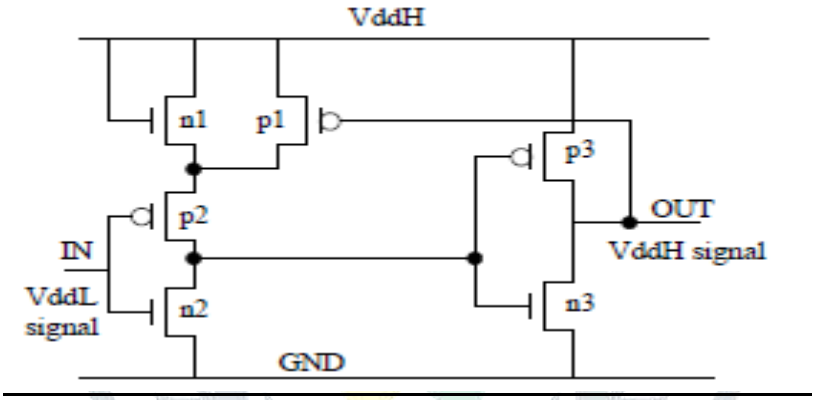

Fig.4 LH Converter using Multi Vth

IV. SIMULATION RESULTS AND CONCLUSION

H-tree Version of Clock Distribution Network

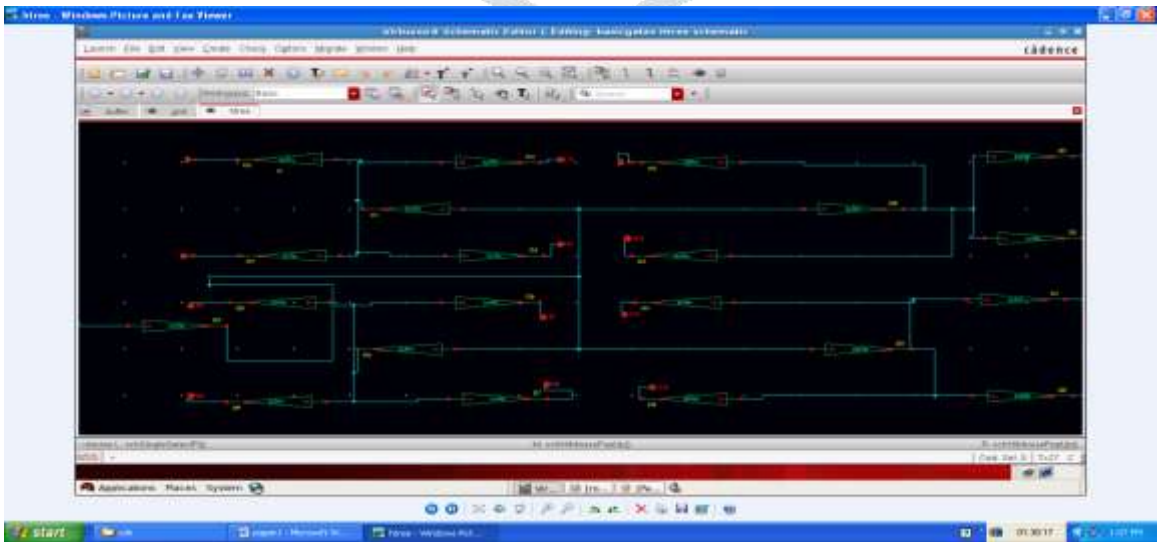

Fig. 5 H-tree Version of CDN

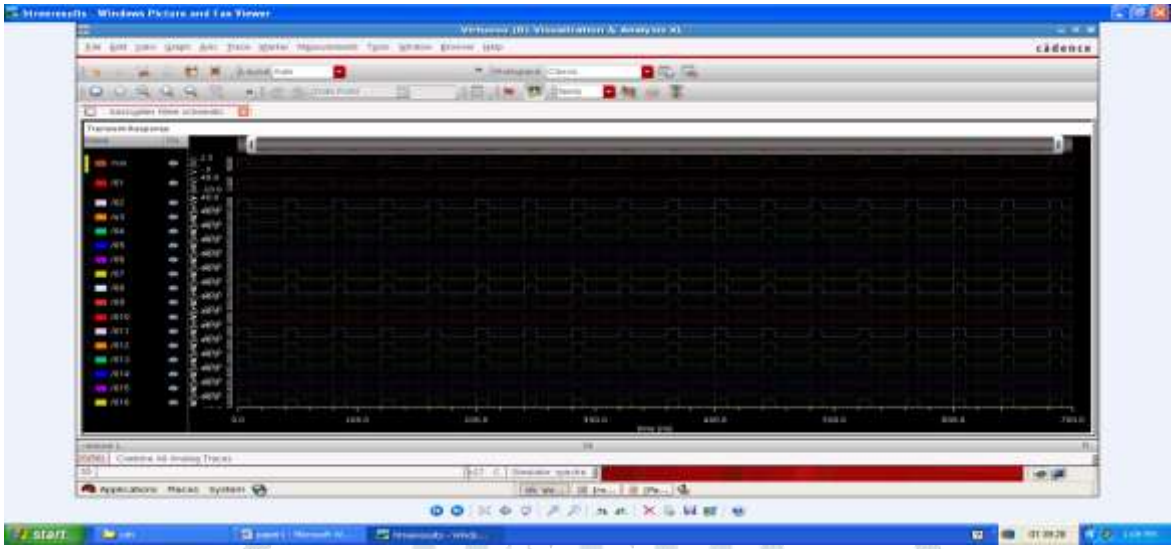

Fig. 6 Simulation Results of H-tree Version of CDN

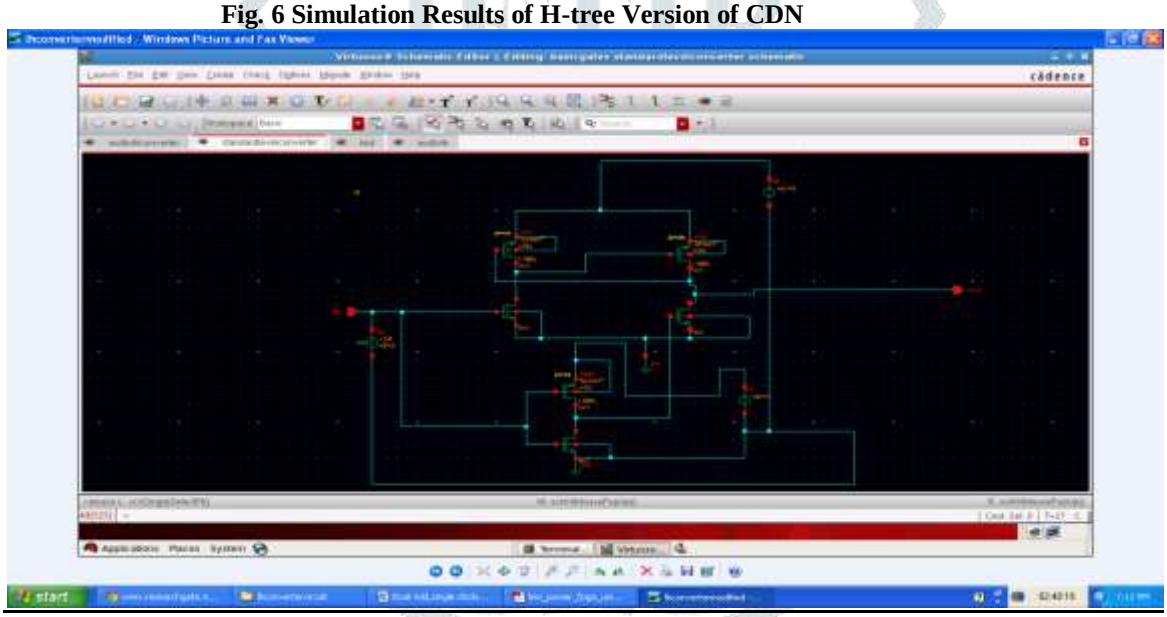

Fig.7 LH Converter

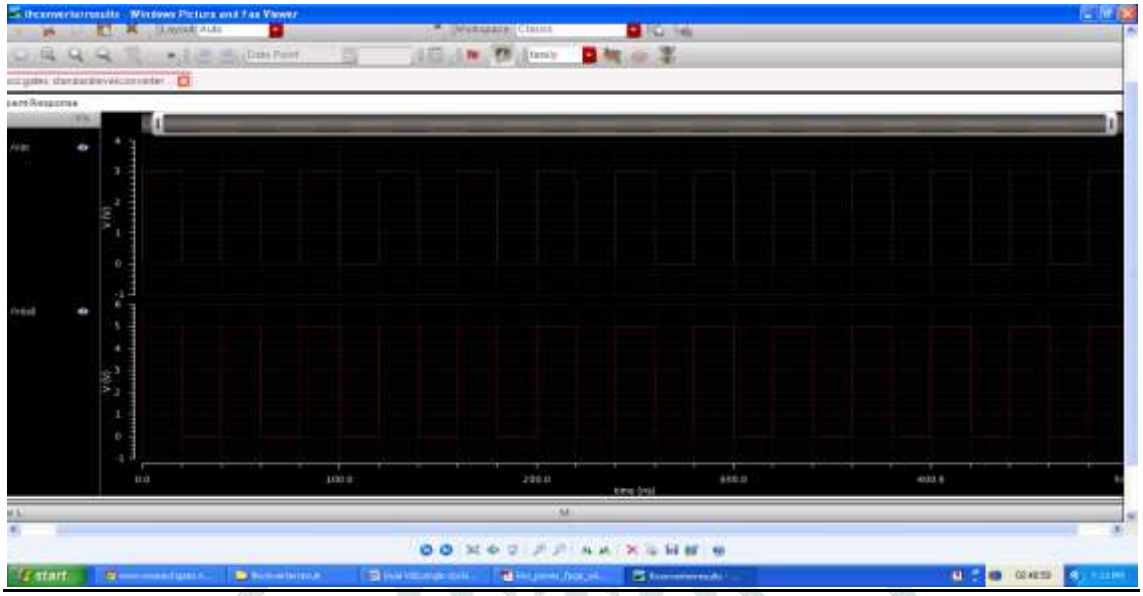

Fig.7 Simulation results of LH Converter

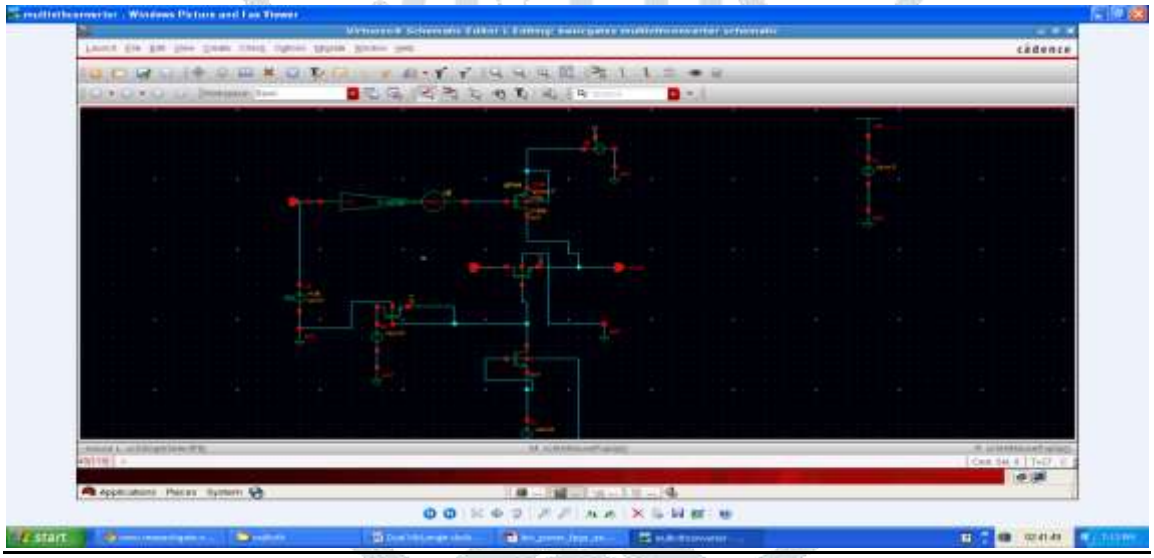

Fig.8 Multi-Vth Converter Circuit

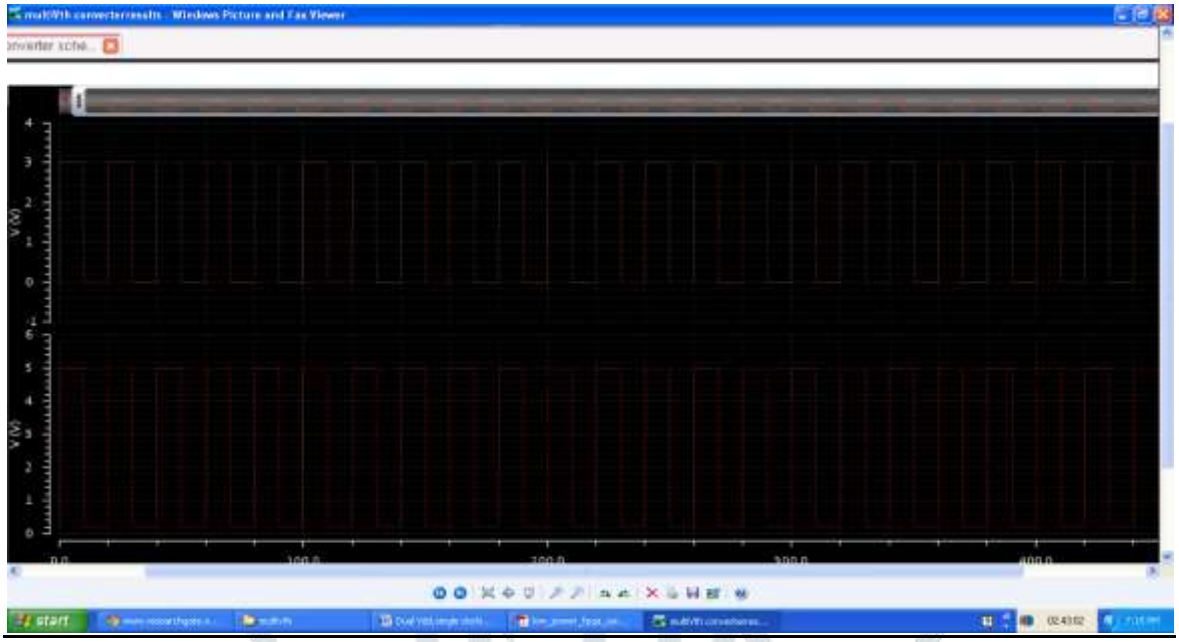

Fig.9.Simulation Results of Multi-Vth Converter Circuit

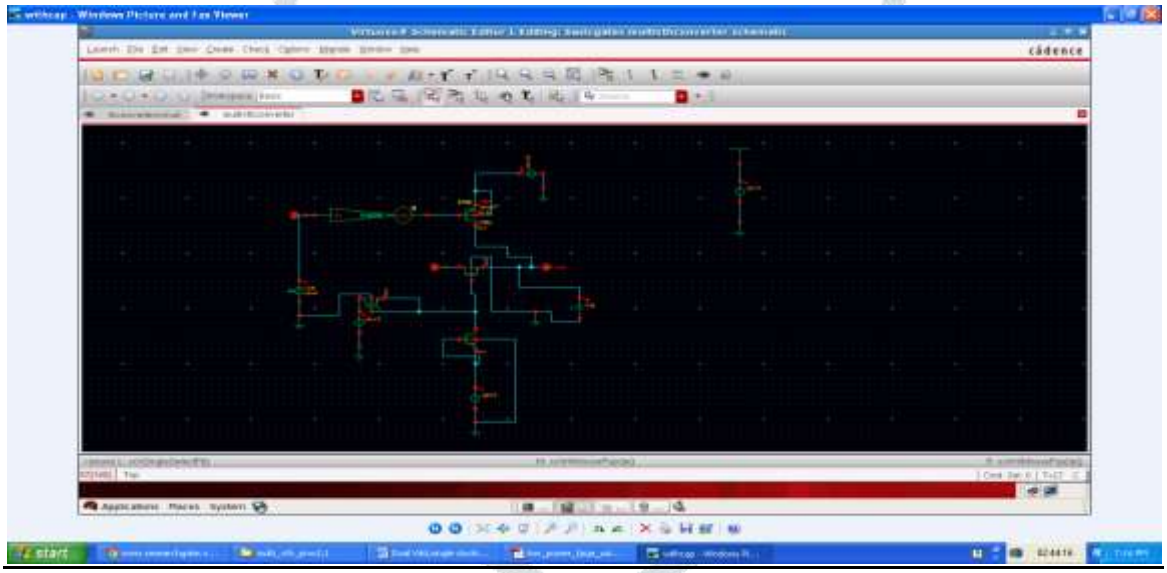

Fig.10 Multi-Vth Converter Circuit with C_{Load}

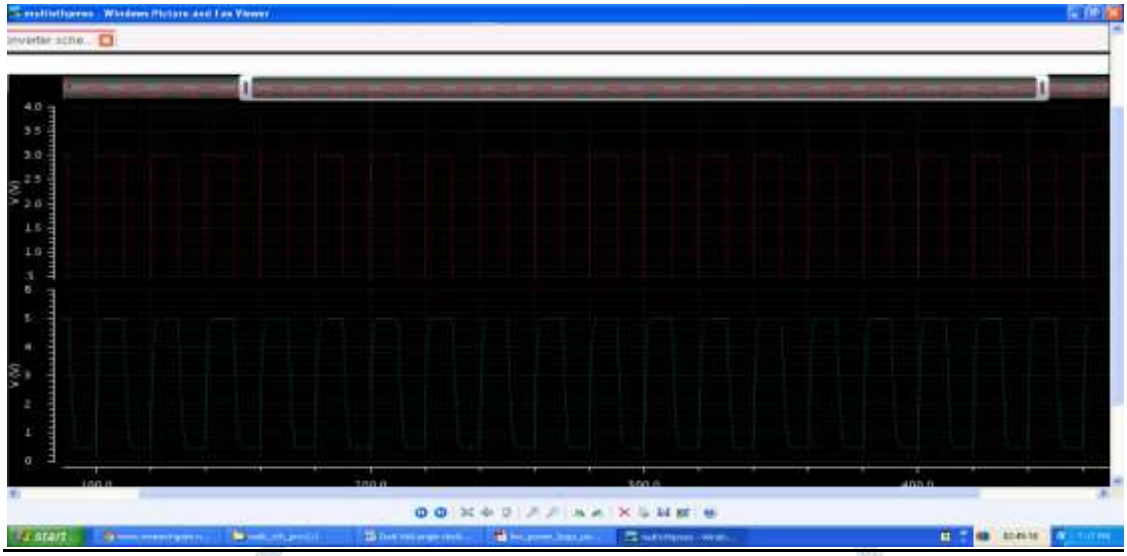

Fig.9.Simulation Results of Multi-Vth Converter Circuit Using C_{load}

IV. RESULTS & CONCLUSION

In this paper, I investigated the performances and com-plexities of the Various Clock Distribution networks regarding effect of interconnect resistance and load capacitance when driving long signal lines. The Clock skew and clock jitter can be minimized by selection of proper clock distribution network and the parameters affecting it.

Various circuit-based design methodologies and techniques for distributing the clock signals have been suggested and practical circuit applications have been reviewed.

It is often noted that the design of the clock distribution network represents the fundamental circuit-based performance limitation in high-speed synchronous digital systems. In this paper, dual –Vdd(VDDL=3v) ,(VDDH=5V) single Frequency Clock distribution Level Converters are designed using Cadence Tools. The delay associated with the sgnal propagation was 10.9ns which makes us to utilize the clock frequency of more than 100 Mhz. Thus Proper designs of clock distribution networks and Level converters help in reduce power dissipation of systems and on chip circuits. The local data path-dependent nature of clock skew, rather than any global characteristics, requires extreme care in the design, analysis, and evaluation of high-speed clock distribution networks.

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