SIMULATION OF MULTI CONVERTER BASED UNIFIED POWER-QUALITY (MC-UPQC) CONDITIONING SYSTEM ON VOLTAGE STABILITY OF RADIAL DISTRIBUTION SYSTEMS

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Abstract: This paper presents a new unified power-quality conditioning system (MC-UPQC), capable of simultaneous compensation for voltage and current in multi-bus/multi-feeder systems. In this configuration, one shunt voltage-source converter (shunt VSC) and two or more series VSCs exist. The system can be applied to adjacent feeders to compensate for supply-voltage and load current imperfections on the main feeder and full compensation of supply voltage imperfections on the other feeders. In the proposed configuration, all converters are connected back to back on the dc side and share a common dc-link capacitor. Therefore, power can be transferred from one feeder to adjacent feeders to compensate for sag/swell and interruption. The proposed topology can be used for simultaneous compensation of voltage and current imperfections in both feeders by sharing power compensation capabilities between two adjacent feeders which are not connected. The system is also capable of compensating for interruptions without the need for a battery storage system and consequently without storage capacity limitations. The performance of the MC-UPQC as well as the adopted control algorithm is illustrated by simulation. The simulation results show that a significant amount of power-loss reduction, under voltage mitigation, and the enhancement of voltage stability margin can be obtained with an appropriate placement of the MC-UPQC in a distribution network. The performance of MC-UPQC by taking proposed 3-phase converter as our extinction reported design approach shows that it is more efficient in under voltage mitigation.

Index Terms—Power quality, mc-upqc, voltage stability, vsc.

I. INTRODUCTION:

With increasing applications of nonlinear and electronically switched devices in distribution systems and industries, power-quality (PQ) problems, such as harmonics, flicker, and imbalance have become serious concerns. In addition, lightning strikes on transmission lines, switching of capacitor banks, and various network faults can also cause PQ problems, such as transients, voltage sag/swell, and interruption. On the other hand, an increase of sensitive loads involving digital electronics and complex process controllers requires a pure sinusoidal supply voltage for proper load operation. Recently, multi converter FACTS devices, such as an interline power-flow controller (IPFC) and the generalized unified power-flow controller (GUPFC) are introduced. The aim of these devices is to control the power flow of multi lines or a sub network rather than control the power flow of a single line by, for instance, a UPFC.

When the power flows of two lines starting in one substation need to be controlled, an interline power flow controller (IPFC) can be used. An IPFC consists of two series VSCs whose dc capacitors are coupled. This allows active power to circulate between the VSCs. With this configuration, two lines can be controlled simultaneously to optimize the network utilization. The GUPFC combines three or more shunt and series converters. It extends the concept of voltage and power-flow control beyond what is achievable with the known two-converter UPFC. The simplest GUPFC consists of three converters—one connected in shunt and the other two in series with two transmission lines in a substation. The basic GUPFC can control total five power system quantities, such as a bus voltage and independent active and reactive power flows of two lines. The concept of GUPFC can be extended for more lines if necessary. The device may be installed in some central substations to manage power flows of multi lines or a group of lines and provide voltage support as well. By using GUPFC devices, the transfer capability of transmission lines can be increased significantly.

II. PROPOSED MC-UPQC SYSTEM:
A. Circuit Configuration
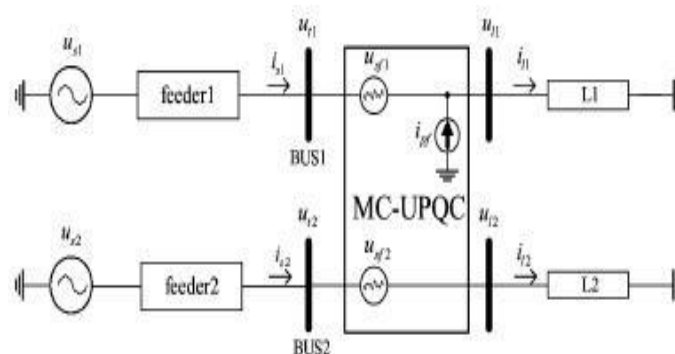The single-line diagram of a distribution system with an MC-UPQC is shown in Fig.1.

Fig.1 Single-line diagram of a distribution system with an MC-UPQC.

As shown in this fig.1, two feeders connected to two different substations supply the loads L1 and L2. The MC-UPQC is connected to two buses BUS1 and BUS2 with voltages of U_{t1} and U_{t2} respectively. The shunt part of the MC-UPQC is also connected to load L1 with a current of I_{l1} Supply voltages are denoted by U_{s1} and U_{s2}, while load voltages are U_{l1} and U_{l2} Finally, feeder currents are denoted by Is1 and Is2 and load currents are I_{l1} and I_{l2} Bus voltages U_{t1} and U_{t2} are distorted and may be subjected to sag/swell. The load L1 is a nonlinear/sensitive load which needs a pure sinusoidal voltage for proper operation while its current is non-sinusoidal and contains harmonics. The load L2 is a sensitive/critical load which needs a purely sinusoidal voltage and must be fully protected against distortion, sag/swell, and interruption.

These types of loads primarily include production industries and critical service providers, such as medical centers, airports, or broadcasting centers where voltage interruption can result in severe Economical losses or human damages.

B. MC–UPQC Structure

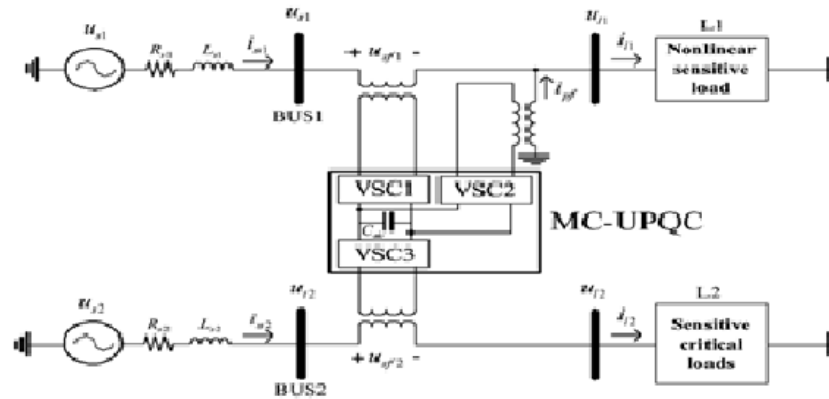The internal structure of the MC–UPQC is shown in Fig.2.

Fig.2 Typical MC-UPQC used in a distribution system.

It consists of three VSCs (VSC1, VSC2, and VSC3) which are connected back to back through a common dc-link capacitor. In the proposed configuration, VSC1 is connected in series with BUS1 and VSC2 is connected in parallel with load L1 at the end of Feeder1. VSC3 is connected in series with BUS2 at the Feeder2 end. Each of the three VSCs in Fig. 2 is realized by a three-phase converter with a commutation reactor and high-pass output filter as shown in Fig.3
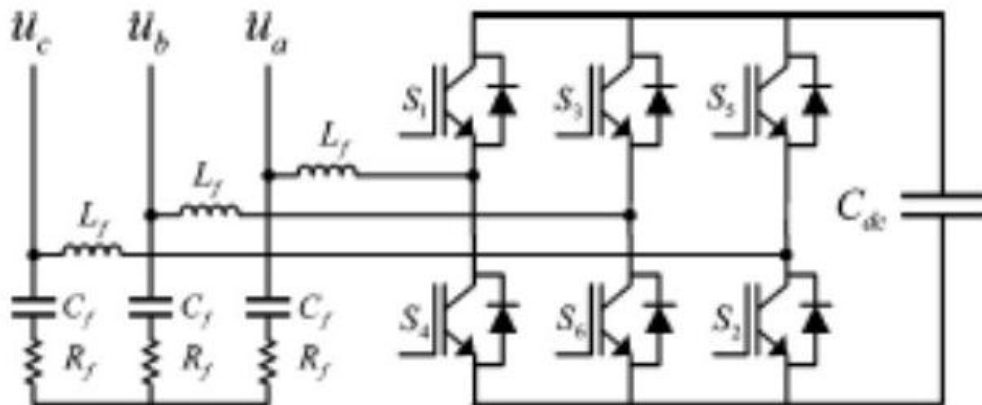

Fig.3 Schematic structure of a VSC.

The commutation reactor (L_f) and high- pass output filter (R_f,Cf) are connected to prevent the flow of switching harmonics into the power supply. As shown in Fig, all converters are supplied from a common dc-link capacitor and connected to the distribution system through a transformer. Secondary (distribution) sides of the series-connected transformers are directly connected in series with BUS1 and BUS2, and the secondary (distribution) side of the shunt-connected transformer is connected in parallel with load L1.

The aims of the MC-UPQC shown in Fig.3 are:
1) To regulate the load voltage (U_{t1}) against sag/swell and disturbances in the system to protect the nonlinear/sensitive load L1;
2) To regulate the load voltage (U_{t2}) against sag/swell, interruption, and disturbances in the system to protect the sensitive/ critical load L2;
3) To compensate for the reactive and harmonic components of nonlinear load current (i_{l2}) .

In order to achieve these goals, series VSCs (i.e., VSC1 and VSC3) operate as voltage controllers while the shunt VSC (i.e., VSC2) operates as a current controller. C. Control Strategy.

As shown in Fig.2, the MC-UPQC consists of two series VSCs and one shunt VSC which are controlled independently. The switching control strategy for series VSCs and the shunt VSC are selected to be sinusoidal pulse width-modulation (SPWM) voltage control and hysteresis current control, respectively. Details of the control algorithm, which are based on the d–q method [12], will be discussed later. Shunt-VSC: Functions of the shunt-VSC are:
1) To compensate for the reactive component of load L1 current;
2) To compensate for the harmonic components of load L1 current;
3) To regulate the voltage of the common dc-link capacitor.

Fig.3 shows the control block diagram for the shunt VSC. The measured load current (i_{l_abc}) is transformed into the synchronous dq0 reference frame by using

$$i_{l\_dq0} = T^{dq0}_{abc} \, i_{l\_abc} \qquad\text{-------- (1)}$$

where the transformation matrix is shown in (2), at the bottom of the page.

By this transform, the fundamental positive-sequence component, which is transformed into dc quantities in the d and q axes, can be easily extracted by low-pass filters (LPFs). Also, all harmonic components are transformed into ac quantities with a fundamental frequency shift

Where $i_{l\text{-}d}$, $i_{l\text{-}q}$ are d-q components of load current, $i_{l\text{-}d}, i_{l\_\text{-}q}$ are dc components, and $\overline{i}_{l\_d}, \overline{i}_{l\_q}$ are the ac components of

$$\overline{i}_{l\_d}, \overline{i}_{l\_q} \; .$$

If i_s is the feeder current and i_{pf} is the shunt VSC current and knowing $i_s = i_l - i_{pf}$, then d–q components of the shunt VSC reference current are defined as follows:

Consequently, the d–q components of the feeder current are

$$i_{s\_d} = \overline{i}_{l\_d}$$
$$i_{s\_q} = 0.$$

This means that there are no harmonic and reactive components in the feeder current. Switching losses cause the dc-link capacitor voltage to decrease. Other disturbances, such as the sudden variation of load, can also affect the dc link. In order to regulate the dc-link capacitor voltage, a proportional–integral (PI) controller is used as shown in Fig. The input of the PI controller is the error between the actual capacitor voltage (U_{dc}) and its reference value $\left(u^{ref}_{dc}\right)$. The output of the PI controller (i.e., i_{dc}) is added to the d component of the shunt-VSC reference current to form a new reference current as follows:

$$\begin{cases} i^{ref}_{pf\_d} = \overline{i}_{l\_d} + \Delta i_{dc} \\ i^{ref}_{pf\_q} = i_{l\_q} \end{cases} \qquad\text{------------------------------------- (2)}$$

As shown in Fig., the reference current in (9) is then transformed back into the abc reference frame. By using PWM hysteresis current control, the output-compensating currents in each phase are obtained

$$i^{ref}_{pf\_abc} = T^{abc}_{dq0} i^{ref}_{pf\_dq0}; \; (T^{abc}_{dq0} = T^{dq0^{-1}}_{abc}). \qquad\text{-- (3)}$$

Series-VSC: Functions of the series VSCs in each feeder are:

1) To mitigate voltage sag and swell;
2) To compensate for voltage distortions, such as harmonics;
3) To compensate for interruptions (in Feeder2 only).

The control block diagram of each series VSC is shown in Fig. The bus voltage $\left(u_{t\_abc}\right)$ is detected and then transformed into the synchronous dq0 reference frame using
Where

$$\begin{cases} u_{t1p} = \begin{bmatrix} u_{t1p\_d} & u_{t1p\_q} & 0 \end{bmatrix}^T \\ u_{t1n} = \begin{bmatrix} u_{t1n\_d} & u_{t1n\_q} & 0 \end{bmatrix}^T \\ u_{t10} = \begin{bmatrix} 0 & 0 & u_{00} \end{bmatrix}^T \\ u_{th} = \begin{bmatrix} u_{th\_d} & u_{th\_q} & u_{th\_0} \end{bmatrix}^T \end{cases} \qquad\text{-- (4)}$$

U_{t1p}, U_{t1n} and U_{t10} are fundamental frequency positive-, negative-, and zero-sequence components, respectively, and U_{th} is the harmonic component of the bus voltage. According to control objectives of the MC-UPQC, the load voltage should be kept sinusoidal with constant amplitude even if the bus voltage is disturbed. Therefore, the expected load voltage in the synchronous dq0 reference frame $\left(u^{exp}_{l\_dq0}\right)$ only has one value.

$$u^{exp}_{l\_dq0} = T^{dq0}_{abc} u^{exp}_{l\_abc} = \begin{bmatrix} U_m \\ 0 \\ 0 \end{bmatrix} \qquad\text{----------------- (5)}$$

where the load voltage in the abc reference frame $\left(u^{exp}_{l\_abc}\right)$ is

$$u^{exp}_{l\_abc} = \begin{bmatrix} U_m \cos(\omega t) \\ U_m \cos(\omega t - 120^\circ) \\ U_m \cos(\omega t + 120^\circ) \end{bmatrix} \qquad\text{--- (6)}$$

The compensating reference voltage in the synchronous dq0 reference frame $\left(u_{\text{sf\_}dq0}^{\overline{\text{ref}}}\right)$ is defined as

$$u_{\text{sf\_}dq0}^{\text{ref}} = u_{t\_dq0} - u_{l\_dq0}^{\exp}.$$ -- (7)

This means U_{t1p_d} in should be maintained at U_m while all other unwanted components must be eliminated. The compensating reference voltage is then transformed back into the abc reference frame. By using an improved SPWM voltage control technique (sine PWM control with minor loop feedback), the output compensation voltage of the series VSC can be obtained.

III.PROPOSED SIMULATION MODEL

The proposed MC-UPQC and its control schemes have been tested through extensive case study simulations using Mat lab. In this section, simulation results are presented, and the performance of the proposed MC-UPQC system is shown.
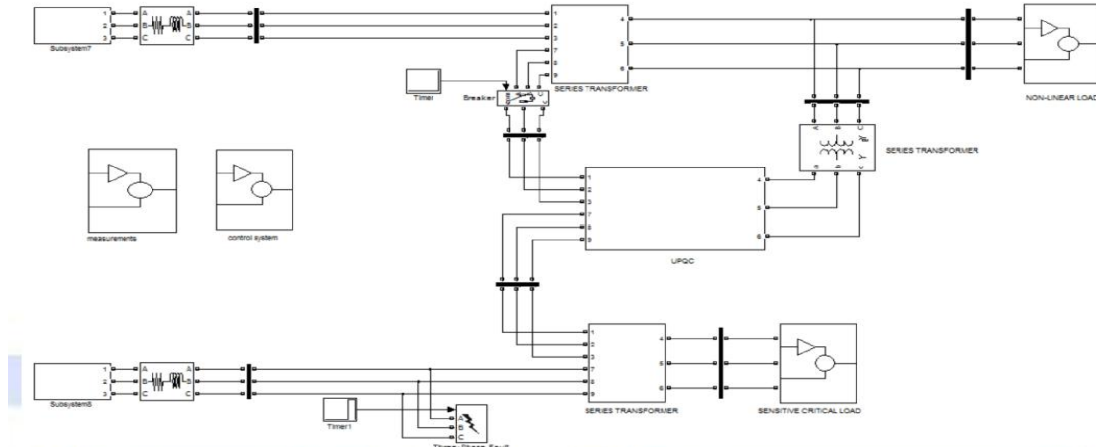

Fig.4 simulation model of MC UPQC
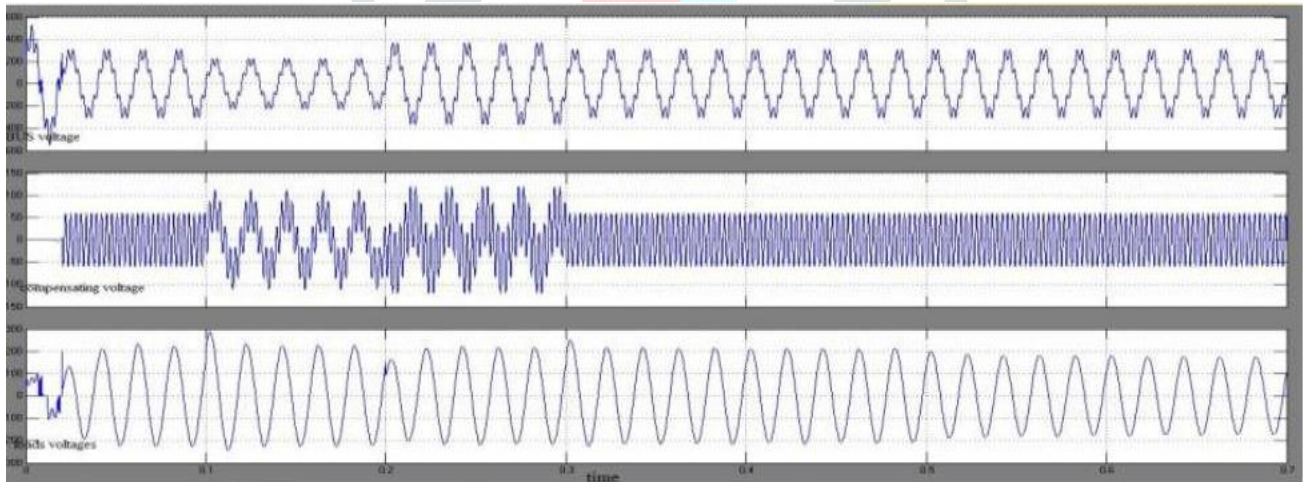
IV. SIMULATION RESULTS:

Fig.5 Simulation results for an upstream fault on Feeder2: BUS2 voltage, compensating voltage, and loads L1 and L2 voltages.
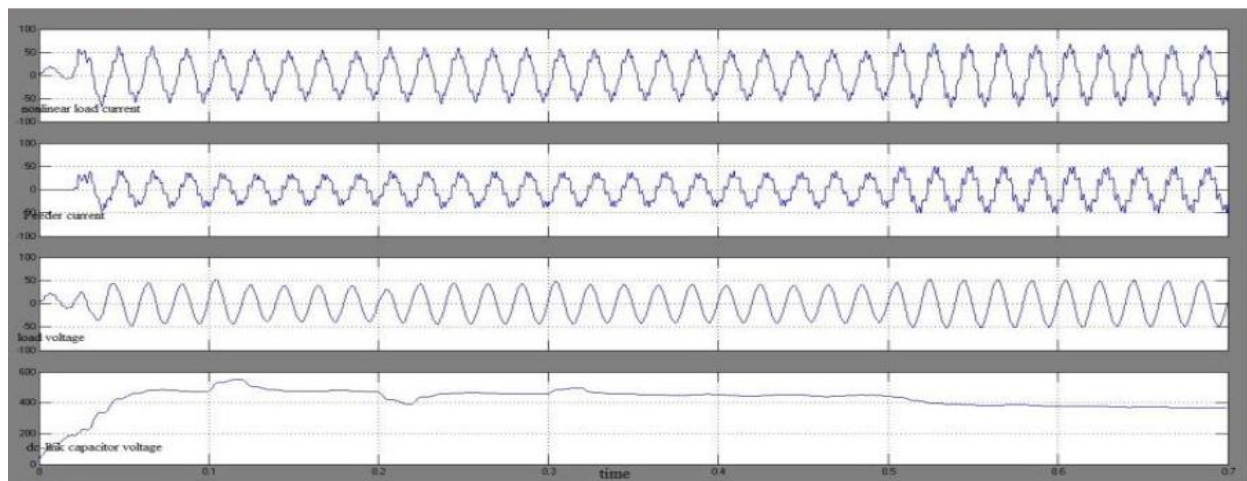

Fig.6 Simulation results for load change: nonlinear load current, Feeder1 current, load L1
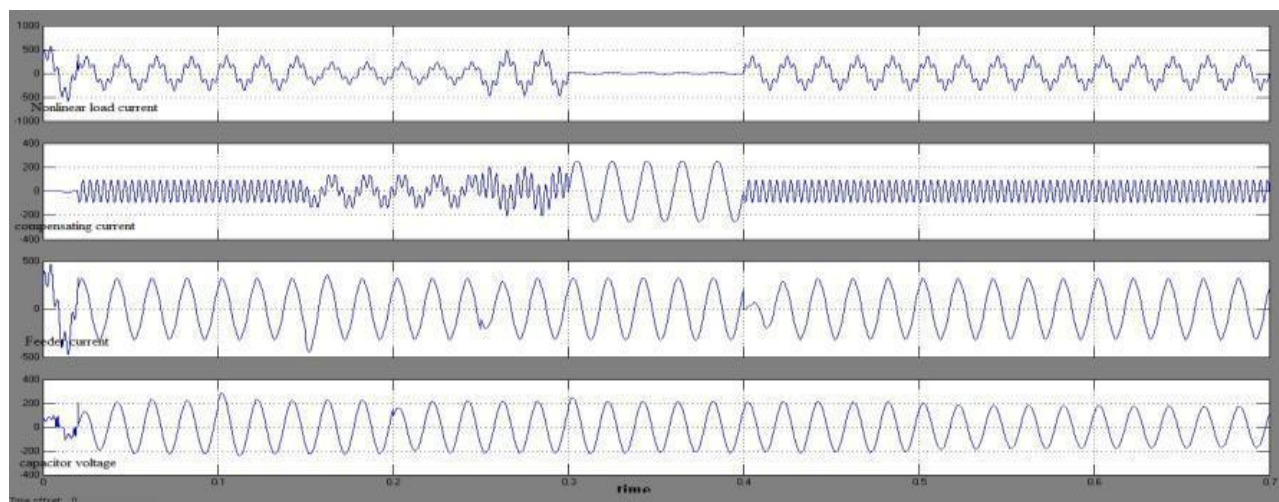Voltage, load L2 voltage, and dc-link capacitor voltage.

Fig.7 Nonlinear load current, compensating current, Feeder1 current, and capacitor voltage.

A. Distortion and Sag/Swell on the Bus Voltage

Let us consider that the power system in Fig. 2 consists of two three-phase three-wire 380(v) (rms, L-L), 50-Hz utilities. The BUS1 voltage (U_{t1}) contains the seventh-order harmonic with a value of 22%, and the BUS2 voltage (U_{t2}) contains the fifth order harmonic with a value of 35%. The BUS1 voltage contains 25% sag between 0.1s < t < 0.2s and 20% swell between 0.2s t < 0.3s. The BUS2 voltage contains 35% sag between 0.15s < t < 0.25 and 30% swell between 0.25s< t < 0.3s. The nonlinear/sensitive load L1 is a three-phase rectifier load which

Supplies an RC load of 10Ω and 30 F. Finally, the critical load L2 contains a balanced RL load of 10Ω and 100mH.

The MC–UPQC is switched on at t=0.02 s. The BUS1 voltage, the corresponding compensation voltage injected by VSC1, and finally load L1 voltage.

CONCLUSION:

In this paper, a new configuration for simultaneous compensation of voltage and current in adjacent feeders has been proposed. The new configuration is named multi-converter unified power-quality conditioner (MC-UPQC). The performance of the MC-UPQC is evaluated under various disturbance conditions and it is shown that the proposed MC-UPQC offers the following advantages:

1) Power transfer between two adjacent feeders for sag/swell and interruption compensation;

2) Compensation for interruptions without the need for a battery storage system and, consequently, without storage capacity limitation;

3) Sharing power compensation capabilities between two adjacent feeders which are not connected.

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